NEW ARCHITECTURES FOR HIGH PERFORMANCE GRANULAR POWER SUPPLIES

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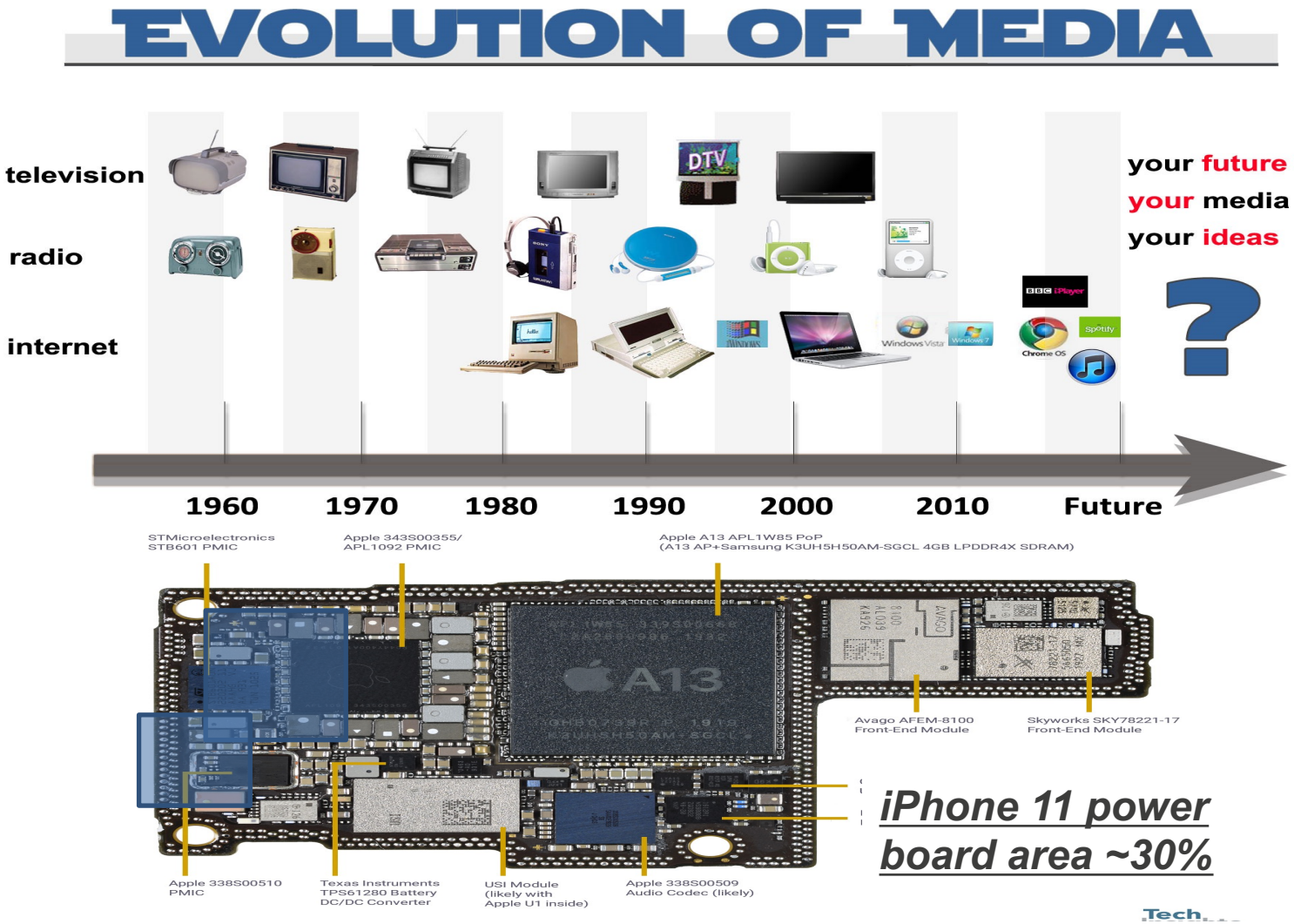
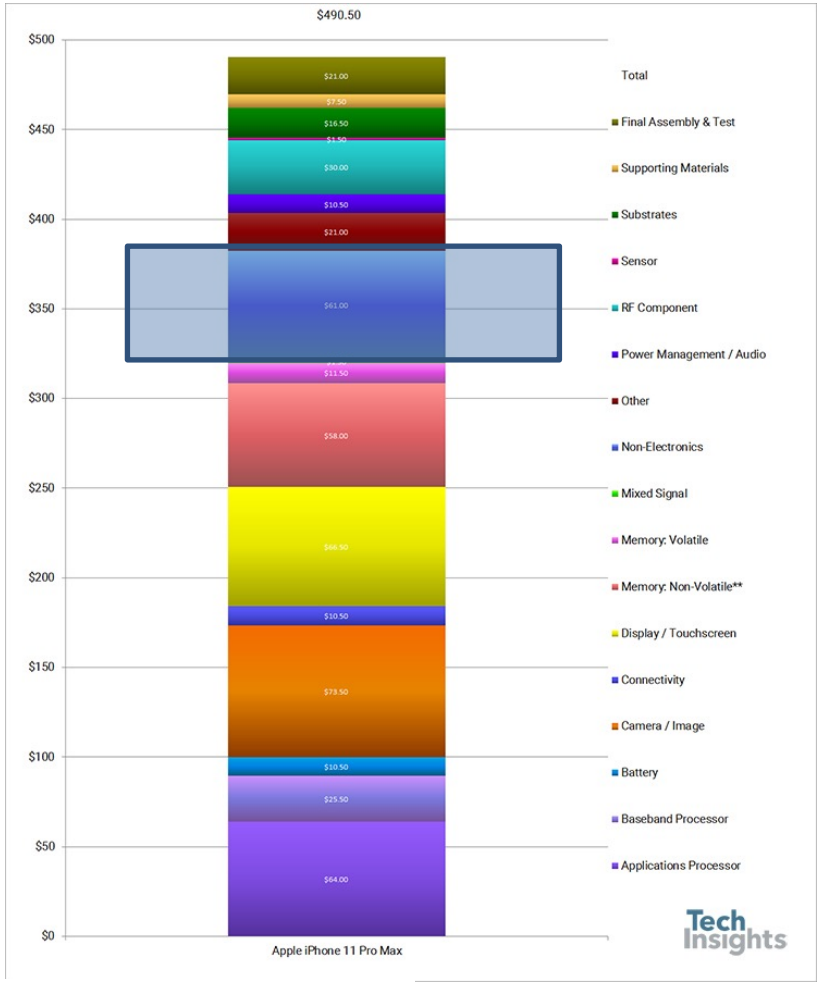
AGENDA

- Introduction
- Microprocessor Power Supply- Challenges
- Integrated Voltage Regulator (IVR)
- Architectures for Integrated Voltage Regulator
- Comparison of different IVR Architectures
- Key Challenges & Summary

EVOLUTION OF PRODUCTS & POWER DELIVERY

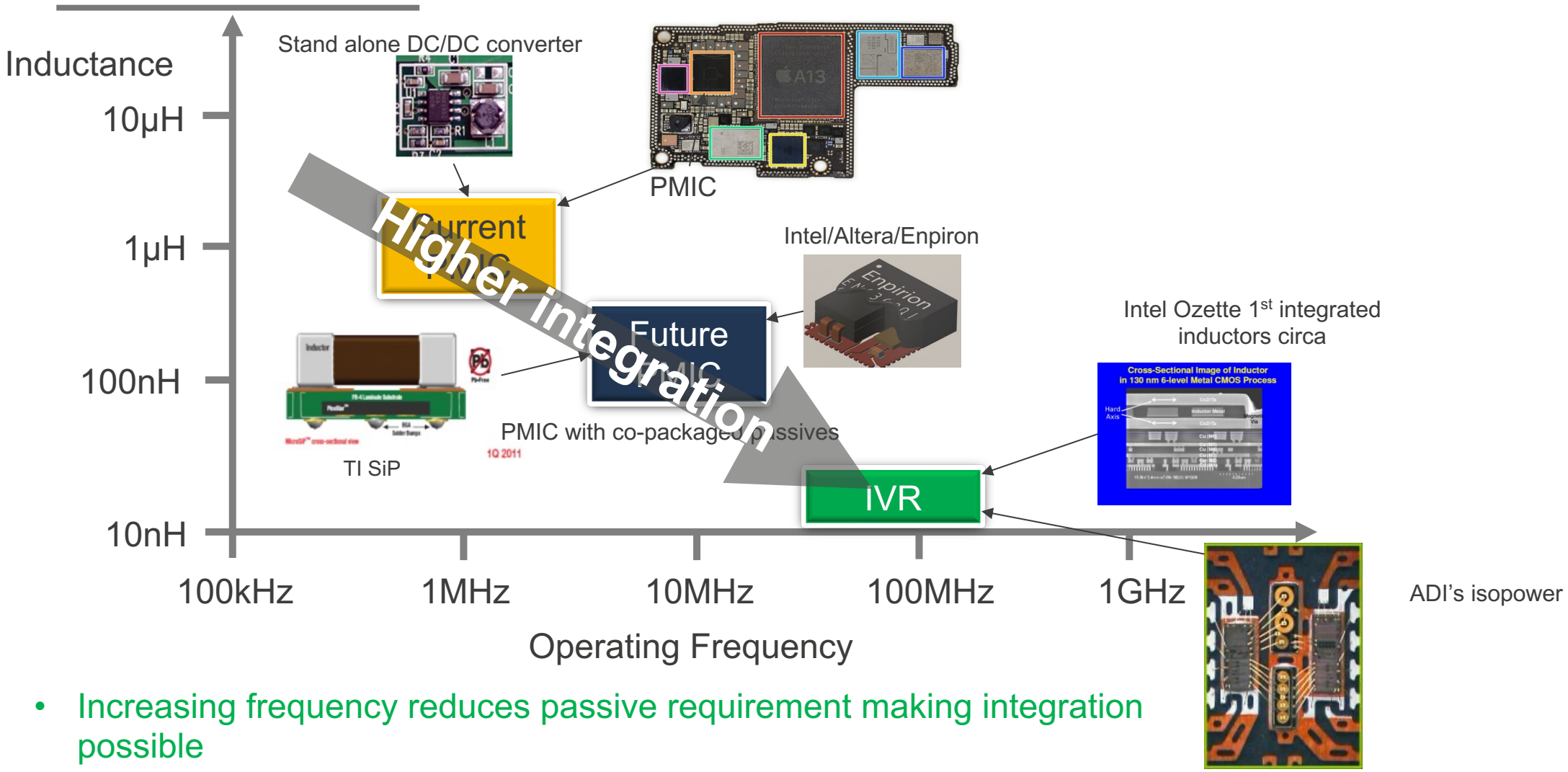


iPhone 11 – Power cost ~ 12%



Achieving increased power density, performance & cost requires integration of PMIC with SoC

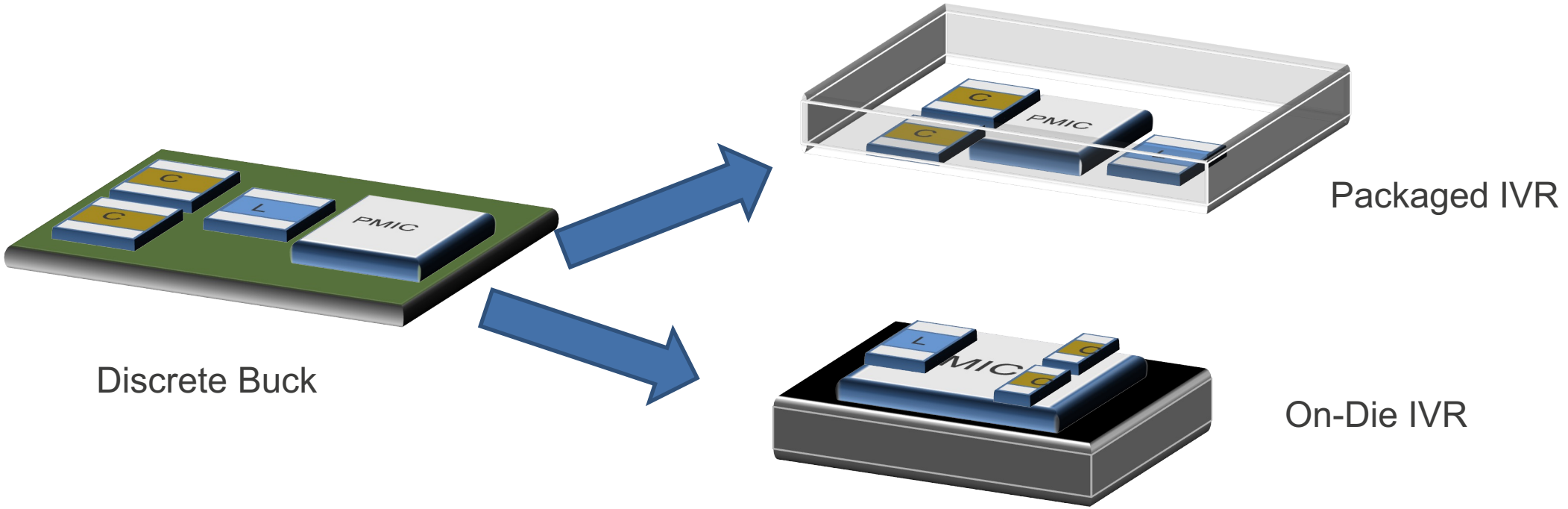
REDUCING THE AREA FOR POWER CONVERSION



- Increasing frequency reduces passive requirement making integration possible

INTEGRATED VOLTAGE REGULATOR

- IVR is a highly miniaturized, integrated power management device
- IVR offers high performance, efficiency, size & cost benefits to power hungry highly integrated electronics applications
- IVR integrates switches, control, drivers, external components on a single platform (package or on-die)
- IVR can be integrated directly with application within the same package or on the same die

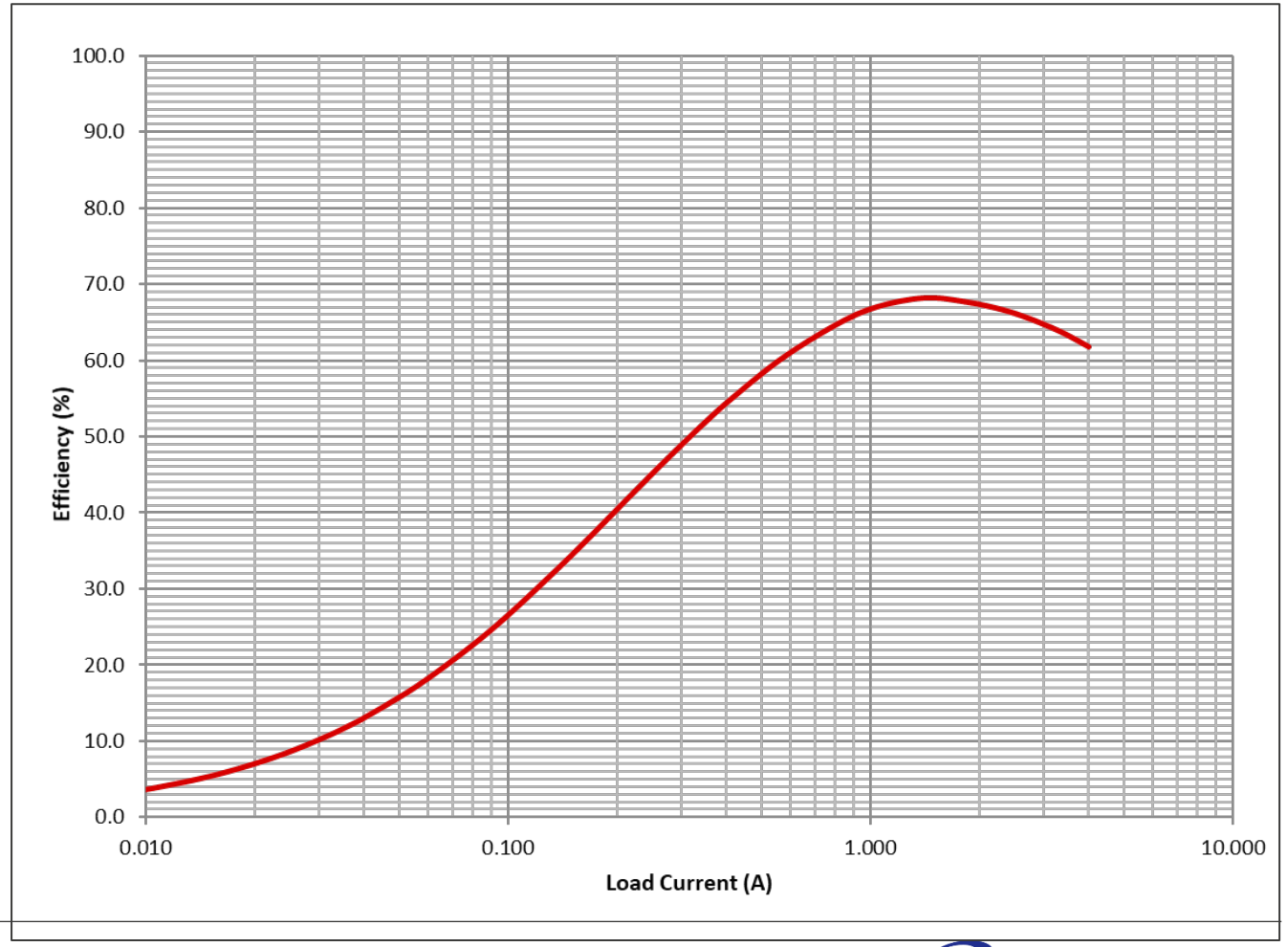


TYPICAL SPECIFICATIONS FOR MICROPROCESSOR POWER DELIVERY

- Input Voltage- 5V-2.5V (3.8V –typical)
- Output Voltage- 1.2V-0.5V (0.8V – typical)
- Output current- 2A/phase (typical)
- Solution height- 0.3mm (for integration with processor)
- Integration technology- Co-package with SoC
- Inductor- 20nH (Package inductors)
- Capacitor- 1uF (Package capacitors)

TRADITIONAL BUCK CONVERTER

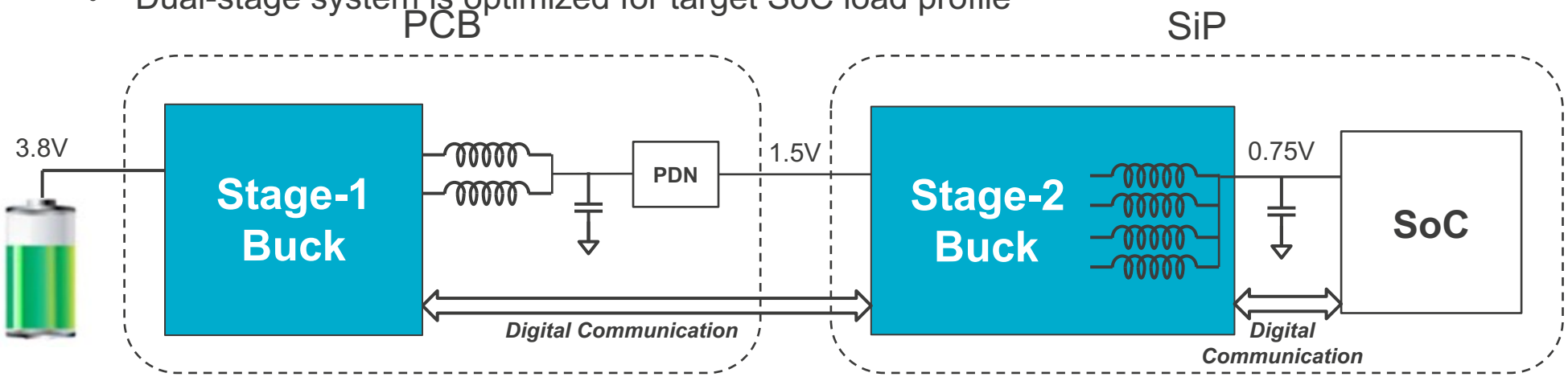
- For L-20nH, Cin/Cout-1uF
- Buck converter switching at 15MHz for maximum efficiency
- Peak efficiency of 69%
- Significant drop in efficiency for package L/C
- Existing architecture cannot be used for powering SOCs



DUAL STAGE BUCK ARCHITECTURE

Dual-stage buck system

- Stage-1 pre-regulator typically remains with main system PMIC
- Stage-2 high-frequency buck is in-package with SoC
- Dual-stage system is optimized for target SoC load profile



- Target fsw < 5MHz
- Target efficiency ~93% @ 2:1 voltage ratio
- Low accuracy, high efficiency, low bandwidth, low power modes
- External magnetics

Target fsw > 50MHz

Target efficiency ~85% @ 2:1 voltage ratio

High accuracy, high efficiency, wide bandwidth, droop mitigation

On-die/in-package magnetics

BENEFITS OF DUAL-STAGE SYSTEM

1. Wide bandwidth buck converter (stage-2 regulator)
- Very effective at eliminating 2nd and 3rd droop
- Limited effect on 1st droop due to bandwidth limitations

2. Large on-die decoupling capacitors
- Very effective at reducing 1st droop
- Tends to be very area intensive (even with 20fF/µm MiM capacitors).

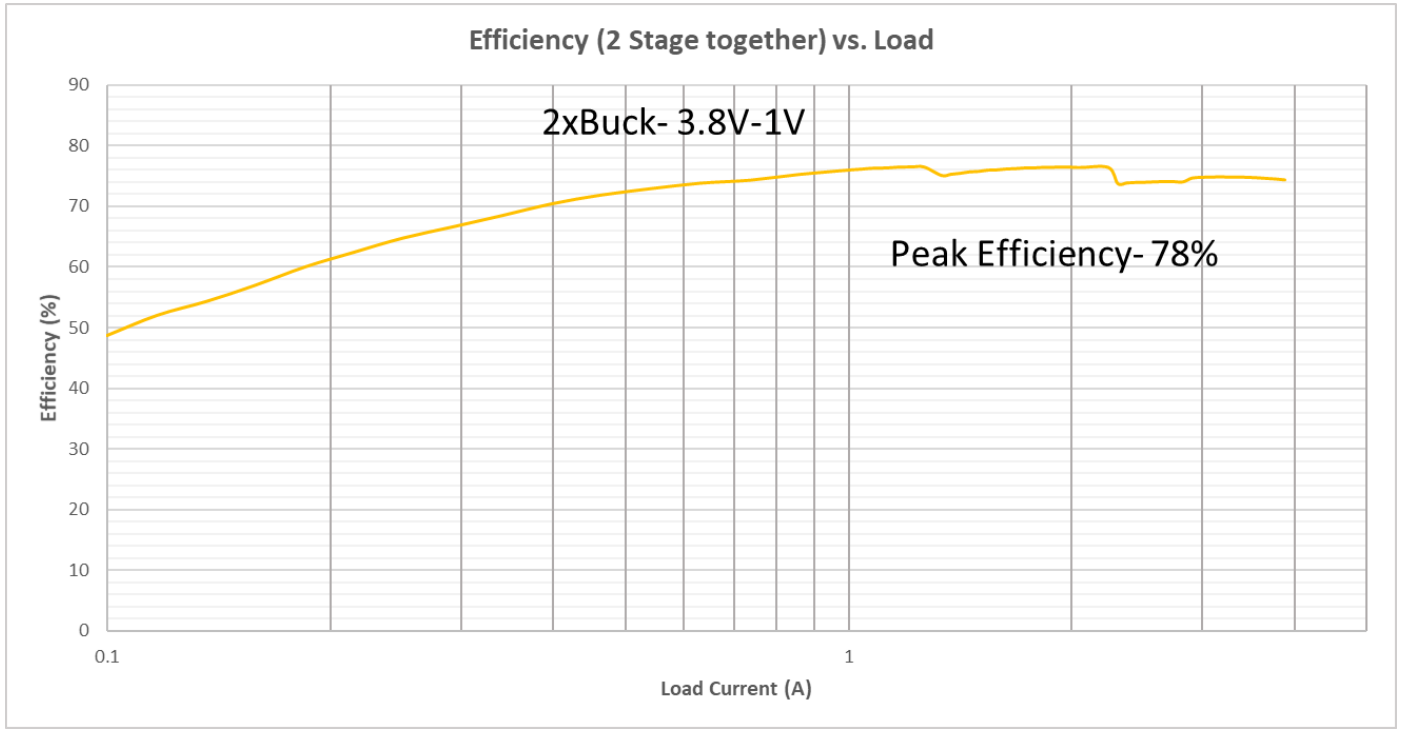
3. SoC clock stretching in response to voltage droop
- Requires close interaction between PMIC and SoC to detect and respond to droop
- Careful balance between too much and not enough clock stretching

4. Parallel high-speed OTA
- Behaves as a closed-loop wide bandwidth parallel current source
- Low efficiency, but only triggered under droop conditions

5. Non-linear droop response
- Synchronous non-linear phase alignment on droop detection
- Use of fast triggers and high-speed comparators
- Non-linear response to droop conditions is effective but difficult to control

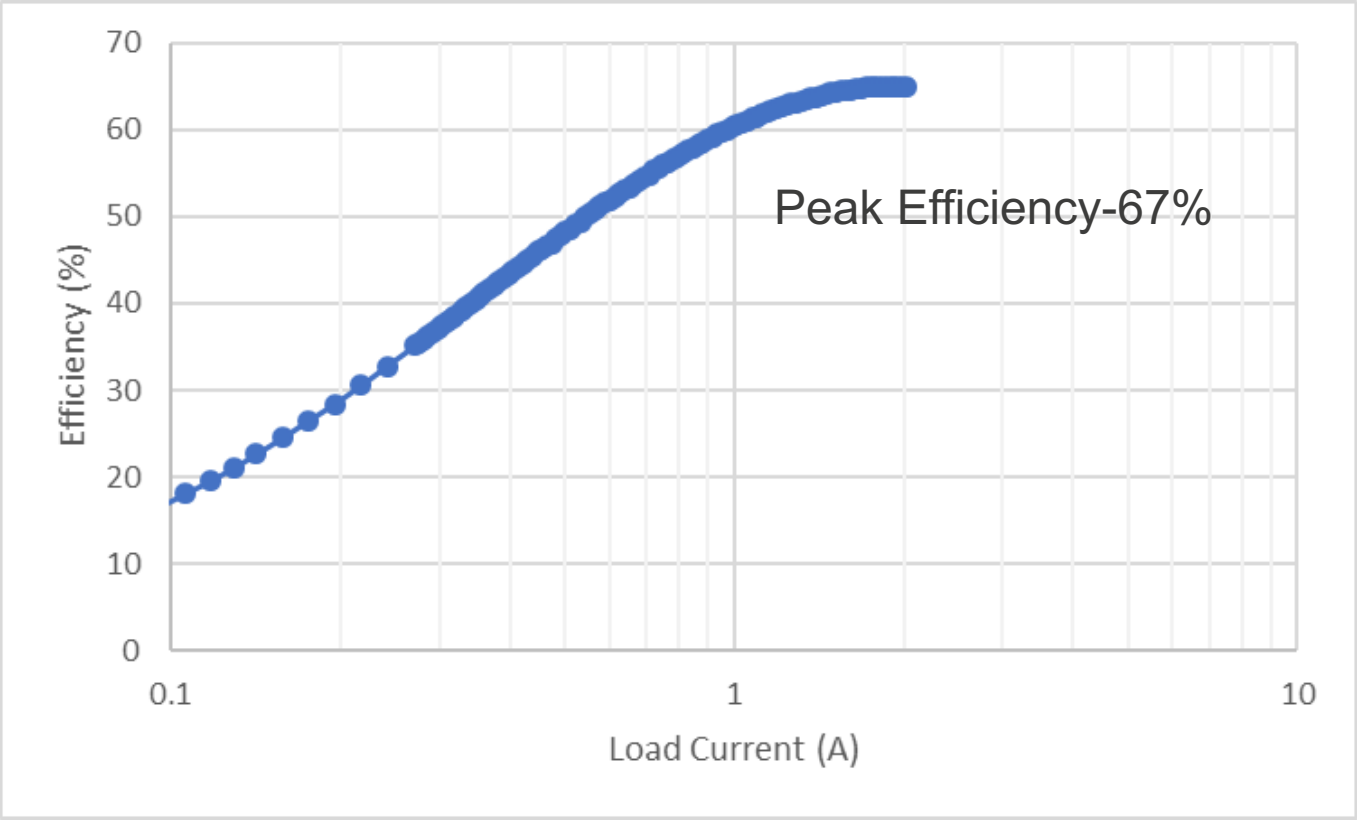
TWO STAGE BUCK CONVERTER-1

- Two stage solution with standard buck as 1st stage and IVR as 2nd stage
- Standard buck +IVR architecture to improve efficiency by reducing the voltage swing across the inductor
- 1st buck uses ferrite inductor (470nH) & PMIC sits outside the package; 2nd stage uses package inductors & sits within the same package as SoC



TWO STAGE BUCK CONVERTER-2

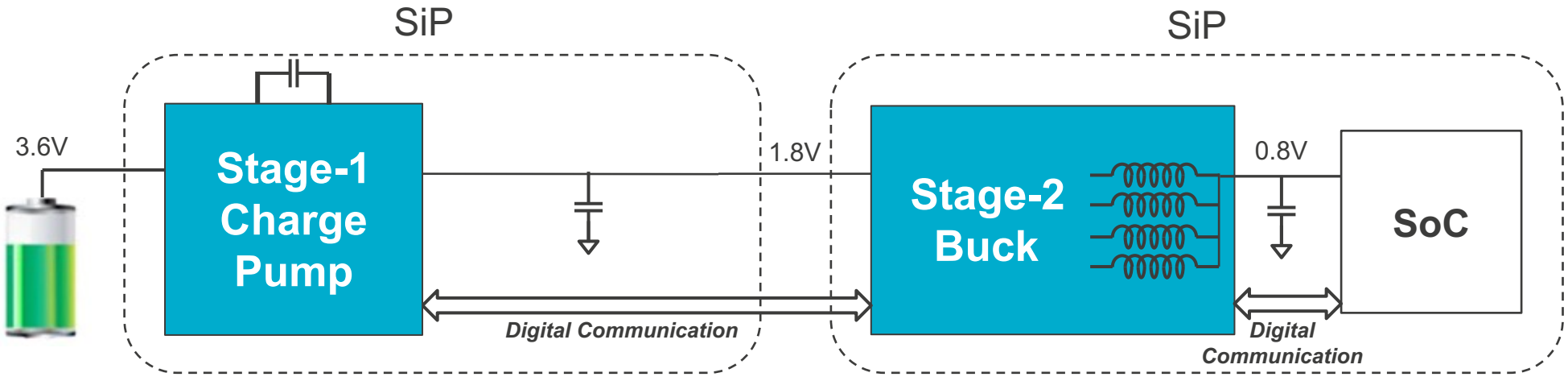
- Two stage solution with buck as 1st stage and IVR as 2nd stage
- 1st & 2nd bucks use package inductor (20nH) & both PMICs sit inside the package
- 10% drop in efficiency when 470nH inductor is replaced by 20nH



ARCHITECTURES FOR FULL INTEGRATION OF IVR

- Traditional solution of single stage and dual stage bucks do not offer significant performance when using package passives
- Need to look at different architectures if we want to achieve full integration, while using a dual stage architecture
- Different architectures which offer the opportunity to fully integrate PMIC + passives
  - Charge pump + Buck
  - Charge pump + Charge pump +LDO
  - Multi level Converter (MLC)
- These three architectures allow the use of smaller, faster switches, which can operate efficiently at higher switching frequencies, resulting in improved performance with smaller package compatible passives

SWITCH-CAP + IVR CONVERTER

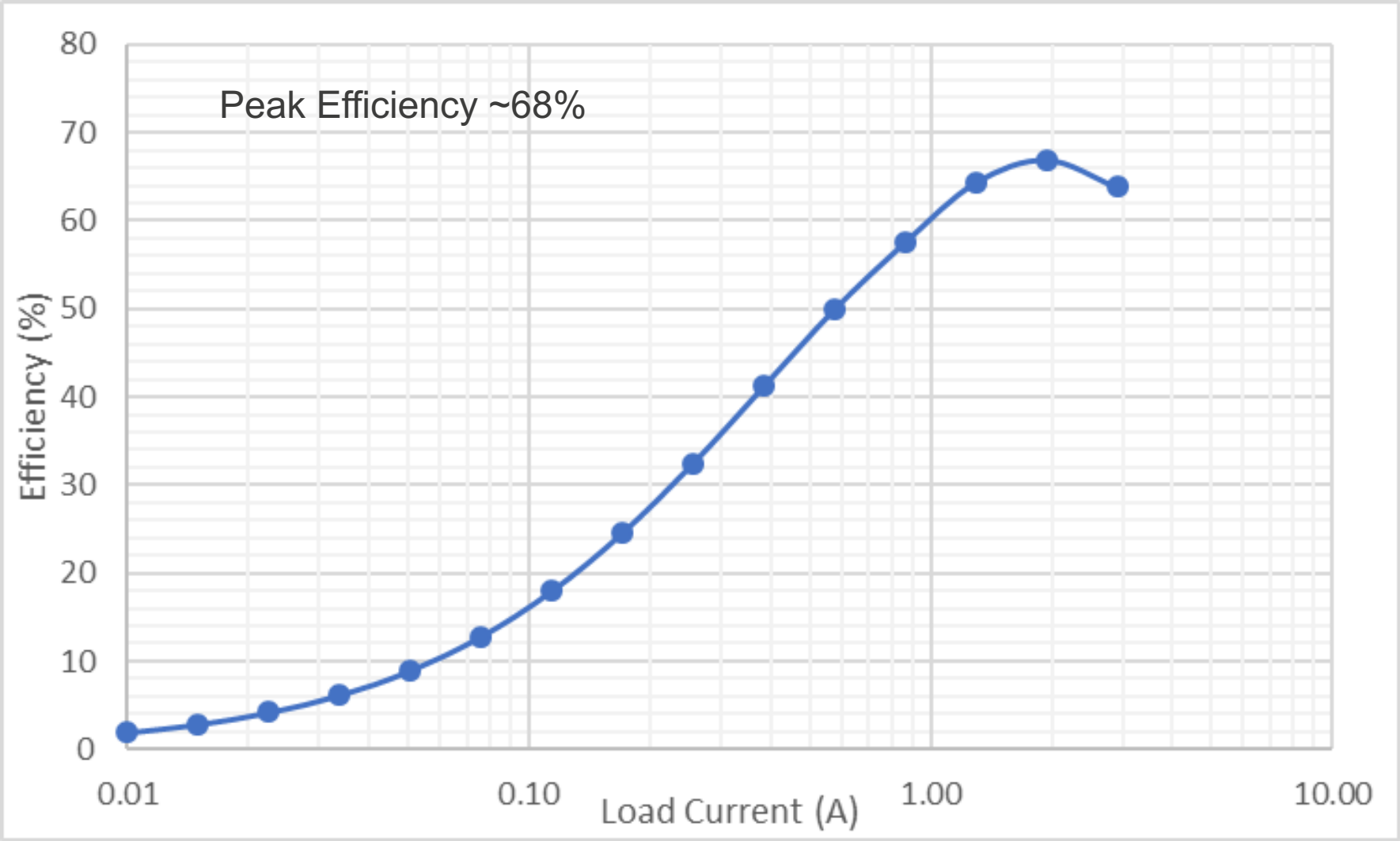


- Target fsw < 5MHz
- Step down @ 2:1 voltage ratio
- Integrated caps/package MLCC
- Loosely regulated output

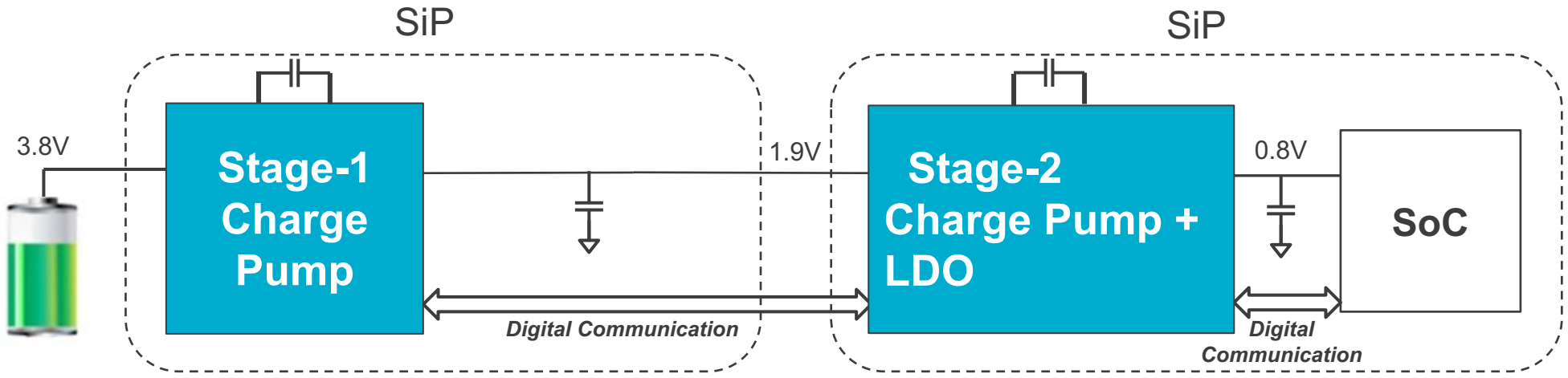
- Target fsw > 10MHz
- On-die/in-package magnetics
- Fully regulated output

SWITCHED CAP+IVR CONVERTER

- Efficiency impacted by need to use higher voltage devices for both stages as charge pump output is around 1.9V



SWITCH CAP X 2 + LDO CONVERTER

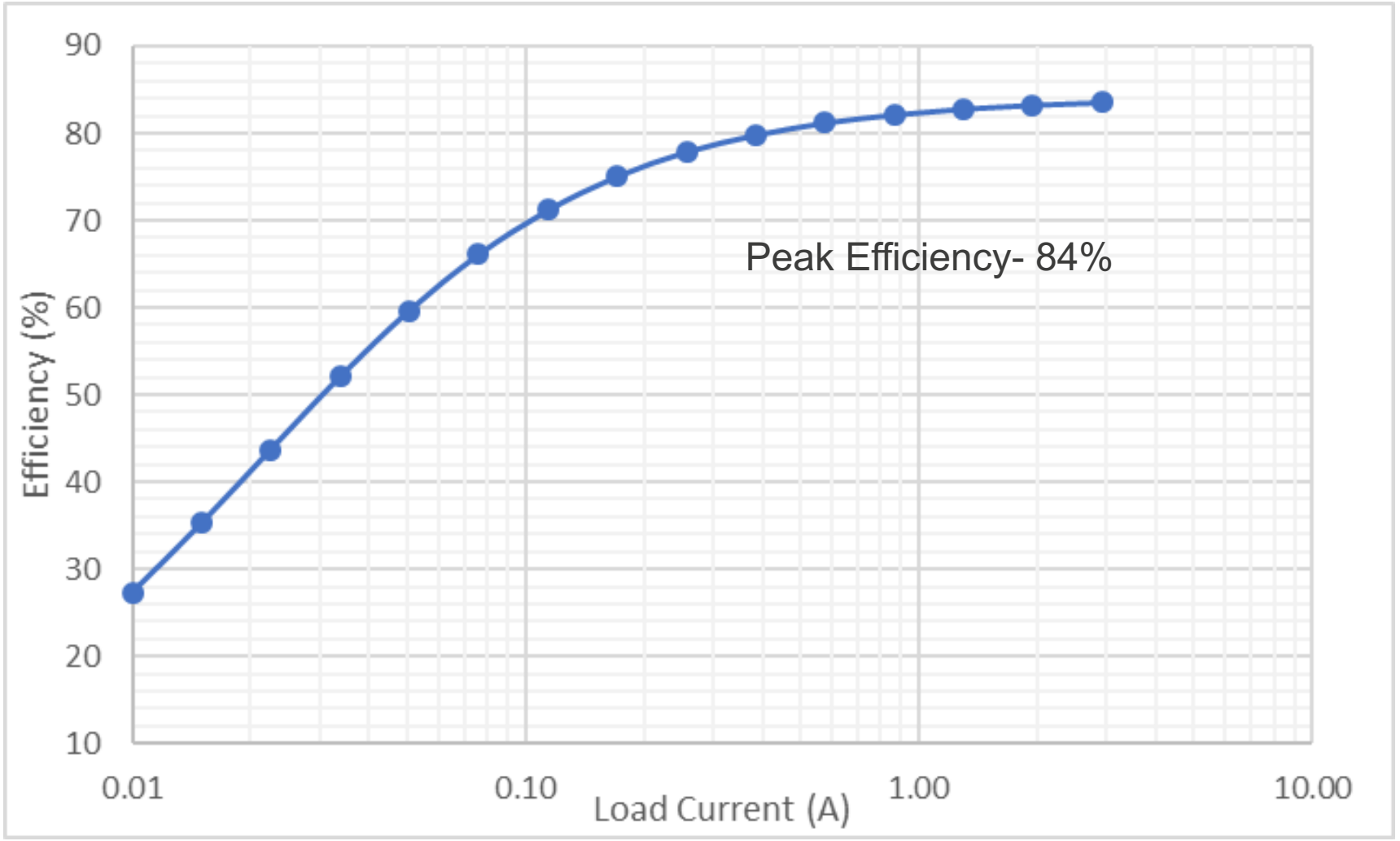


- Target fsw < 5MHz
- Step down @ 2:1 voltage ratio
- Integrated caps/package MLCC
- Loosely regulated output

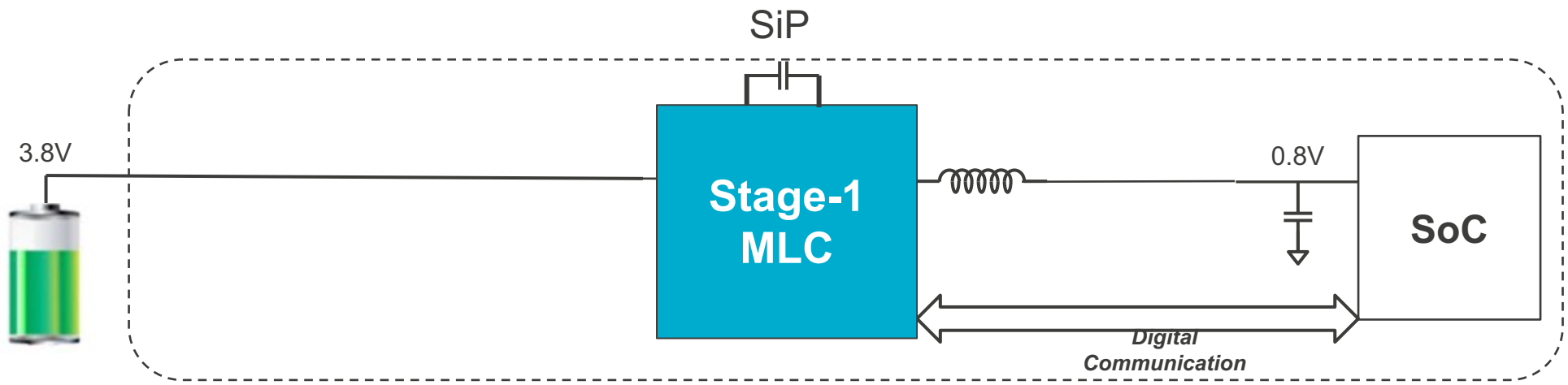
- Target fsw > 5MHz
- Step down @ 2:1 voltage ratio
- Integrated caps/package MLCC
- Fully regulated output

SWITCH CAP X 2+LDO CONVERTER

- Improved efficiency however requires twice the silicon area compared to 1x buck
- Drawback- if the input voltage changes the impact on performance can be significantly



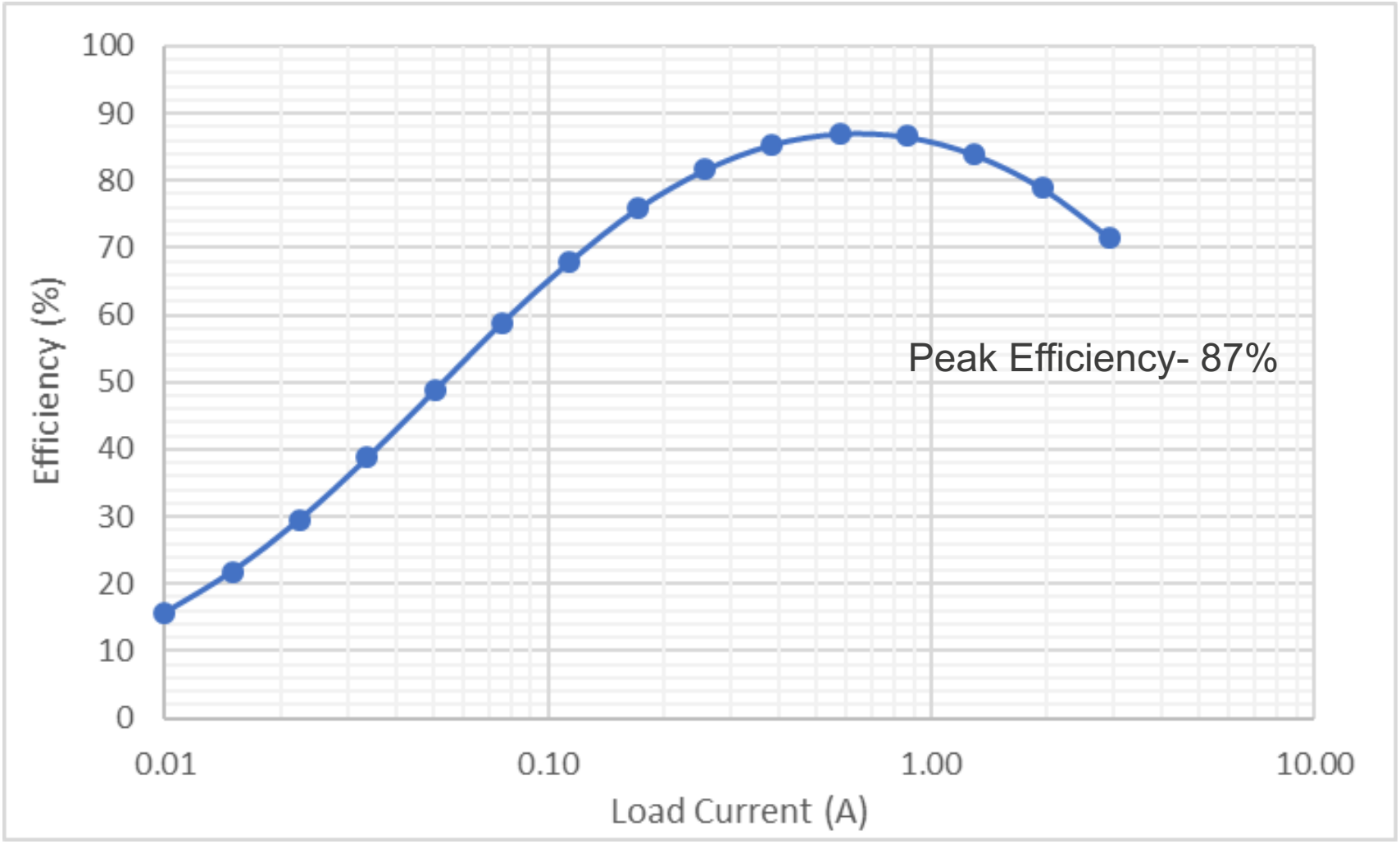
MULTI LEVEL CONVERTER



- Target fsw < 10MHz
- Low accuracy, high efficiency, low bandwidth, low power modes
- Integrated caps/package MLCC
- Integrated Magnetics
- Fully regulated output

MULTI LEVEL CONVERTER

- Voltage swing across the switch and inductor reduced by half; hence significant improvement in efficiency
- Drawback- increase in silicon area



SUMMARY OF DIFFERENT ARCHITECTURE OPTIONS

Five main PMIC architecture options for microprocessor power supply

1. 1xBuck: single stage 3.6V to 0.8V direct conversion
2. 2x Buck: 1st stage from 3.6V to 1.5V, 2nd stage from 1.5V to 0.8V
3. CP + Buck: unregulated 1st stage charge-pump from 3.6V to ~1.8V, 2nd stage from 1.8V to 0.8V
4. CP+CP+LDO: unregulated 1st stage charge pump from 3.6V to ~1.8V, 2nd stage from 1.8V to ~0.9V; LDO from 0.9V to 0.8V
5. MLC: single stage regulation from 3.6V to 0.8V

Parameters	1x Buck	2x Buck	CP+Buck	CP+CP+LDO	MLC
Peak efficiency	70%	70%	70%	85%	87%
Package size (approx.)	Y mm^2	0.8Y mm^2	1.5Y mm^2	2Y mm^2	1.5Ymm^2
Comments	Poor peak eff. & moderate cost increase (base case)	Smaller solution & similar efficiency	Similar efficiency & moderate cost increase	Excellent efficiency & performance changes with Vin	Excellent efficiency & higher cost