System Integrated Manufacturing and Packaging Trends and Roadmaps

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EVSTS
EFFICIENT VEHICLES AND SUSTAINABLE TRANSPORTATION SYSTEMS

Arizona State University
THE UNIVERSITY OF ALABAMA
UNIVERSITY OF LOUISVILLE
TEXAS The University of Texas at Austin
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Phase I: 2016-2022; Phase II: 2022-2027

https://evsts.asu.edu

NSF Center for Efficient Vehicles and Sustainable Transportation Systems (EVSTS)

Center for Efficient Vehicles and Sustainable Transportation Systems

EVSTS home | Research | Projects | How it works | Why participate | Leadership | Events

Getting Around. Our vehicles – getting us to work. To school. To family. To fun. Now more than ever, ground transportation for humans – plus the necessity of effectively, efficiently, and quickly transporting vital goods – is more than a priority. It's a lifeline.

Research = Results. This center combines the best academic minds from four universities with industry-leading OEMs and their suppliers to work together on applied, pre-competitive research. The result? Technologies, methodologies, and tools that shape all aspects of energy-efficient, environmentally sustainable ground vehicles and the infrastructure that supports them.

Member login

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Thrust areas: Electrified Vehicle Powertrains, Conventional Powertrains and Alternative Fuels, Vehicle Systems Optimization, Efficient/Sustainable Autonomous Vehicles, Transportation Systems and Infrastructure

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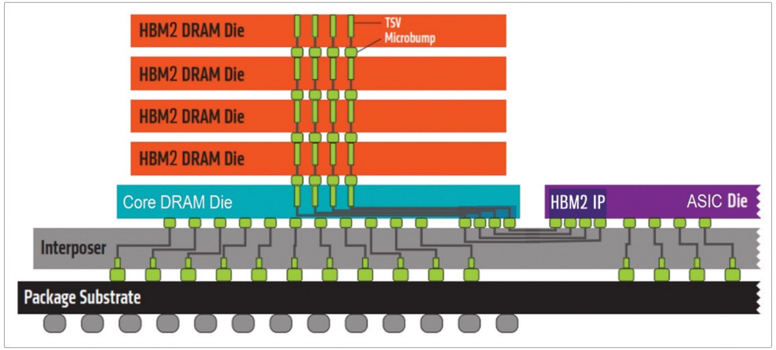
Industry members

cruise, Cummins, DGIST (대구경북과학기술원, Daegu Gyeongbuk Institute of Science & Technology), dialog SEMICONDUCTOR, ERG, Ford, GM, HUAWEI, HYUNDAI, KOPRI (Korea Polar Research Institute), LG&E KU (PPL companies), LG Chem, LG Innotek, NXP, ON Semiconductor, TARDEC, TDK, Texas Department of Transportation, TOYOTA

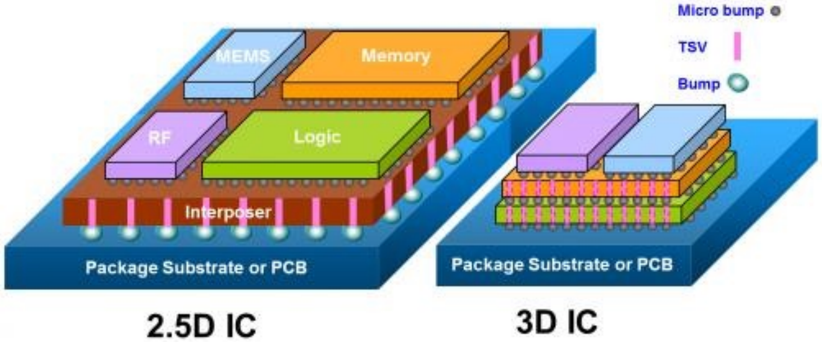
New: U-HAUL

The Importance of Advanced Packaging

- Packages provide power, signal, mechanical stability, and thermal dissipation to Si chips
- Complex 2.5D and 3D designs can place multiple chips side by side, or stack them on top of each other
- Allows scaling without shrinking transistors
- Can incorporate many kinds of chips and features into a single package



Source: SemiWiki 2018

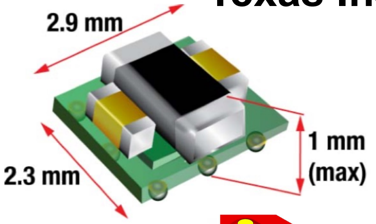


Integration of Inductor in IVR

- **Discrete inductor on mother board**

Texas Instruments

TPS 82671 MicroSiP
Step-Down Converter

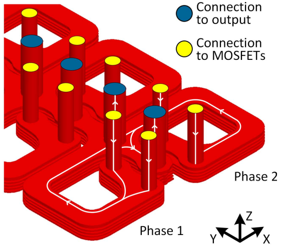


Surface mount inductor

- **Inductor on/in package**

Air core inductor

Large size & EMI

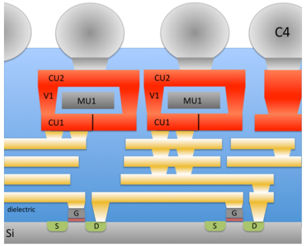


Intel

Magnetic Materials

Direct integration of magnetic core
Advantages: Smaller footprint; low height profile
Challenges: material compatibility; thermal effect

- **Inductor on Si chip**



Post CMOS Si or interposer: Ferric

Challenge: Dimension

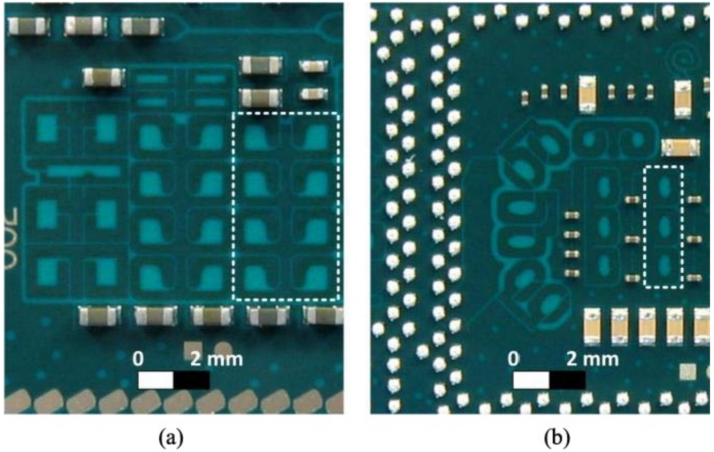


Figure.1 Close-up view of the inductors integrated in (a) 22-nm processor (b) 14nm processor. [1]

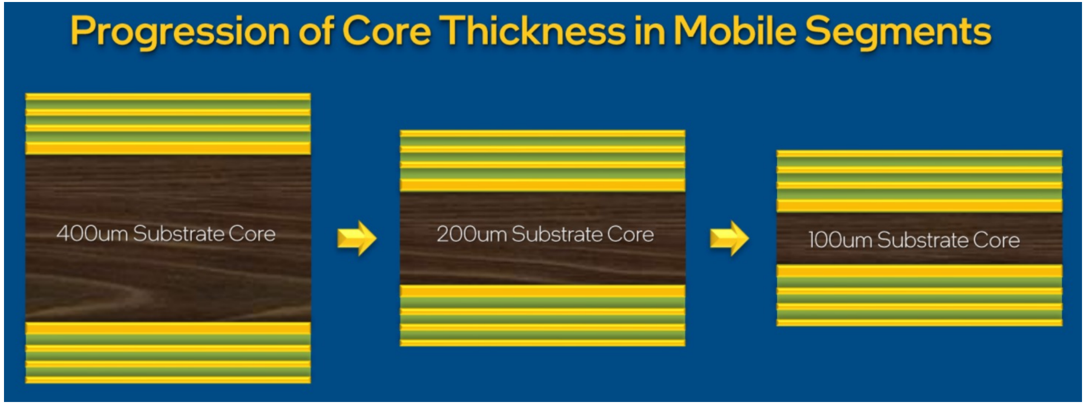
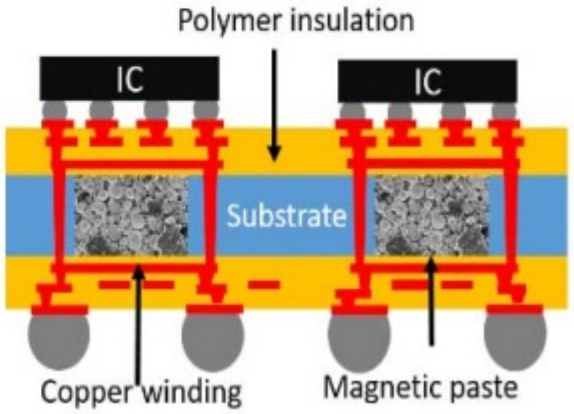


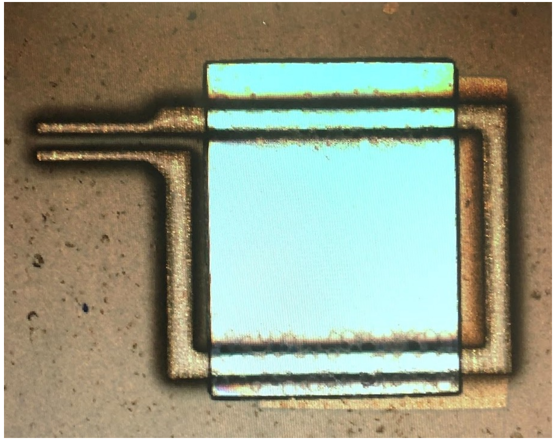
Figure.2 The substrate core thickness scaling down of 3 generations of a mobile CPU. The inductors are integrated in this layer. [2]

[1] Lambert, William J., et al. "Package inductors for Intel fully integrated voltage regulators." *IEEE transactions on components, packaging and manufacturing technology* 6.1 (2015): 3-11.
[2] Kaladhar Radhakrishnan. “Integrated Magnetics Magnetic Inductors for Next Generation IVR.” The 7th International Workshop on Power-Supply-on-Chip (conference), 2021, Philadelphia, PA.

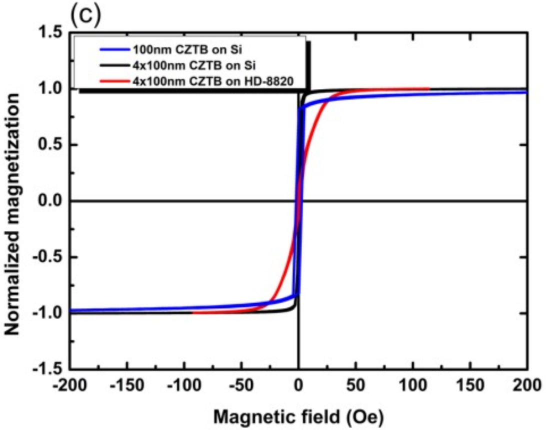
Challenge: Magnetic Core Integration



The schematic of a magnetic core inductor. A kind of magnetic flakes mixed in polymer matrix is used as core material. [1]

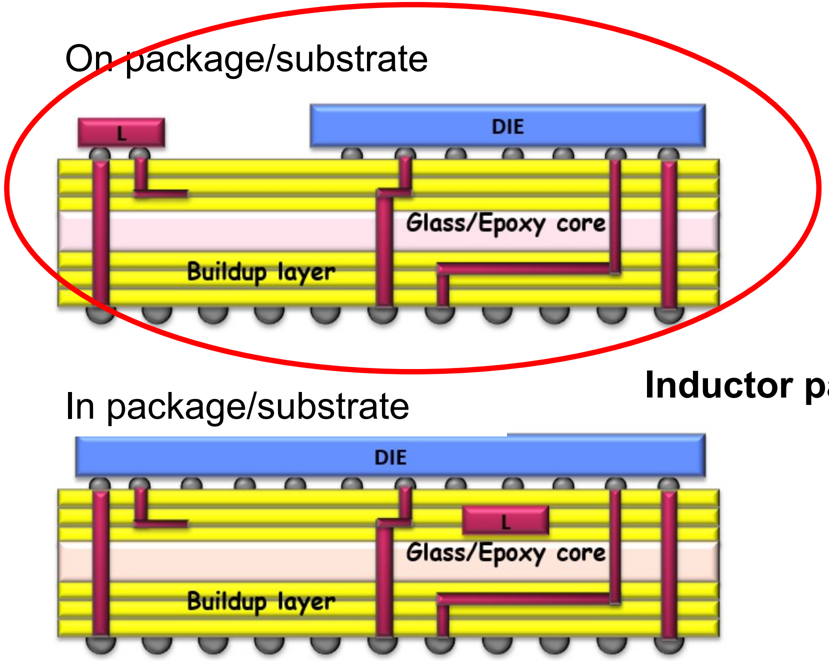


Our fabricated device. CoZrTaB is used as core material.

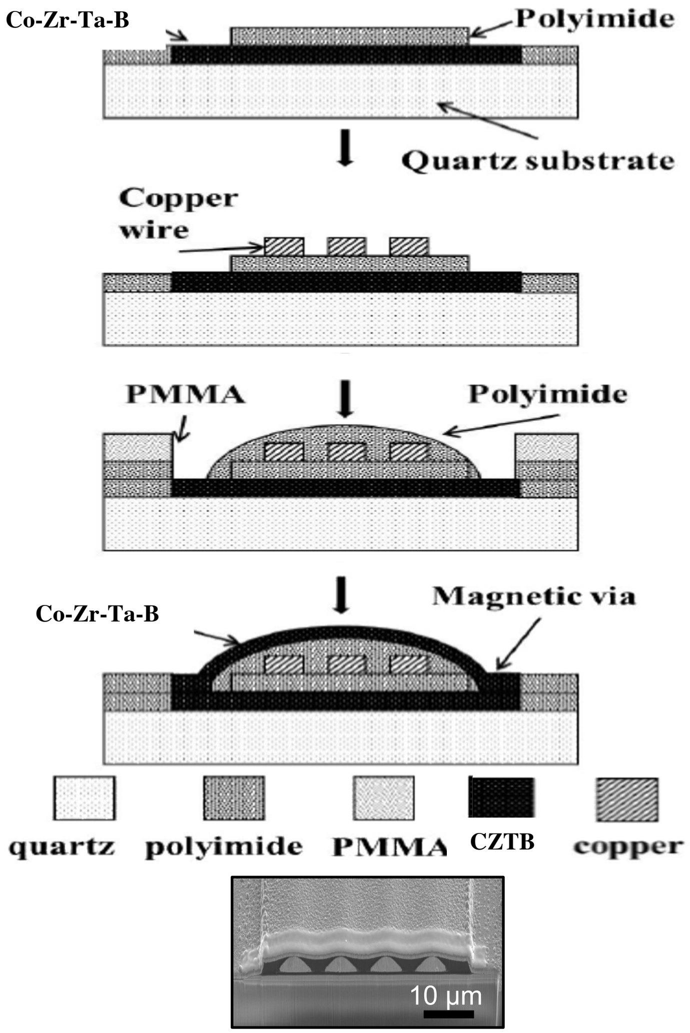


The B-H loop of CoZrTaB thin films on different substrates. [2]

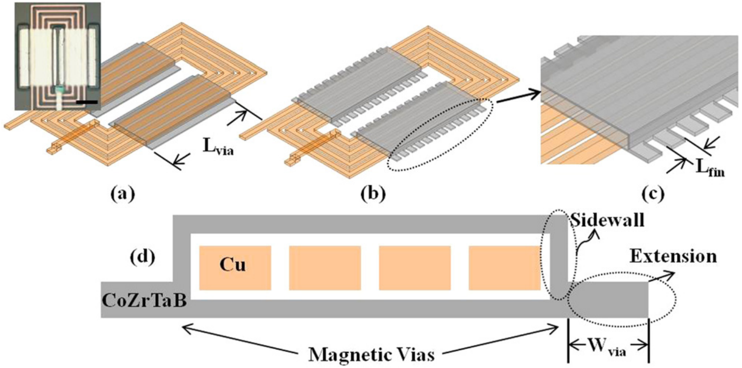
[1] Sun, Teng, et al. "Substrate embedded thin-film inductors with magnetic cores for integrated voltage regulators." *IEEE Transactions on Magnetics* 53.10 (2017): 1-9.
[2] Wu, Yanze, I-Chen Yeng, and Hongbin Yu. "The improvement of CoZrTaB thin films on different substrates for flexible device applications." *AIP Advances* 11.2 (2021): 025139.

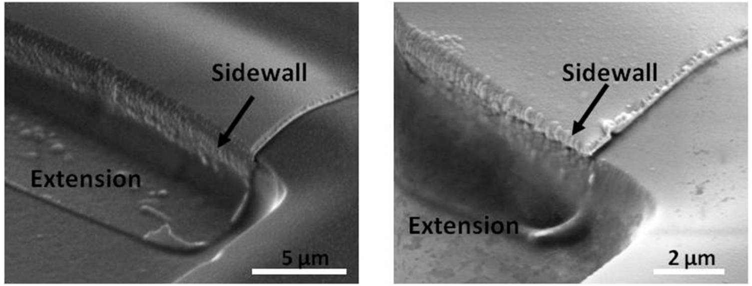


Inductor part



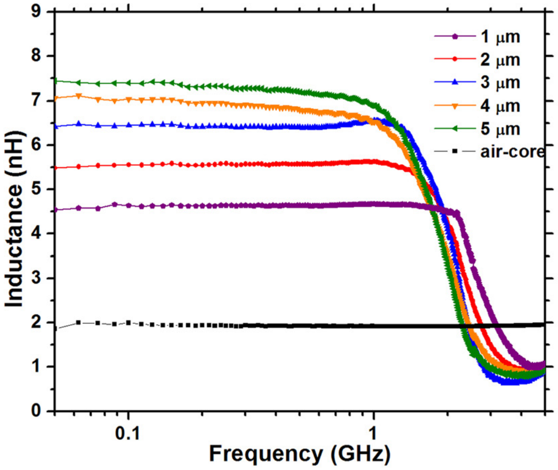
Two kinds of integration methods for the inductor devices.



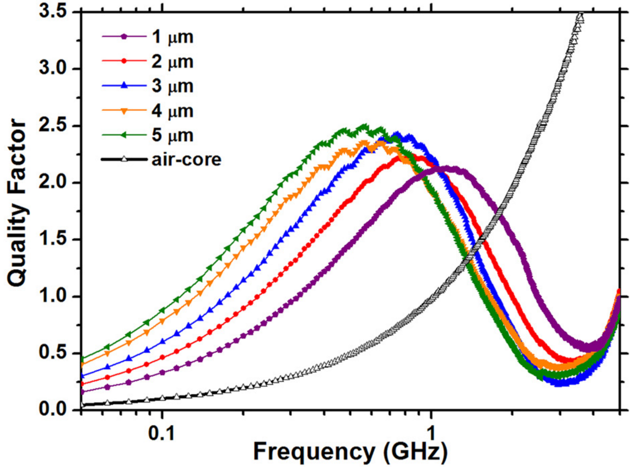


	Ni-Fe	Co-Zr-Ta	Co-Zr-Ta-B
μ	<650	1000	**1070**
ρ	20 μΩ·cm	100 μΩ·cm	**115 μΩ·cm**
FMR	640 MHz	1.4GHZ	**1.6GHz**

Higher resistivity CoZrTaB leads to higher frequency response to GHz range

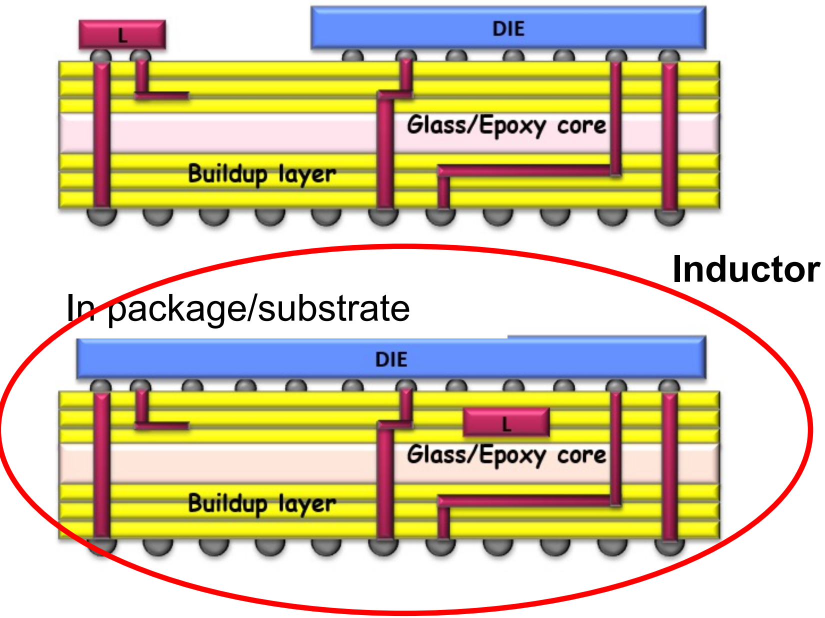


(a)



(b)

On package/substrate



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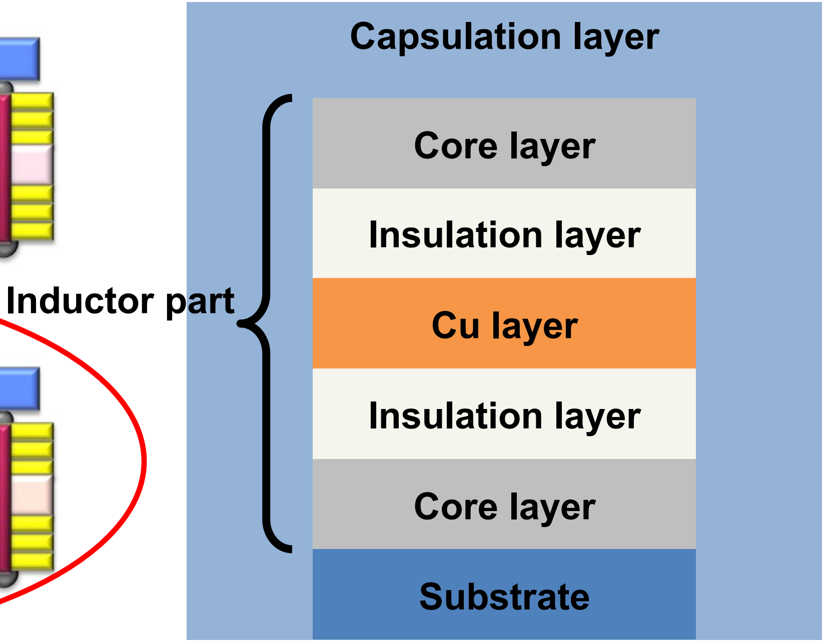
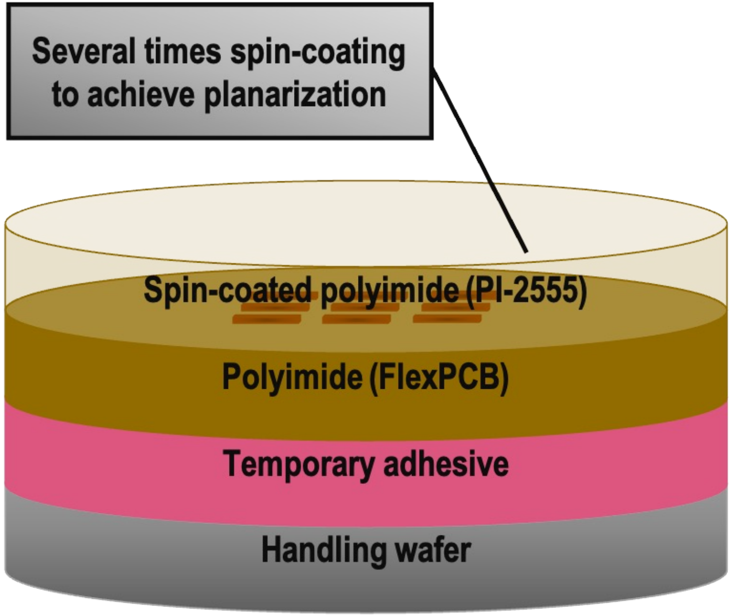


The Schematic of the inductor structure by layers.

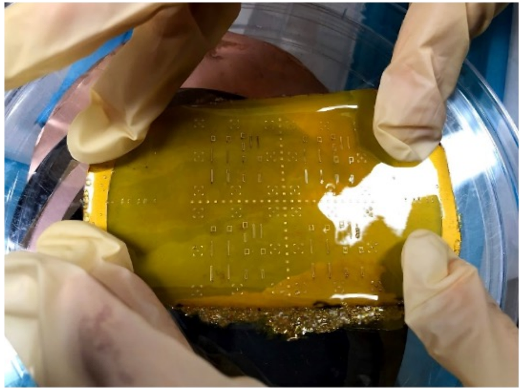
Required process:

- **Lithography**
- **Dry etch**
- **Wet etch**
- **Bonding (alignment)**
- **Spin-coating**
- **Curing**

Cu Pattern Preparations



Schematic of the finished Cu layer of step 2 (Covered with polyimide).

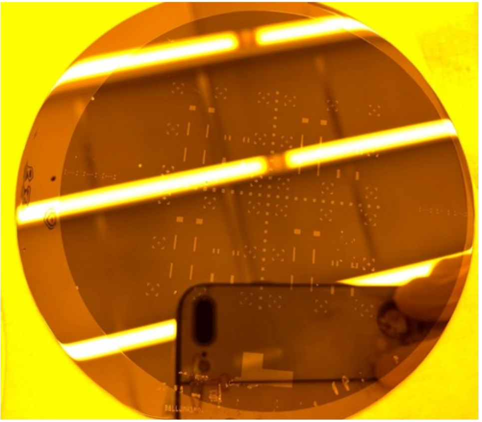


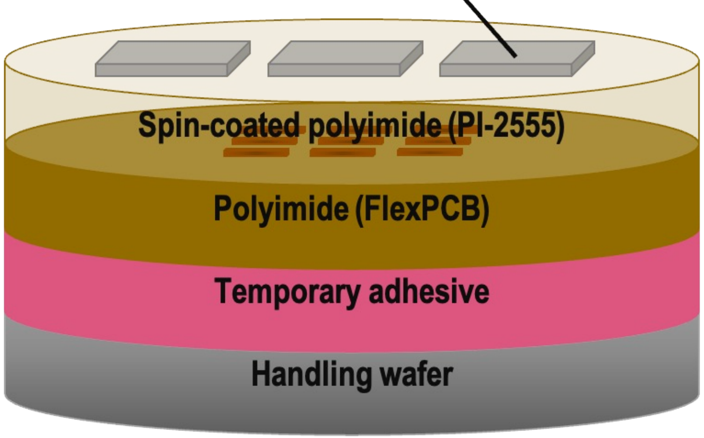
Top view of the finished Cu layer of step 1.

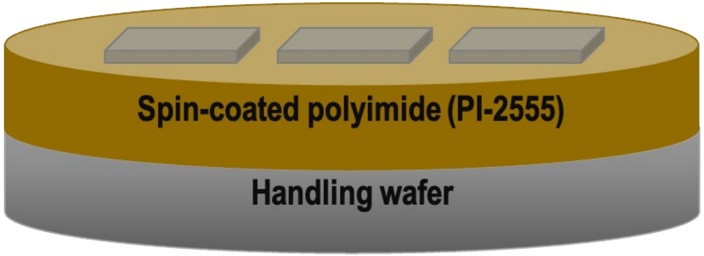
Cu pattern under microscope

Magnetic core Preparations

Photoresist has been patterned for the liftoff (upper layer).

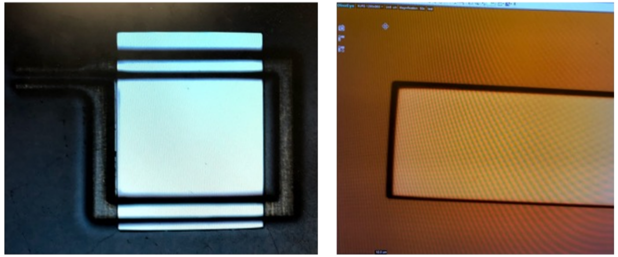




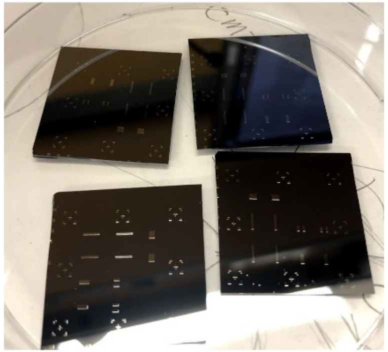


Schematic of the liftoff preparations (upper layer and lower layer).

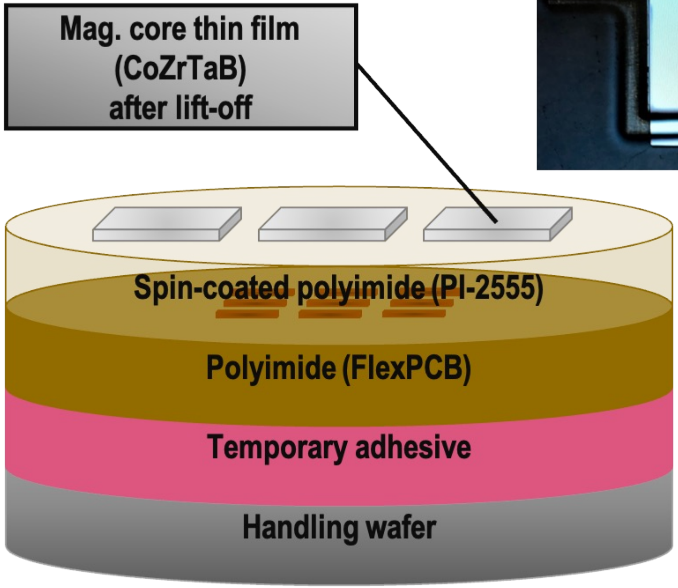
Magnetic core Preparations

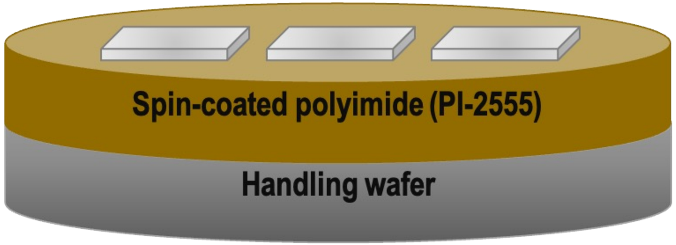


Patterned magnetic thin films under microscope (upper layer and lower layer).



Top view of the magnetic thin films (lower).



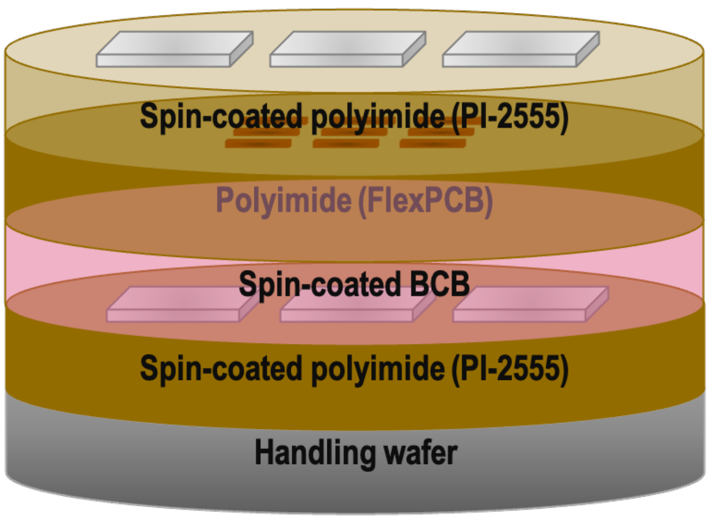


Schematic of the patterned magnetic thin films (upper layer and lower layer).

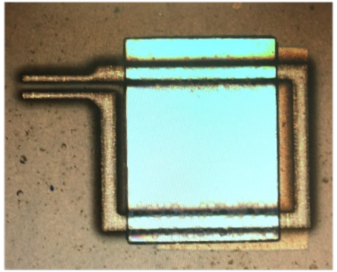
Device Assembly

Flip-chip bonding

One more lithography & dry etch to get the measurement windows

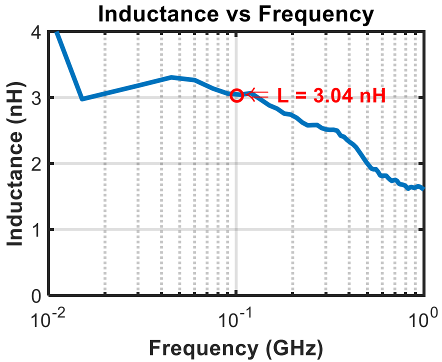


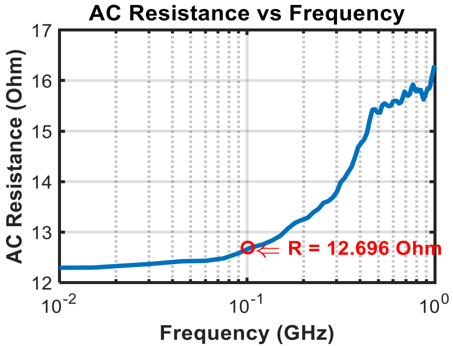
Schematic of the device bonding process (after bonding).



A finished device under microscope.

Measurement Results (Magnetic Core)





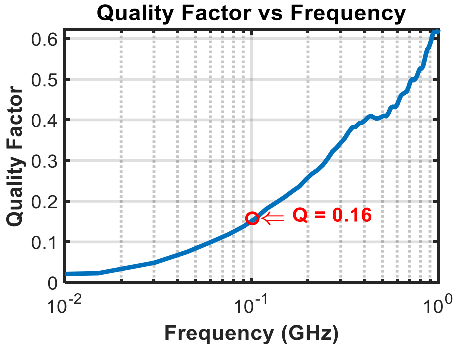


Table5 Design-2 simulation results

	mag.-core	**air.-core**
L (nH)	3.19	2.37
ACR (Ω)	0.203	0.058
Q factor	9.18	25.74

Measurement Results (Air Core)

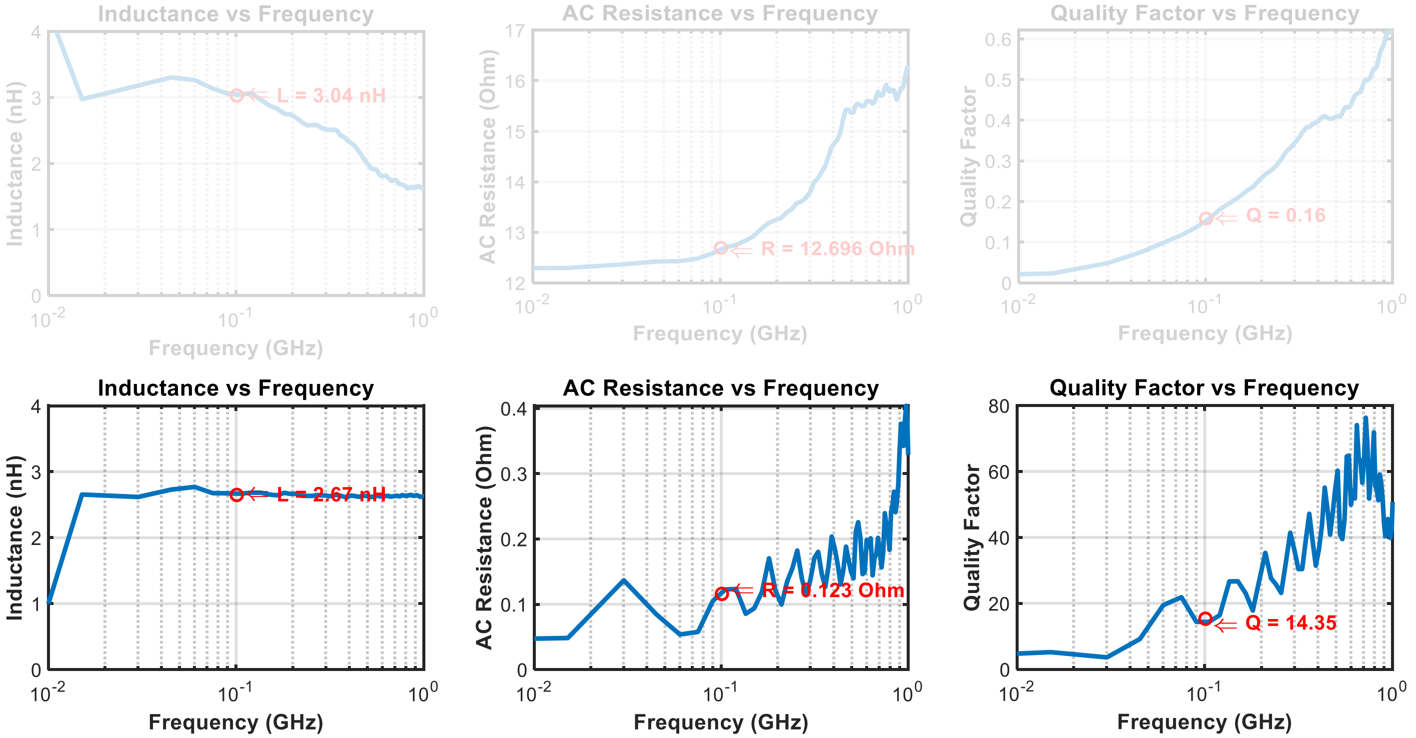


Table5 Design-2 simulation results

	mag.-core	air.-core
L (nH)	3.19	2.37
ACR (Ω)	0.203	0.058
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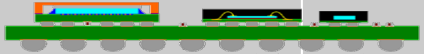
Automotive Processor Roadmap – Infotainment/ ADAS

	Current	5-year	10 year

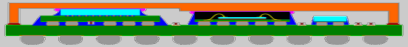

Grade 2, 3 (AEC Q100), fcBGA-H


WB stacked die, Grade 2, 3 (AEC-Q100)


BGA SIP Module, Grade 2, 3


Grade 1 (AEC Q100), fcBGA-H, FC-SIP


fcBGA-H w/ TSI


BGA SIP Module, Mixed Tech


fcBGA-H w/ TSI. Optical IO

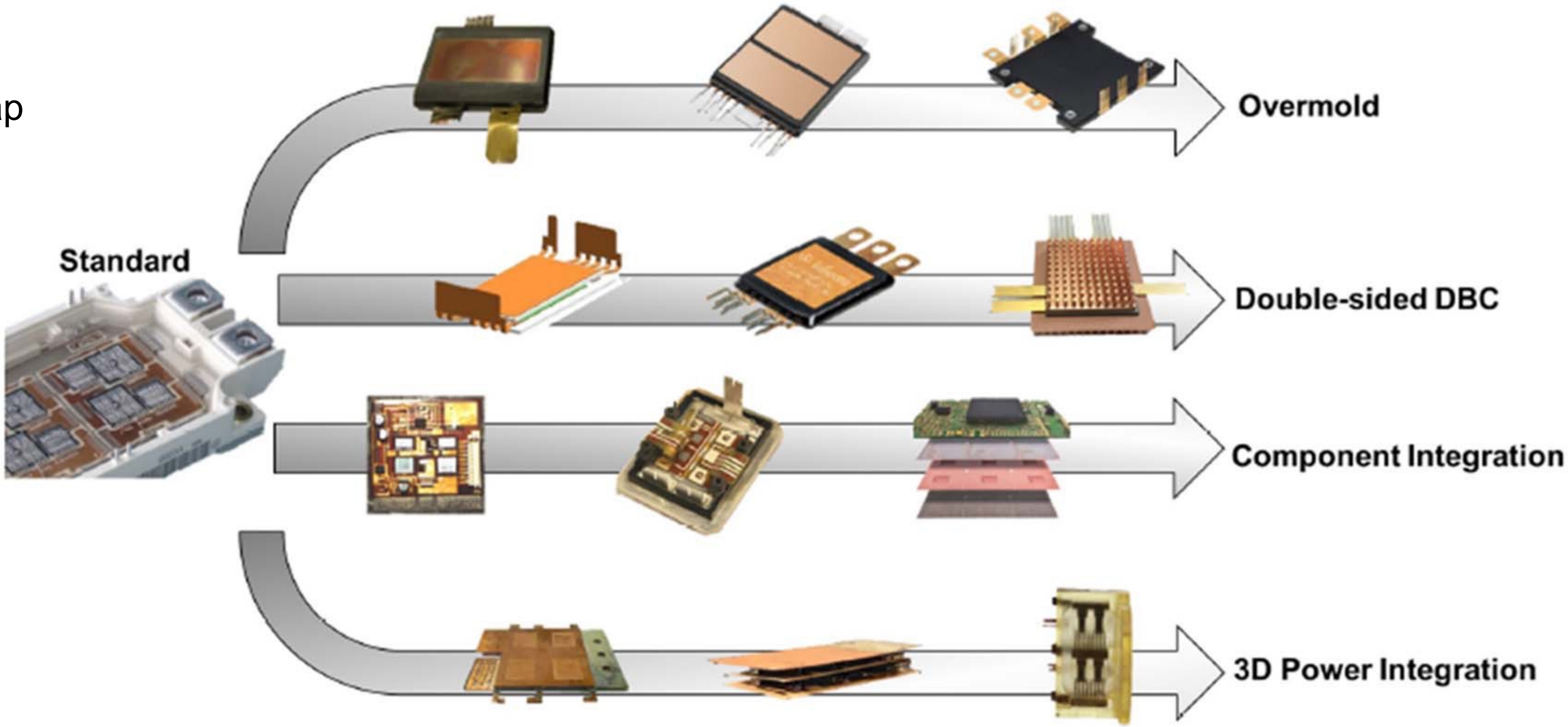
Advanced Si node, increased Graphics and memory BW, Optical IO, Processor Power

Si Node	40nm/28nm/14nm/10nm/7nm		5nm/3nm/2nm
Interface Speed (parallel), opto	High end 128 bit (32bit X 4 channels) →Massive parallelism Mid-end 64 bit (32bit X2 channel)		
Bump pitch	150um/130um/110um		<100um
Mounting structure	PCB Attach		SIP/Module
Reliability	AEC Q100 Grade 3/2/1	AEC Q100 Grade 2/1 AEC Q006 Grade 1	AEC Q100 Grade 1 AEC Q-104 for SIP
Safety	ASIL-B	ASIL-D?	

Chapter 5: Automotive, Heterogenous Integration Roadmap, http://eps.ieee.org/hir

Advances in Package Structures in Power Electronics for Vehicle Electrification

Si IGBT
Wide bandgap devices:
SiC
GaN



Lee, H., J. of Emerging and Selected Topics in Power Elec, 2019.
And Chapter 5: Automotive, Heterogenous Integration Roadmap, http://eps.ieee.org/hir

Conclusion

- Power Delivery driven by high density, efficient, and low cost
- Advances in packaging demand/enable more power delivery innovation
- Magnetic core inductors can be integrated on package or in package
- Different applications have different emphasis, thus implementation: IoT/mobile, HPC, automotive

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