



# Thin-film Magnetics for PwrSoC and Hybrid Integration

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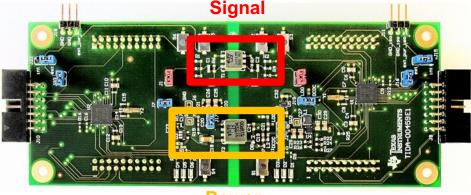
#### Overview

- Introduction
- Thin-film Magnetics technology
- Thin-film Microinductor/-transformer
- Integration Options
- · Reliability
- Outlook & Conclusion

#### Introduction I

- Trend towards miniaturization and higher integration continues
- New inductive components inductors and transformers required suitable for hybrid integration and PwrSoC

application example with discrete magnetic components

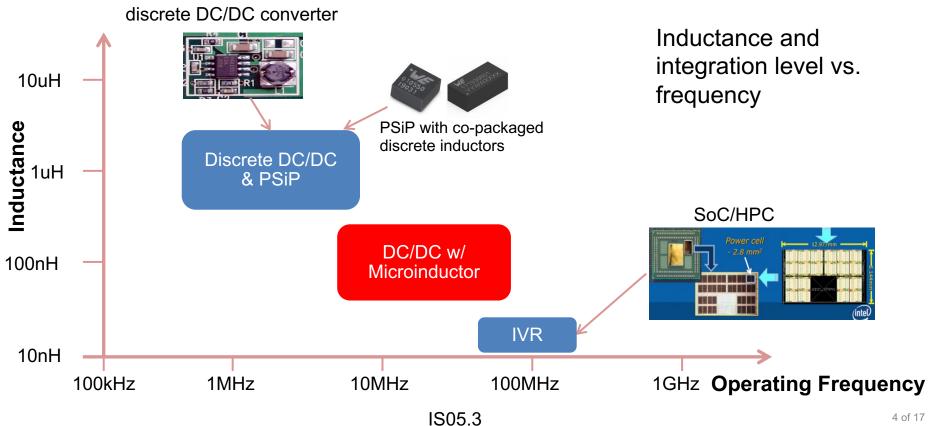


#### Power

Source: TIDA-00459 Highly Efficient Power and Data Transmission Design for Isolated Low Power Applications (Texas Instruments)

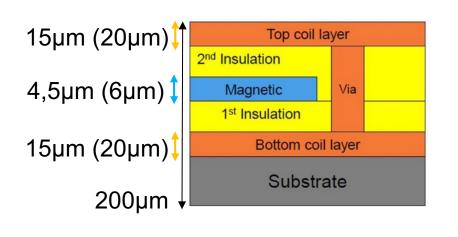
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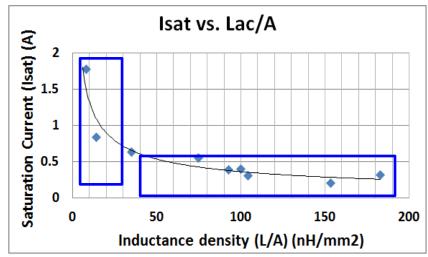
#### Introduction II



### Thin-film Magnetics I

- Thin-film magnetics technology based on silicon substrate for high volume manufacturing on 300mm wafers
- Ultra thin profile height ~200µm
- Polyimide material as insulation between core and Cu layers

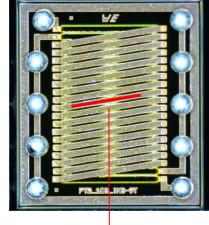


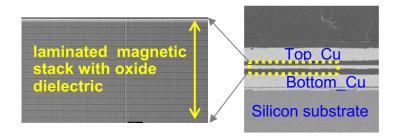


## Thin-film Magnetics II

- Magnetics on Silicon technology:
  - CZT magnetic material for magnetic core
  - Laminated 4,5 or 6µm thick magnetic core
  - 15 or 20µm thick electroplated copper for coil layers







### Thin-film Microinductor I

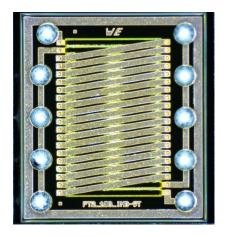
- Microinductor specification range:
  - Inductance range: 5 500nH
  - Inductance density up to 300nH/mm<sup>2</sup>
  - Peak Q-factor 15...20 at ~30MHz
  - L/Rdc > 400nH/ $\Omega$
  - Saturation current 0.2A ~ 2A
  - Inductance tolerance: ±10%



Microinductor

#### Thin-film Microtransformers I

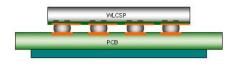
- Microtransformer specification range:
  - Inductance range: 5 500nH
  - Peak Q-factor 12...18 at ~30MHz
  - L/Rdc >200nH/ $\Omega$
  - Isolation voltage up to 3kVrms
  - Coupling coefficient up to 0.95



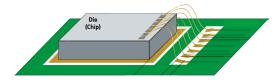
Microtransformer (2.6mm x 2.4mm)

#### Integration options I

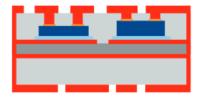
 Various packaging options supported for board level assembly and system-in-package integration



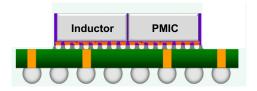
WLCSP for soldering



Bare die for wire bonding interconnects



Bare die for embedding

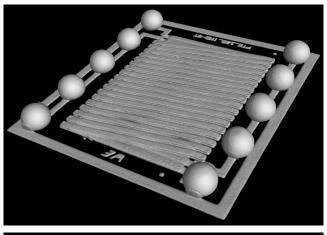


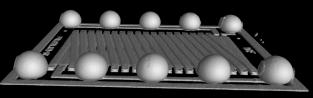
Chiplet integration

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#### Integration options II

- chip height ~ 200µm
- Ball diameter 225µm
- Device height soldered on PCB ~300µm
- Smaller ball diameters possible

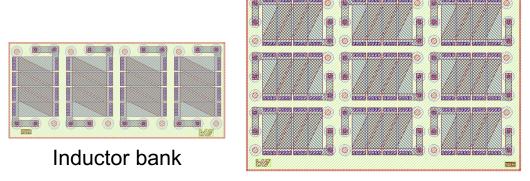




WLCSP packaged discrete magnetic component

#### Integration options III

 Integration of multiple inductors on the same die is possible, optionally with different L values



Inductor array

#### Reliability

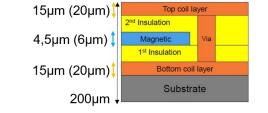
 Reliability proven by AEC-Q200 grade 1 qualification of WLCSP packaged inductor and transformer

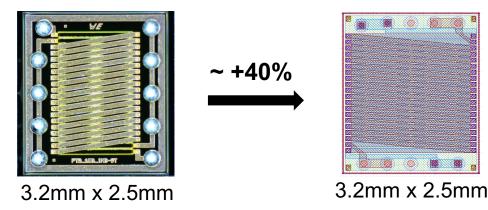
	w/E	Qualific	ation AEC-Q	200 REV D Table5 Test Overvie	w				
	Product Series		WE-MINT (Magnetic Integrated Nano Transformer) WE-MINI (Magnetic Integrated Nano Inductor)						
			Acce	eptance Criteria					
#1		No physical damage and electrical property (Ls, RUC) meets datasheet both premeasurement and postmeasurement							
#2		Inspect device construction, marking and workmanship. Electrical test not required.							
#3		Electrical test not required. Dimension meets datasheet.							
	#4	Marking mus	ing must remain legible.						
	#5	#5 Acceptability of Electronic Assemblies IPC-A-610 class 3.							
	#6	Push off sam	ple from PCB and force	needs to be recorded.					
No.	Test item	Sample Size	Reference	Test conditions	Acceptance Criteria				
3	High Temperature Exposure	77	MIL-STD-202-108	125°C, 1000h	#1				
4	Temperature Cycling	77	JESD22 Method JA-104	-40°C.(30min)~ 125°C.(30min), Transfer time max. 1min., 1000 cycles	#1				
7	Biased Humidity	77	MIL-STD-202-103	85°C, 85%RH, 1000h	#1				
8	Operational Life	77	MIL-PRF-27	85°C. – 40°C Temperature rise, 1000h, rated current from the datasheet	#1				
9	External Visual	30	MIL-STD-883-2009	N/A	#2				

10	Physical Dimension	30	JESD22 Method JB-100	N/A		#3
	Resistance to Solvents	5	MIL-STD-202-215	Solvent 1: Immersion for 3+0.5, -0 minutes @ 25±5°C,brush 10 strokes (wet bristle),hand pressure 2~3 ounce for 3 cycles with air-blown dry		
12		5		Solvent 3: Immersion for 3+0.5, -0 minutes @ 25±5°C,brush 10 strokes (wet bristle),hand pressure 2~3 ounce for 3 cycles with rinse in approximately 25°C water and air-blown dry		#4
		5		Solvent 4: Immersion for 3+0.5, -0 minutes @ 63°C-70°C,brush 10 strokes (wet bristle),hand pressure 2~3 ounce for 3 cycles with rinse in approximately 25°C water and air-blown dry		
13	Mechanical Shock	30	MIL-STD-202-213	3 shocks in each direction(x, -x, y, -y, z, -z) , peak value 100g's, duration 6ms, half-sine, velocity change 12.3ft/sec.		#1
14	Vibration	30	MIL-STD-202-204	10g's for 20min, 12cycles each of 3 orientations, test from15~2000HZ		#1
15	Resistance to Soldering Heat	30	J-STD-020	Tp, tp=30~35s, 3 times reflow		#1
17	ESD	15	AEC-Q200-002 or ISO/DIS10605	Test Environme Size Micro Ind Micro Trafo	nt: 22°C ± 5°C, Humidity: 30% ~ 60% Component Classification 2 (200V DC to <4000V DC) 2 (200V DC to <4000V DC)	#1
18	Solderability(SMD)	30	IPC-A-610	Steam Aging 8 hrs±15min @93°C, Tc=240~245°C,tp=20~30s.		#5
19	Electrical Characterization	30	User Spec.	measure electrical property@ 20°C, 125°C, -40°C		#1
21	Board Flex	30	AEC-Q200-005	bending 2mm (Min), 60(+5) sec		#1
22	Terminal Strength(SMD)	30	AEC-Q200-006	Product Type Micro Ind Micro Trafo	Push Off Force(N) 17,7N 17,7N	#6
*N/A	Low Temperature Storage Life	77	JESD22-A119	-40°C., 1000h		#1

# **Outlook – Technology Enhancements**

- AEC-Q200 grade 0 qualification
- Increased Cu layer thickness:  $15\mu m \rightarrow 20\mu m$
- Increased core layer thickness:  $4.5\mu m \rightarrow 6\mu m$
- Increased active area

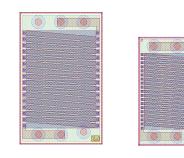




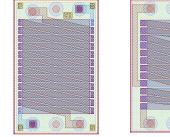
#### **Outlook – Microinductors /-transformers**



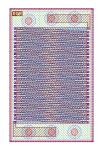
Inductor for IVR



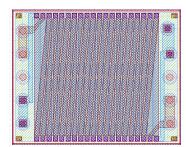
Inductor for PoL DC/DC



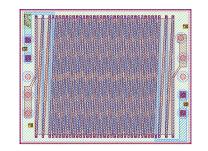
Coupled inductors for PoL DC/DC



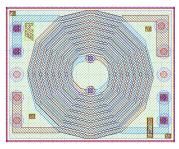
Signal inductor



Transformer for isolated DC/DC

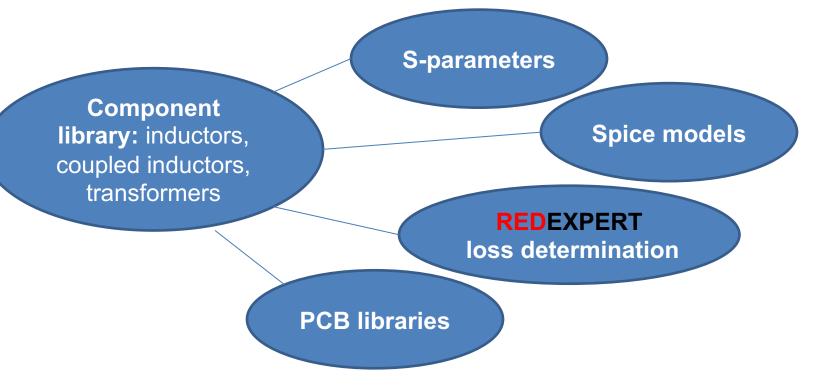


**Pulse transformer** 



**Spiral transformer** 

#### Outlook – Design enablement



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#### Conclusion

- Thin-film magnetics (microtransformer and -inductor) in WLCSP package AEC-Q200 qualified
- Various packaging options support hybrid integration
- Improved performance expected from enhanced layer stack
- Various microinductor and –transformer designs available for sampling



#### Thanks for your attention! martin.haug@we-online.de

