Industry Session 05: PwrSoC for Next-Gen Power

Integrated Capacitors and Energy Storage Devices for PwrSoC: Trends and challenges

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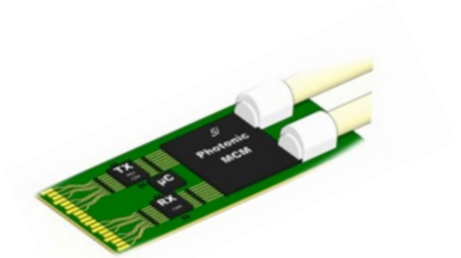
Outline

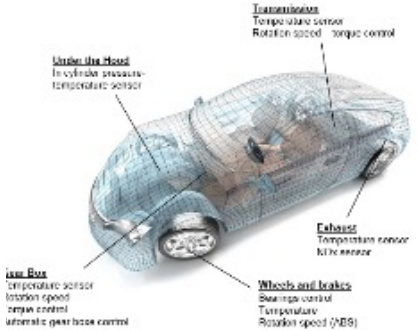
1- Introduction

2- Silicon Capacitors technology

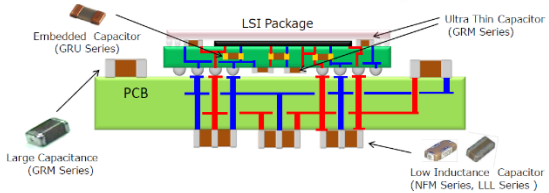
3- 3D Silicon capacitors for power applications

- 3.1- Automotive
- 3.2- Optical transceivers
- 3.3- Mobile & HPC

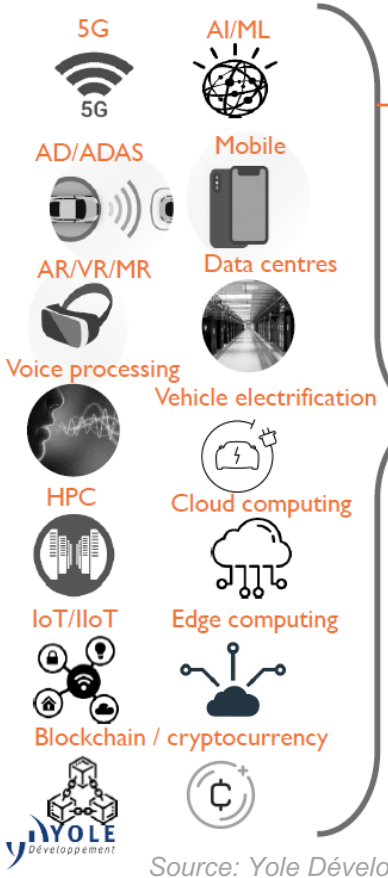




4- Conclusion



1- New Trends & Drivers



System requirement

- More computing power
- High speed
- More bandwidth
- Low latency
- Low power
- More functionality
- System integration
- More sensors
- More memory
- Low cost
- Hardware-software compatibility

Opportunity for various devices

Megatrends create business for variety of ICs from high end xPUs to low end discretes

- CPUs, GPUs, SoCs, APUs, FPGAs
- ASICS, DSPs, MCUs
- MEMS/Sensors
- Power ICs/discretes
- Memories
- Optoelectronics

Opportunity for fab/front end

Front end scaling slowdown but continues: Moore's Law keep going but at smaller pace => high end fab business keep growing (5nm & below)

More & more heterogeneous integration to support functionality, faster time to market and low cost : More than Moore's => Resurgence of legacy fabs => Increasing business

8" wafer fabs and related tools demand to remain strong

Require new technology / innovations: Front end design / manufacturing innovations: from von Neuman to neuromorphic computing architecture; new processes: beyond FinFet, nanowires FET, vertical NAND etc; require EUV and new deposition/etching technologies; new interconnect materials, dielectrics etc.

Opportunity for semiconductor packaging

Create business opportunity for both advanced and traditional packaging platforms

Advanced packaging (WLPs, flip-chip, TSV) business opportunity supported by AI/ML, Mobile, AR/VR, 5G, smart automotive

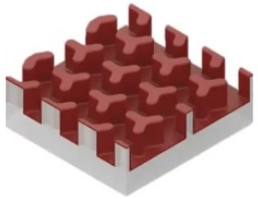
Traditional packaging (wire-bond lead frame based) business opportunity created by IoTs, Industry 4.0, smart automotive

Mega trends like mobile, automotive, IoTs, industry 4.0, require variety of MEMS sensors that create opportunity for both traditional & advanced packaging

Require Back end and assembly innovations: panel level packaging, high accuracy bonders, TCB, CtW/WtW bonding, photonics integration in package. As for materials, there is a desire to develop new dielectric materials, mold compounds, underfill, solder interconnects, and TIMs for fulfilling the stringent performance and reliability requirements demanded by next-generation hardware.

Source: Yole Développement

2- Silicon Capacitors extending MLCC portfolio



Classical 2D capacitor : Capacitance value depends on electrode surface

3D structures enable a higher density

2D structure

Electrode

Dielectric

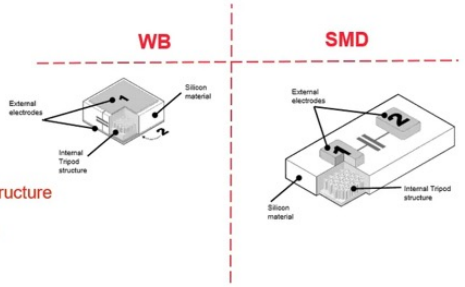
No Trench

First cylindrical structure

Tripod structure

$$C = \varepsilon_0 \varepsilon_r \frac{S}{d} N$$

C : Capacitance
S : Area of the two electrodes
d : Separation between electrodes
ε_0: Electric constant
ε_r: Dielectric constant
N : Stack number



High stability in temperature
Up to **250°C** environments

Signal stability over frequency
Up to **110 GHz** applications

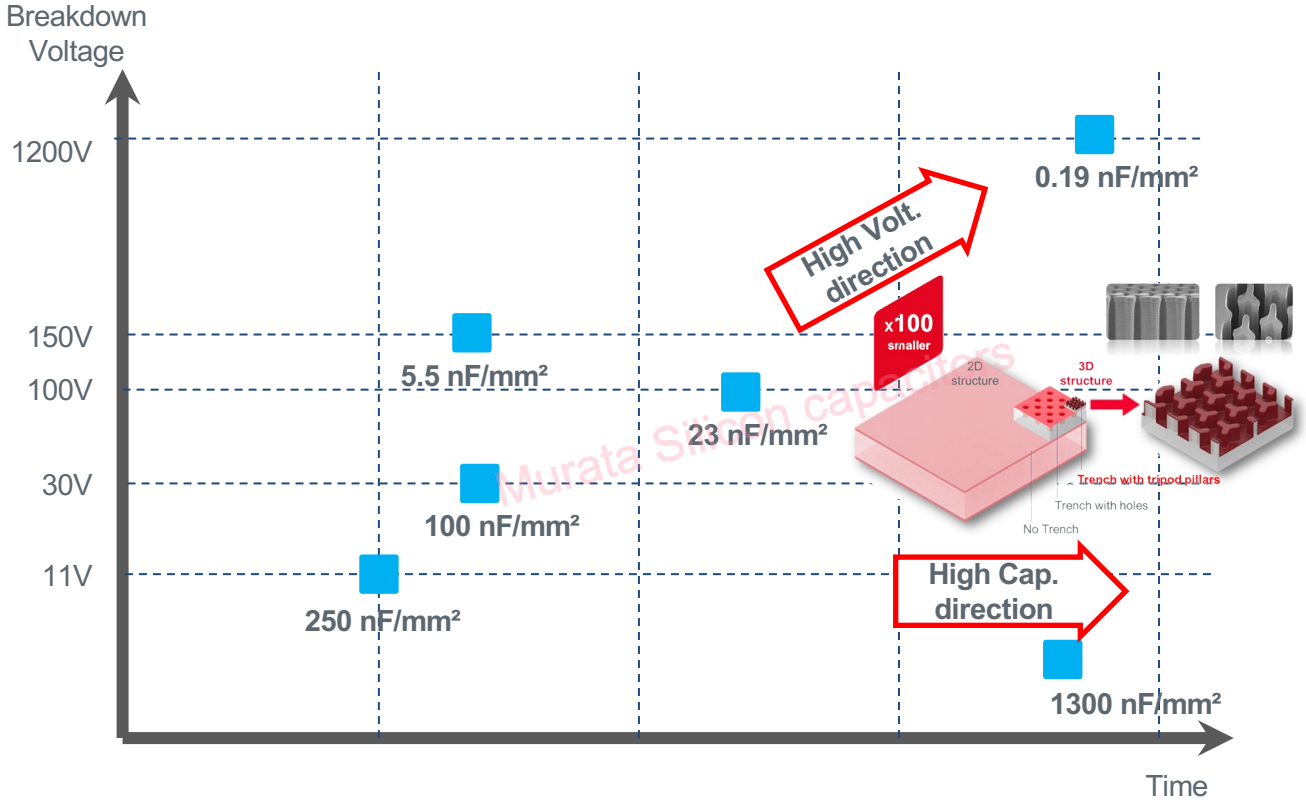
Stability regarding voltage
For **450 V** applications

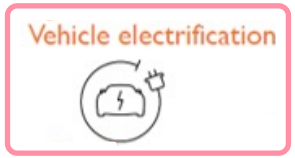
Stability over ageing
Minimum lifetime of **10 years**

Extreme low thickness
Down to less than **50 µm**

High Density | Low ESL | Low ESR | Low profile | Mechanical strength

2- Silicon Capacitor - Technology Road Map

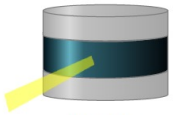




- Murata is committed to a vision of developing innovative integrated Silicon capacitors to match the requirements and trends of SOC

3.1- LiDAR Applications_Si-cap benefits

Vehicle electrification

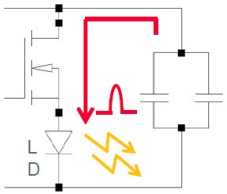


LiDAR

Longer sensing distance is required

Needs Trend

- Higher peak & Shorter pulse width
- Stability of pulse
- High reliability



Discharged pulse from capacitors flow LD and generate laser pulse

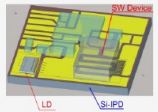
Needs Trend for discharge capacitor

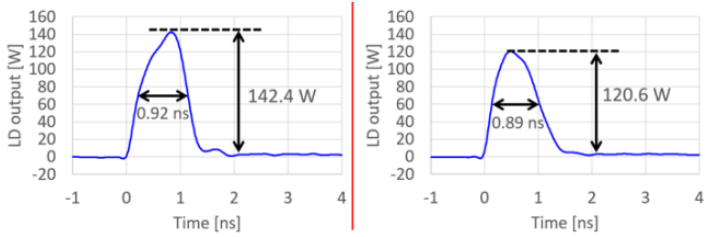
- Low ESL design
- Stability of Capacitance
- AEC-Q100

Si-cap Wire bondable

0202 size, 1nF(BV150)
0302 size, 470pF(BV450)

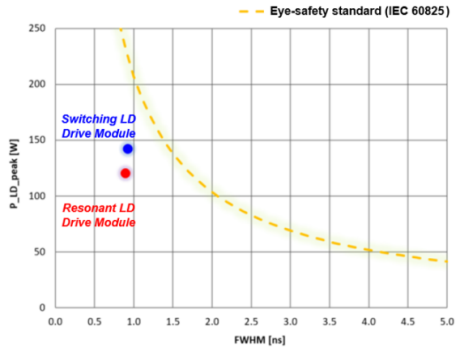
Si-interposer



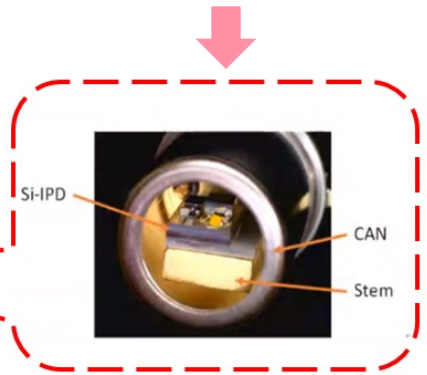


(a) Switching LD driver module

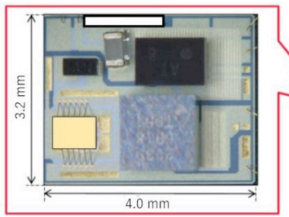
(b) Resonant LD driver module



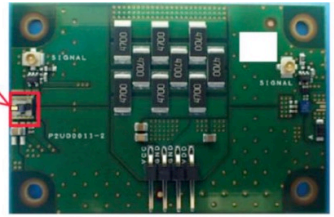
Extreme Miniaturization



Presented @ APEC 2021



Si-IPD



PCB

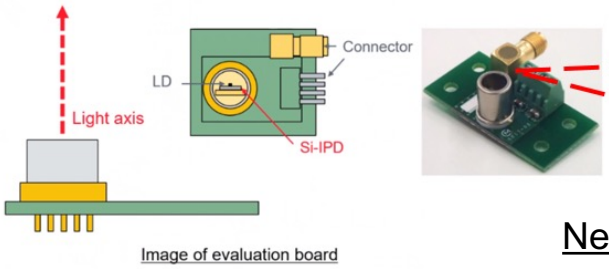


Image of evaluation board

New evaluation board available

3.1- WBG power switching challenges

Vehicle electrification

Market trend

High power density / integration density / efficiency

High temp. operation

High speed switching by using SiC / GaN

High frequency noise

Lifetime & Reliability
- parasistic L on DC bus
- SW junction recovery (IGBT, SiC, GAN …)

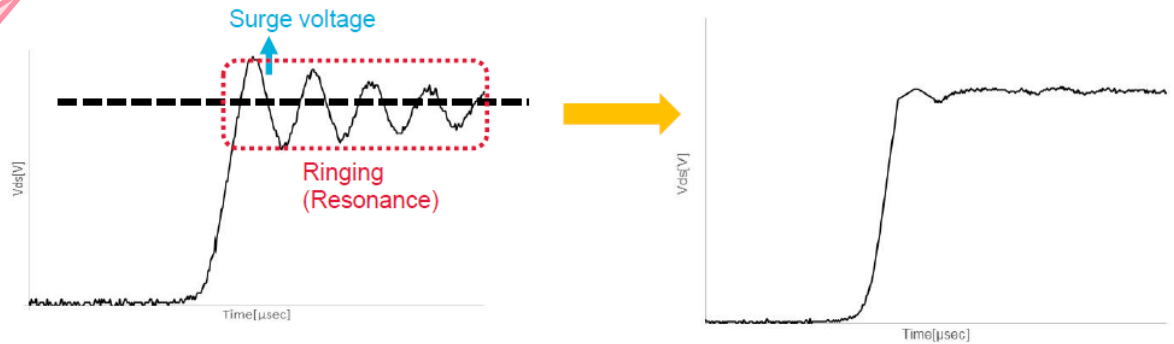
EMI
- complex resonnance of parasitic L and C

Challenge for high speed switching

Parasitic inductance in the circuit cause
1. Surge voltage
2. Ringing

Capacitor Optimization

Damping surges and lowering ringing frequencies

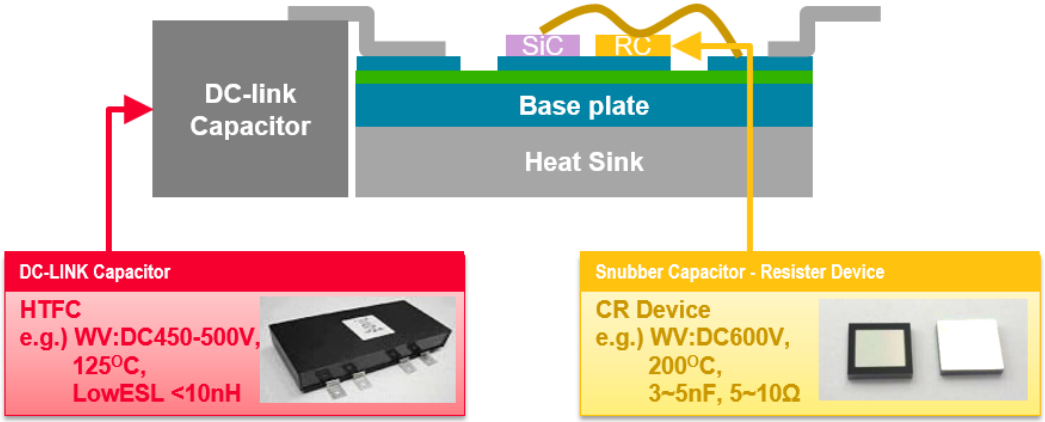


Integration of low ESL components and innovative packaging → Built-in snubber solution for power module

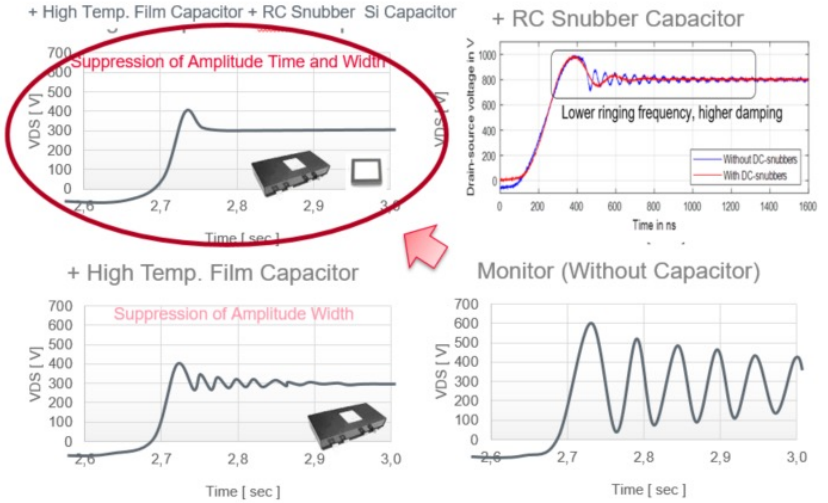
3.1- Synergy with Murata Film capacitor

Vehicle electrification

Since it's very important to design both snubber capacitor and DC-link capacitor together to reduce surge voltage and ringing.
Murata can propose the best solution considered combination of snubber capacitor and DC-link capacitor. HTFC is for DC-link and Si-cap is for snubber.



Expected Improvement by New Solutions



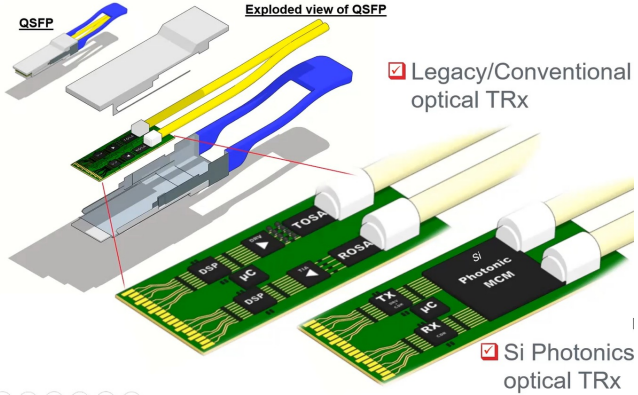
1.High temp. operation (200℃)
Put Si-RC device close to SiC/GaN which operates under high temp.

2. Same mounting method as power device
Ex) Top→ Wire bonding
Bottom→ Soldering and Sintering

3. Function of CR device as 1 chip
Realize downsizing of power module by saving space.
(If you used other capacitors, both capacitors and resistor must be used.)

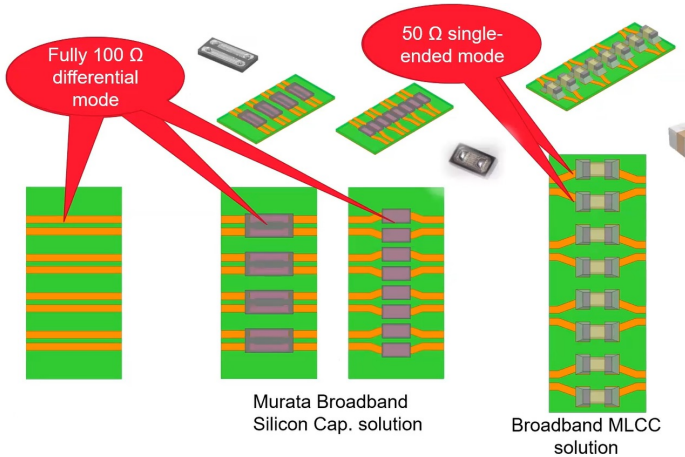
3.2- Optical Transceivers

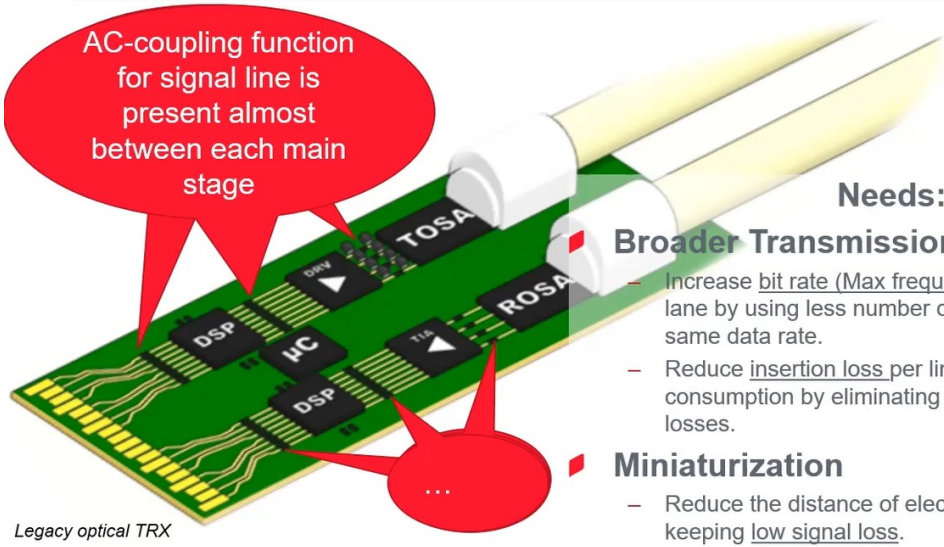
Data centres



☑ Legacy/Conventional optical TRx

☑ Si Photonics optical TRx

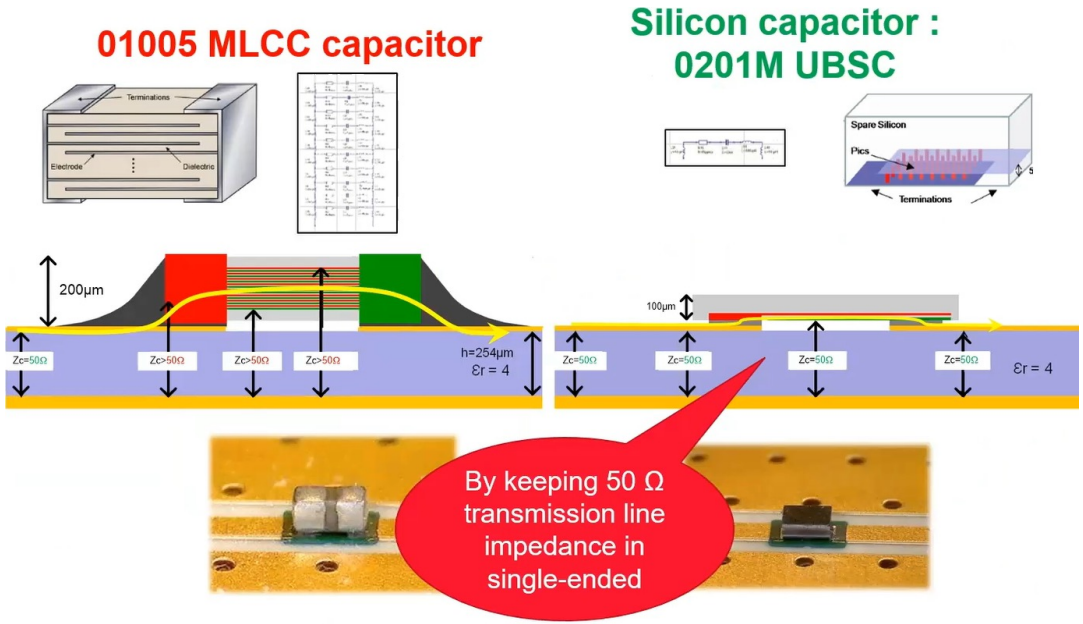




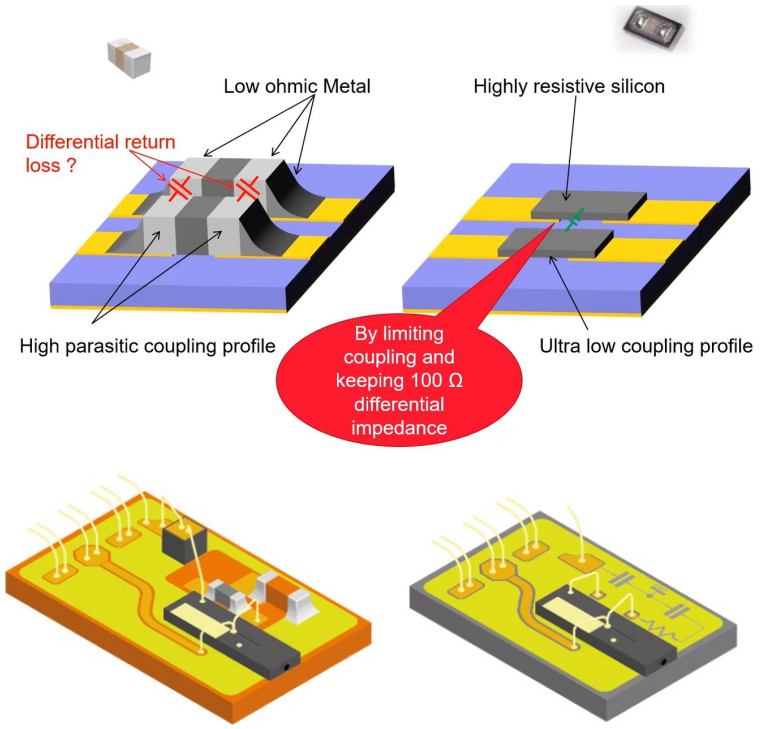
Needs:

- **Broader Transmission line**
  - Increase bit rate (Max frequency) per electrical lane by using less number of TRx and keeping the same data rate.
  - Reduce insertion loss per line to minimize current consumption by eliminating unnecessary signal losses.
- **Miniaturization**
  - Reduce the distance of electrical lane (pitch) by keeping low signal loss.
  - Improve the SNR by rejecting noise and by keeping full differential transmission mode.
- **Standardization**
  - Support long and short distance with same TRx type (with high Rx sensitivity and High Tx swing).

3.2- Optical Transceivers

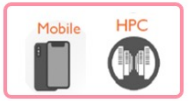


No signal integrity degradation



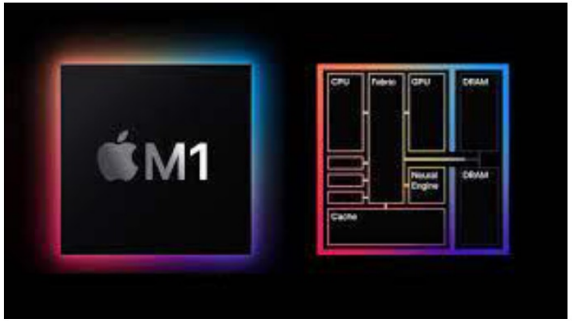
Further integration with Si-IPD

3.3- PDN Applications

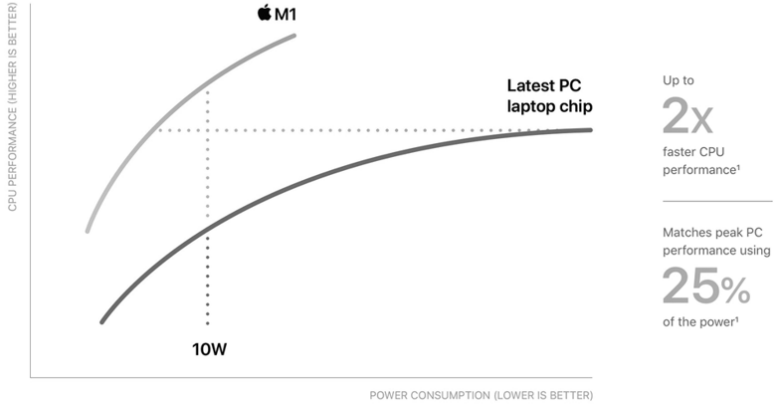


Macbook Pro 2020

M1 Chip

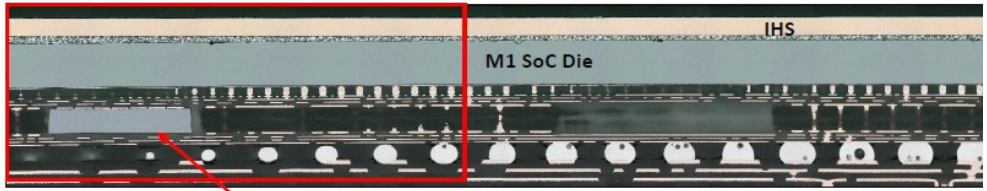


CPU performance vs. power



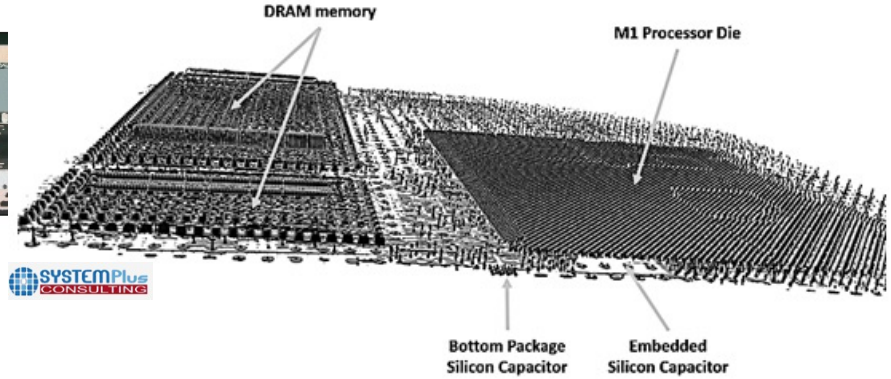
Source: https://www.apple.com/fr/newsroom/2020/11/apple-unleashes-m1/

4 Land Side + 6 Embedded Silicon capacitors



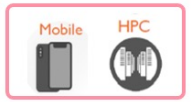
M1 SoC Package Cross Section 1
©2021 by System Plus Consulting

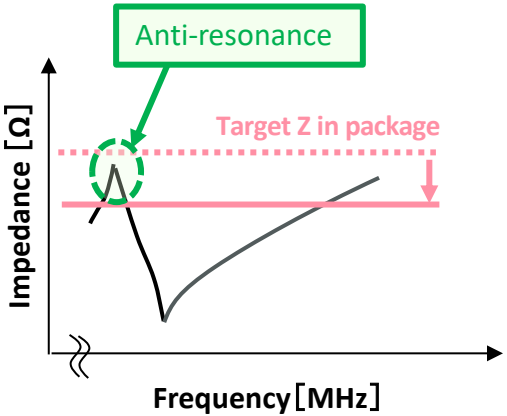
Embedded Silicon capacitor

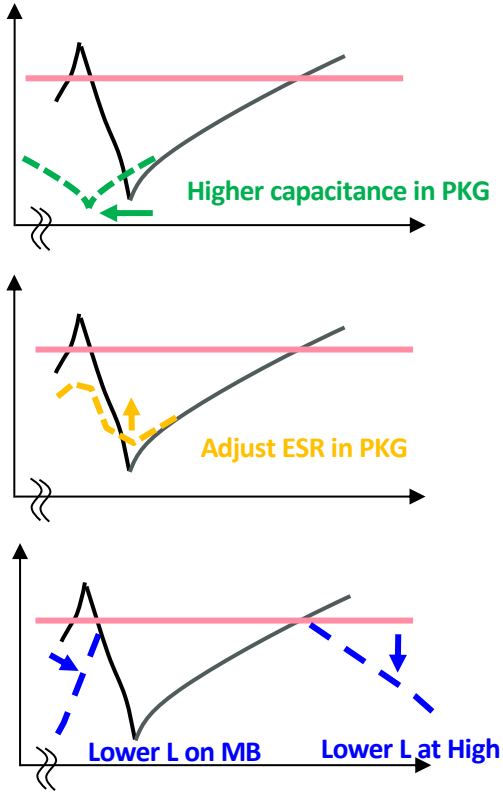


Source: SystemPlus consulting

3.3- Lower PDN impedance



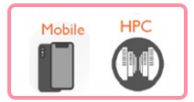


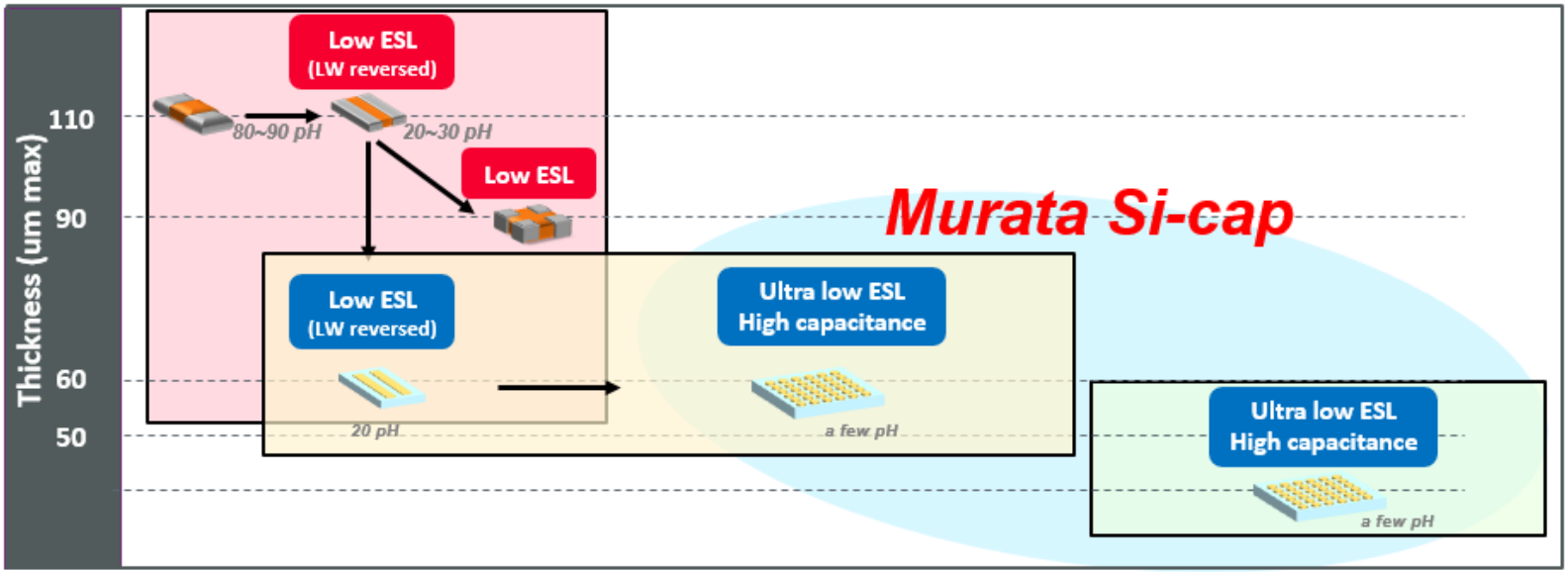


Solution for low Z for anti-resonance

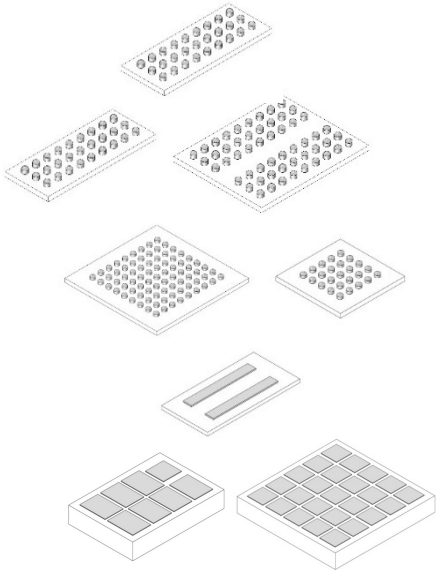
→ ① **Higher capacitance in PKG**
→ ② **Adjust ESR of Capacitor**
→ ③ **Lower L on MB and high frequency**

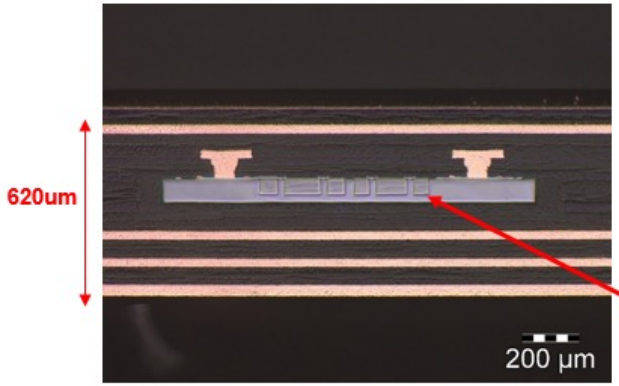
3.3- Increased Interest in Si-Caps is Driven by ..



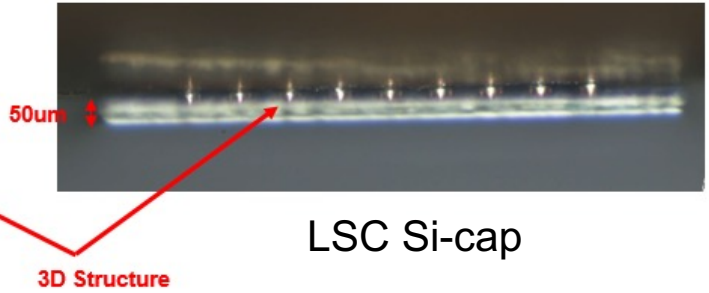


3.3- Murata's innovative solutions





Embedded Si-cap

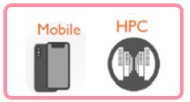


LSC Si-cap

Ultra Low ESL Silicon capacitor with:

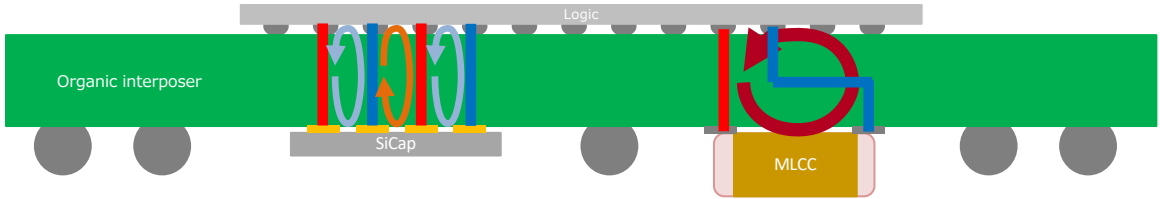
- **World record of 1300 nF/mm²** in Silicon, 1 µF in ultra compact 0404 form factor
- Ultra-low ESL (< 5 pH) and ESR (< 10 mΩ)
- <50 µm thickness
- Mechanical robustness of silicon during assembly

3.3- Landside benefits



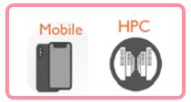
Si-Caps help reducing ESL

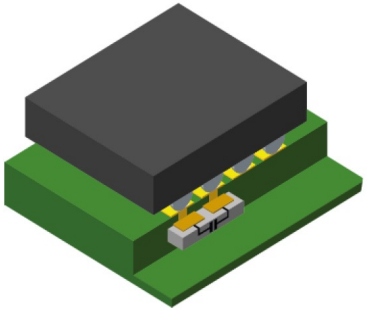
- Si-Caps intrinsic ESL is lower than MLCC
- Assembly ESL is reduced
  - Multi-terminals generate smaller current loop ➔ lower ESL (shorter distance between pads)



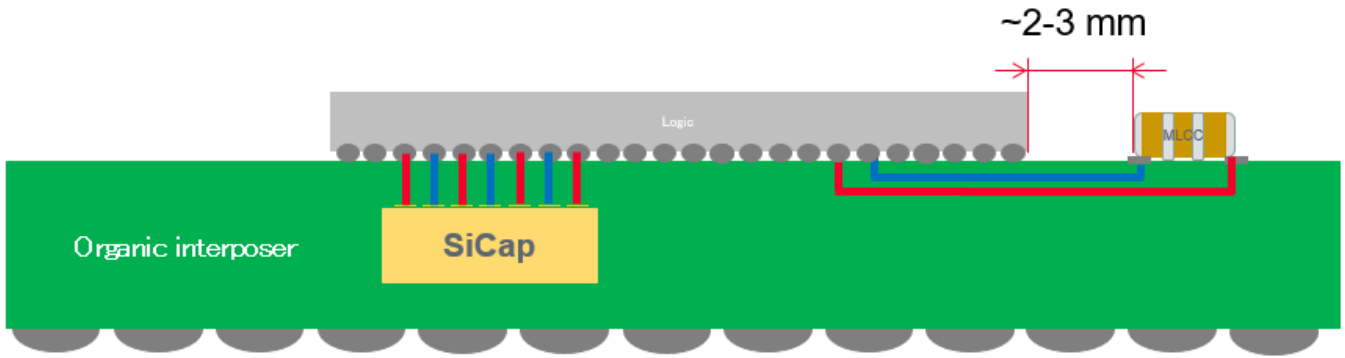
  - Low-profile enables integration closer to IC

3.3- Embedded benefits





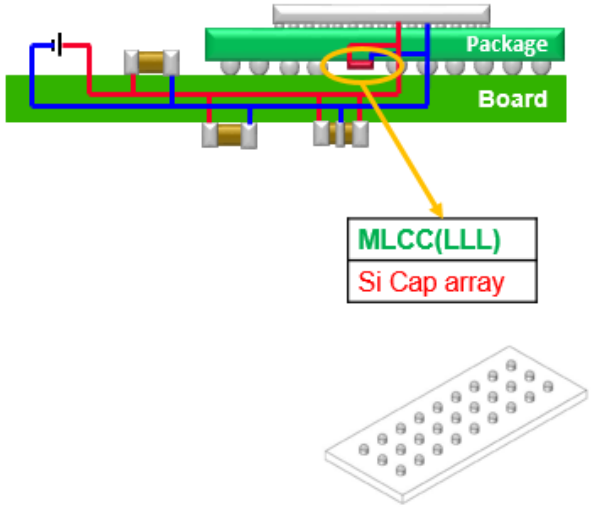
Source: N. Normand [IMAPS 2021]

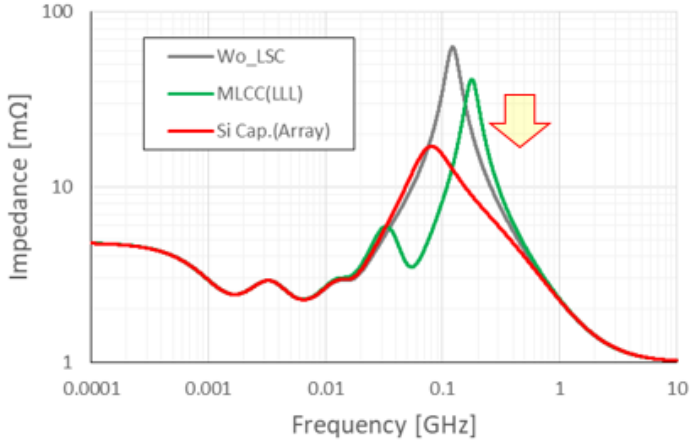


Decoupling cap	Parasitic from assembly	Cap intrinsic ESL	Conclusion
MLCC die-side	**High ESL** high distance - Underfill	**High ESL**	**Standard**
SiCap embedded	**Low ESL** close to IC	**Low ESL** Multi-terminals Adjacent opposite loops	**Improvement**

+ Ability to reduce substrate X/Y size

3.3- Si-caps improve system performance



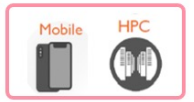


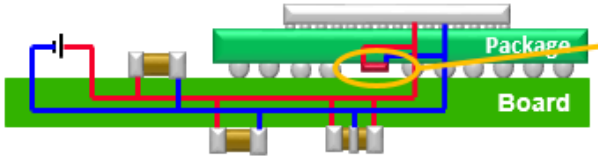
	Z_{peak} (mΩ)
Wo LSC	62.7
MLCC(LLL)	41.2
Si Cap.(Array)	17.0

-24.2 mΩ

- Abrupt changes in processor activity induce large current transients in the power delivery network
- There is a need to reduce losses → provide better and more granular regulation to the processor cores

3.3- Si-caps improve system performance

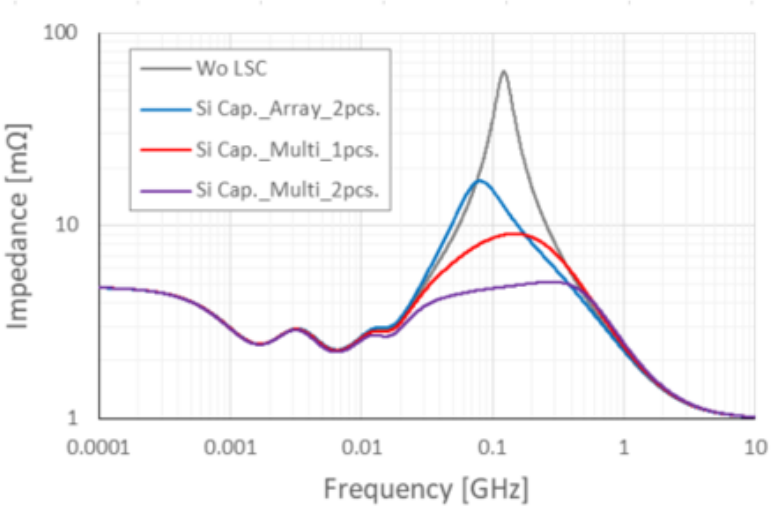




0404 Multi-term

Cap Array

Z_{peak} : anti-resonance between Chip and Board



	Z_{peak} (mΩ)	Improvement rate (%)
Wo LSC	62.3	
Si Cap. ×2 pcs.	17.0	-72.7%
Si Cap. ×1pcs.	9.1	-85.4%
Si Cap. ×2pcs.	5.1	-91.8%

＊Wo LSC = Without Land Side Capacitor
＊In the case, we connect Si Cap.(Array) to same power line

・Z_{peak} is reduced by mounting LSC.

4. Conclusion

- Miniaturization enables new markets and applications
- Si-cap use from niche market/application to wider usage
- Solutions that both increase the performance and reduce the power consumption
  - **Automotive:**
    - High voltage, low ESL loop, Thermal stability
    - Silicon capacitive interposer presents innovative solution from electrical and assembly point of view
    - Challenges: automotive reliability standard (AEC-Q100) and Eye safety (IEC 60825)
  - **DataCenter:**
    - Increased bit rate and reduced insertion loss
    - Improved SNR
  - **Mobile & HPC:**
    - Requirements in terms of high density, low profile and low ESL
    - Silicon capacitors flexibility: process, materials, design, interconnects and assembly

Thanks a lot for your time and attention!

Any questions and/or comments?