APEC - PSMA Industry Sessions MPS and EPC Drive Efficiency and Power Density in 48V Datacenters

EPC eGaN™ enables MPS high power density fixed ratio Intermediate Bus Converters

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The Demand for More Power

As demand for cloud computing, AI applications, and high-power processors/accelerators grows datacenters are evolving to accommodate new high-power requirements.

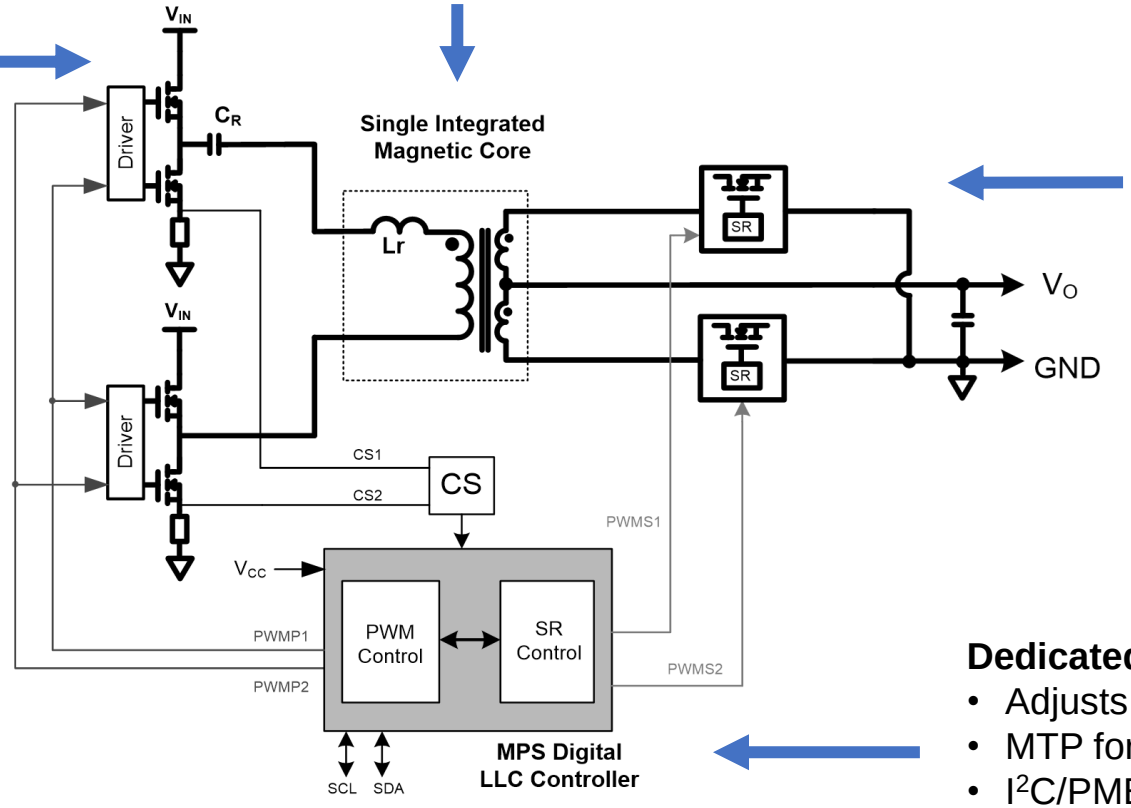
Problem		***Solution***		***Challenge***
12V legacy power distribution too lossy for new current requirements (I^2R)	→	Migrate to 48V datacenter, $1/16^{th}$ distribution loss	→	$R_{DS(ON)}$ of FETs non-linear with V_{IN}. Similar $R_{DS(ON)}$ leads to much larger FET capacitance & switching loss

Power providers *must* adopt new technologies to improve efficiency and provide more power in the same form-factor.

MPS Design Principles

Planar Transformer
- Excellent Heat Dissipation for high-efficiency & density
- Low-height, easy to fit into existing server form-factor

Primary-side GaN FET
- Improved FOM for $R_{DS(on)}$*Q_G
- Smaller FET sizes for better form-factor



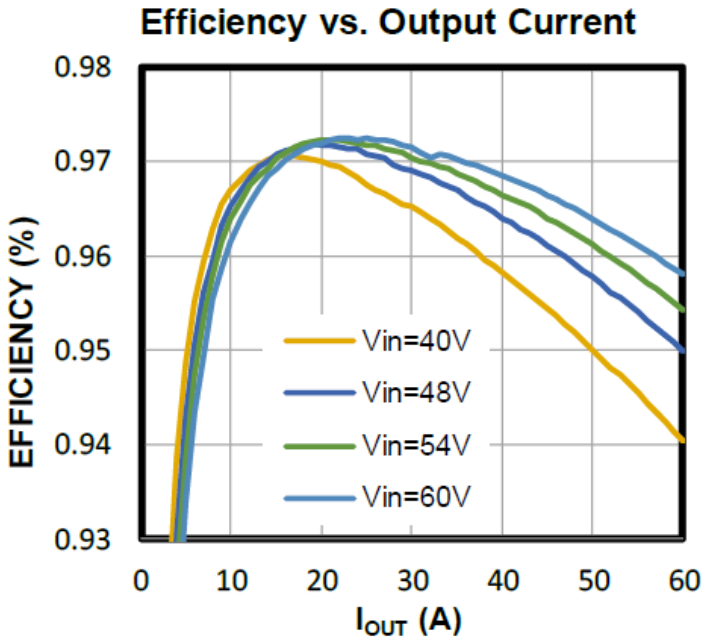
Synchronous Rectifier
- Accusense™ current sensing for accurate sensing (+/-2%) without significant loss from sense resistor or passive network
- Designed as counterpart to controller for optimized control & telemetry

Primary & Secondary-side FETs
- Significant decrease of start-up stress by MP2981 soft-start control. Can power-on under severe conditions

Dedicated LLC Controller
- Adjusts Frequency for Best Efficiency
- MTP for fine-tune control
- I^2C/PMBus for fault and performance monitoring

MPS 10:1 IBC – MPC1100A

Specifications	Min	Typ	Max	Units
Vin	40	54	60	Volts
Vout		5.4		Volts
Pout		300		Watt
Size(X & Y)		18 x 27		mm
Total Thickness		6.1		mm



Benefits:

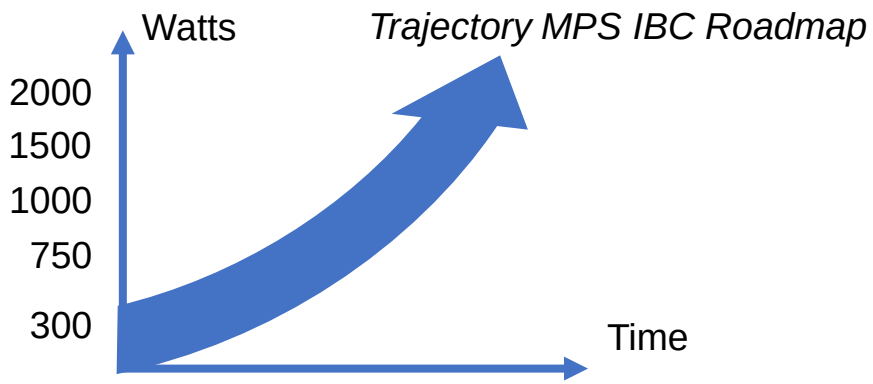
1. Common Footprint
2. Soft-switching for all FETs
3. OVP/UVP/OCP/OTP
4. PMBus/I^{2}C Compatible
5. Programmable soft-start

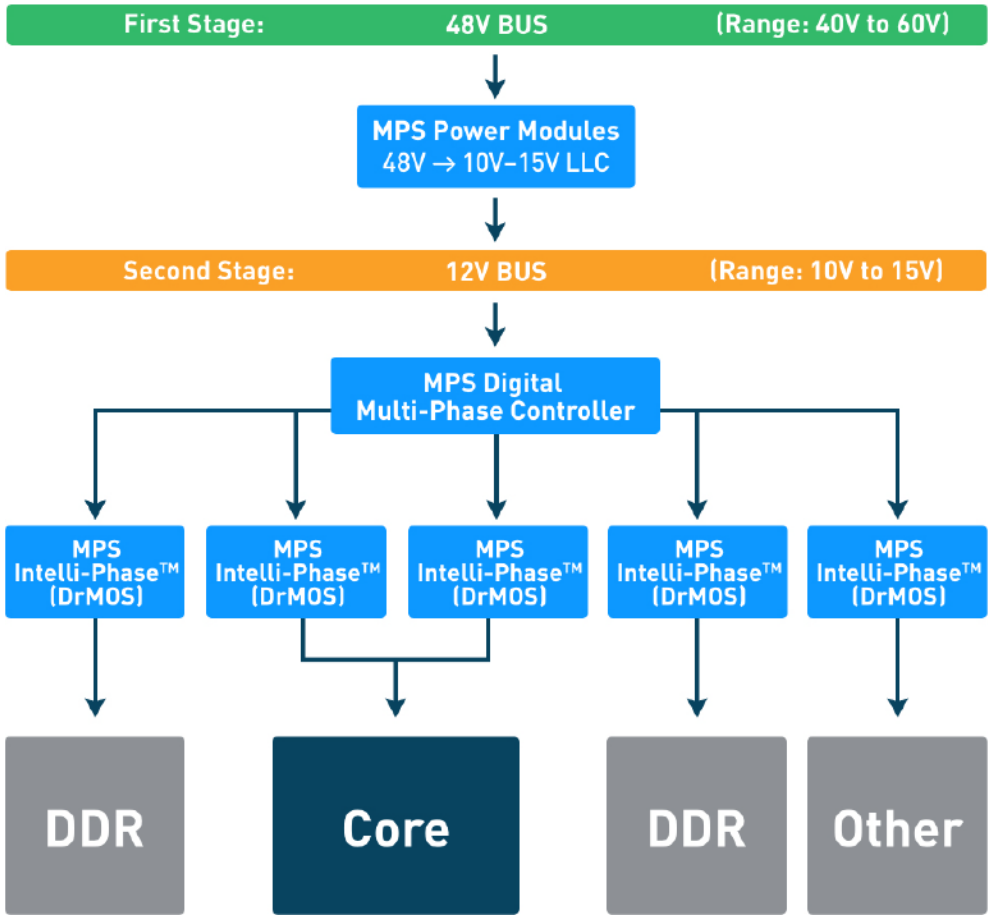
The Next Trend: 48V→12V Conversion, 4:1 LLC

Why 48V → 12V? Key Reasons:

1. **System Development**. Easiest method for 48V migration – can reuse an existing 12V system
2. **Solution Size**. 4:1 conversion can be placed in smaller form-factor, improving system layout

Datacenter power products follow trend for higher power density & efficiency. Regardless of winding ratio or topology new techniques and technologies are vital to maintain relevance.

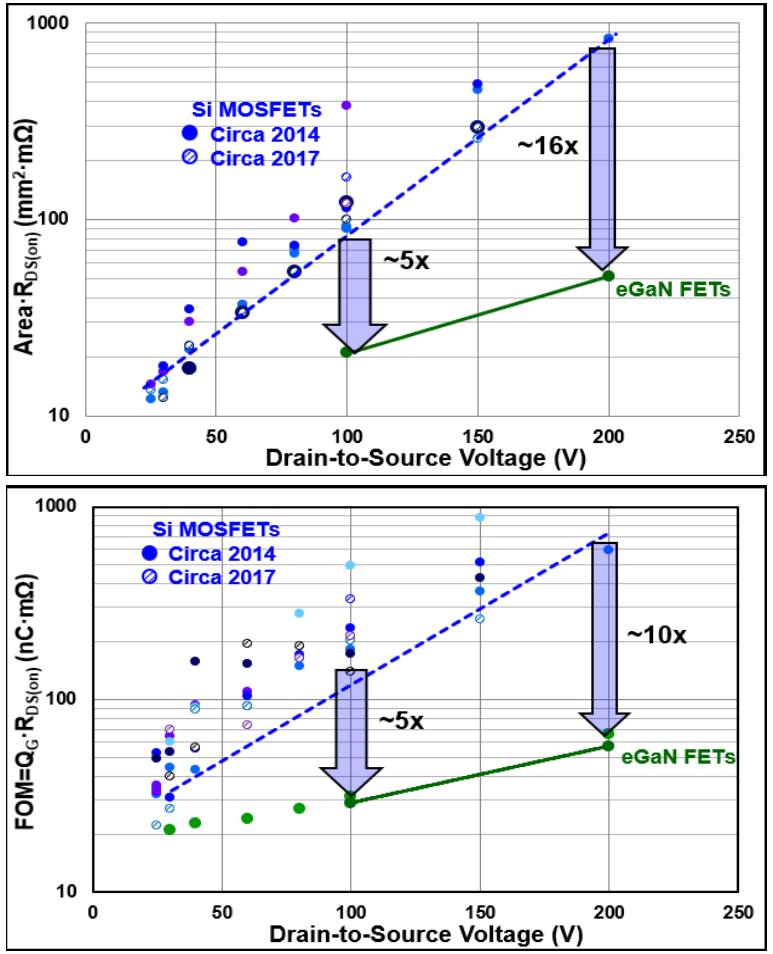




The electrical challenge

The Electrical Advantage

- The theoretical on-resistance versus blocking voltage of a GaN transistor is more than three orders of magnitude lower than that of silicon
- Using the $R_{DS(ON)} \cdot Q_G$ figure of merit, GaN devices show an improvement between almost three times to more than ten times that of silicon, with larger advantages at higher voltage

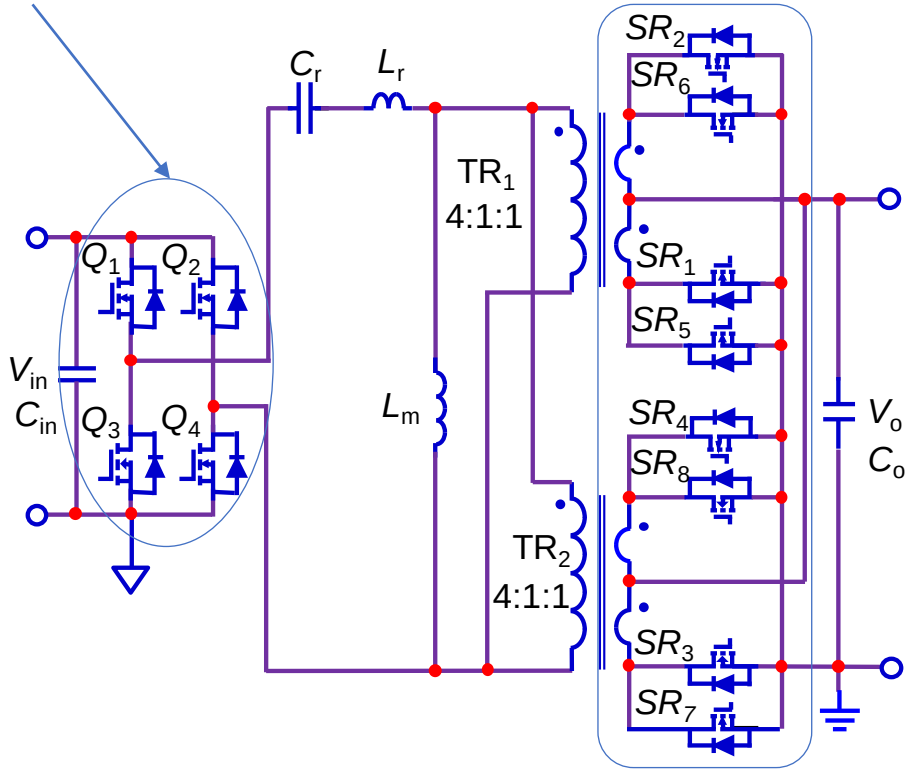


Lidow, Alex; de Rooij, Michael; Strydom, Johan; Reusch, David; Glaser, John. GaN Transistors for Efficient Power Conversion (pp. 43-44). Wiley. Kindle Edition. s

LLC DCx @1MHz

High Density applications operate at fsw ~ 1 MHz

EPC transistors widely outperform alternative solution for primary (100 V or 80 V)



EPC transistors offers competitive performance for 12 V output with ½ of the size vs Si MOSFET

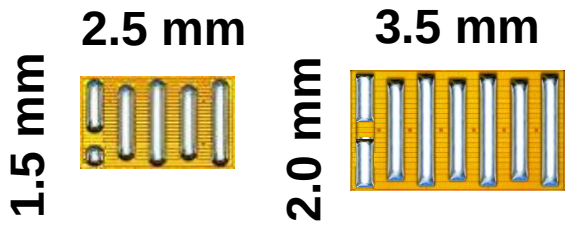
Specification	Min.	Nom.	Max.	Units
Vin	40	48, 54	60	Volts
Vout		12		Volts
Pout		300 W – 2.5 KW		Watt

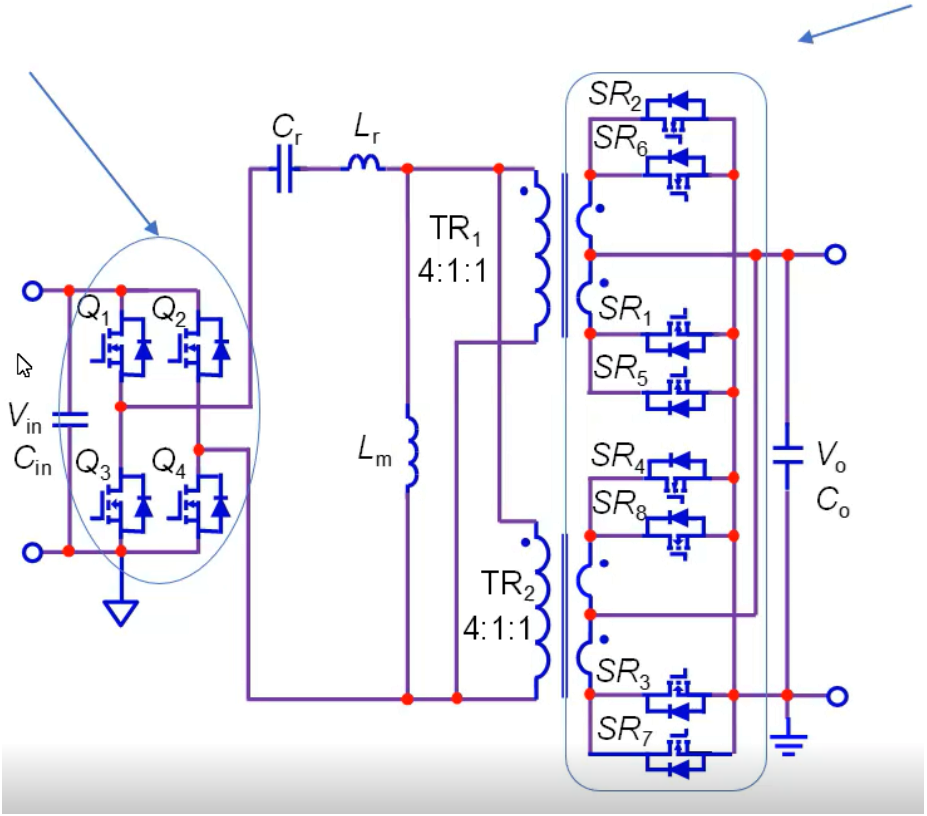
- *Shown with 2 paralleled FETs for secondary and for 4:1*

eGaN FETs for LLC DCx

Primary Side eGaN FET

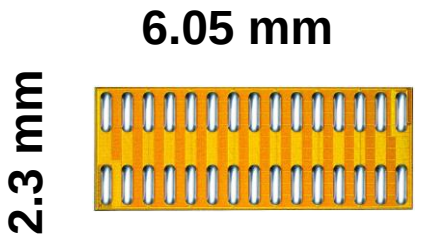
Typical Specification	EPC2204	EPC2218
$V_{ds,max}$	100 V	100 V
$R_{ds,on}$	4.5 mΩ	2.5 mΩ
Q_{oss}	25 nC	46 nC
Q_{gd}	0.9 nC	1.6 nC
Q_g	6.4 nC	11.8 nC
$R_{\theta,jc}$ $R_{\theta,jb}$	1 °C/W 2.5 °C/W	0.54 °C/W 1.8 °C/W





Secondary Side eGaN FET

Typical Specification	EPC2024
$V_{ds,max}$	40 V
$R_{ds,on}$ at 4.5 V_{GS}	1.2 mΩ
Q_{oss}	45 nC
Q_{gd}	2.4 nC
Q_g	18 nC
$R_{\theta,jc}$ $R_{\theta,jb}$	0.4 °C/W 1.1 °C/W

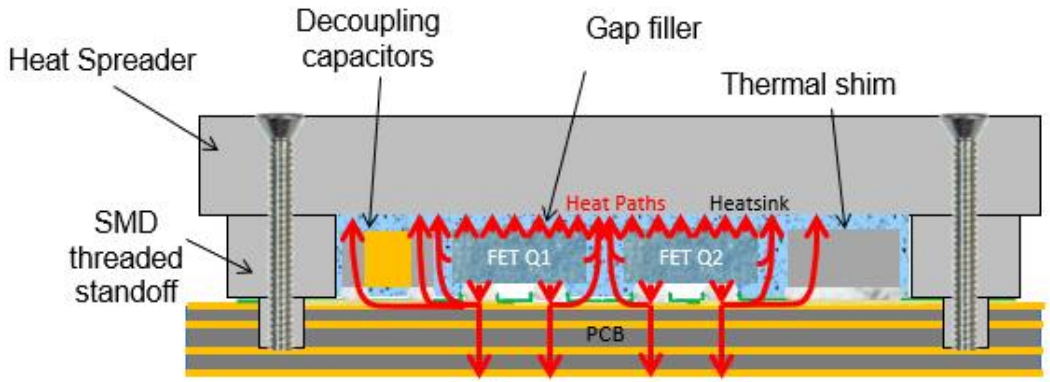


The Thermal Challenge

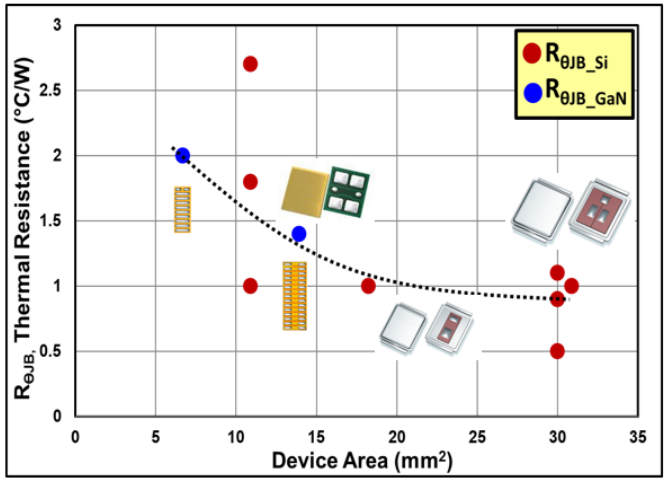
Best Thermal Performance with Double Sided Cooling

How to achieve optimal thermal performance:

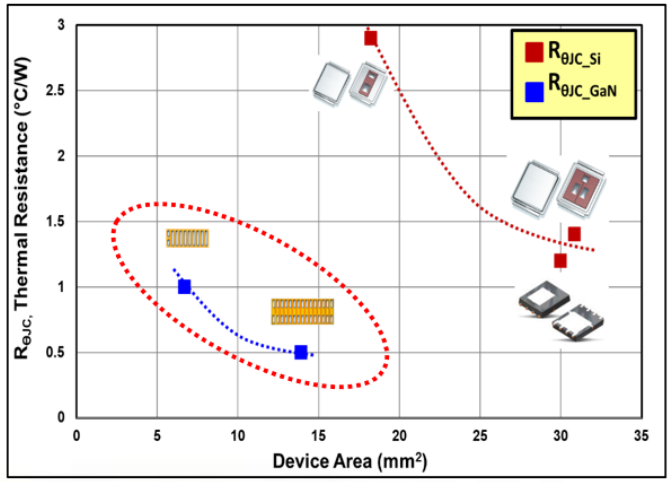
- Thermal Vias
- Gap pads
- Heat-spreader (dual sided cooling)



Heat transfer to PCB $R_{\Theta JBoard}$

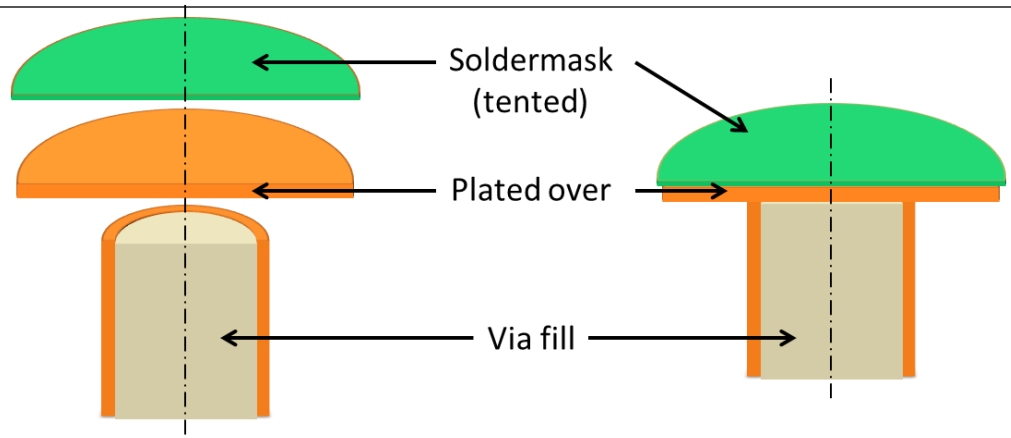


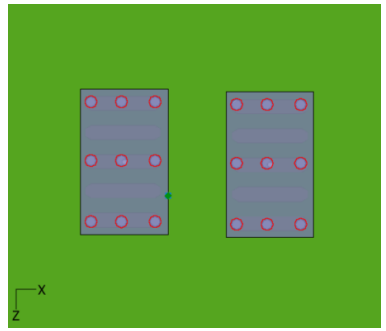
Heat transfer to top Si substrate $R_{\Theta JCase}$

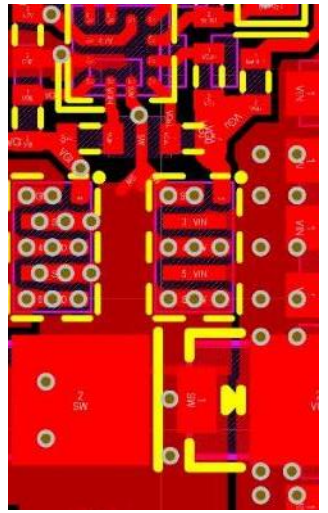


Vias Construction (VIPPO)

- Vias are
  - non-conductive filled (better CTE vs board)
  - plated over
  - hole diameter (typical) = 7.8 mil
  - annular ring = 13.8 mil diameter min.
  - wall thickness = 0.78 mil per IPC standard class 2
- Used for under bump and close to component pads
- Used for up to 2 oz copper thickness





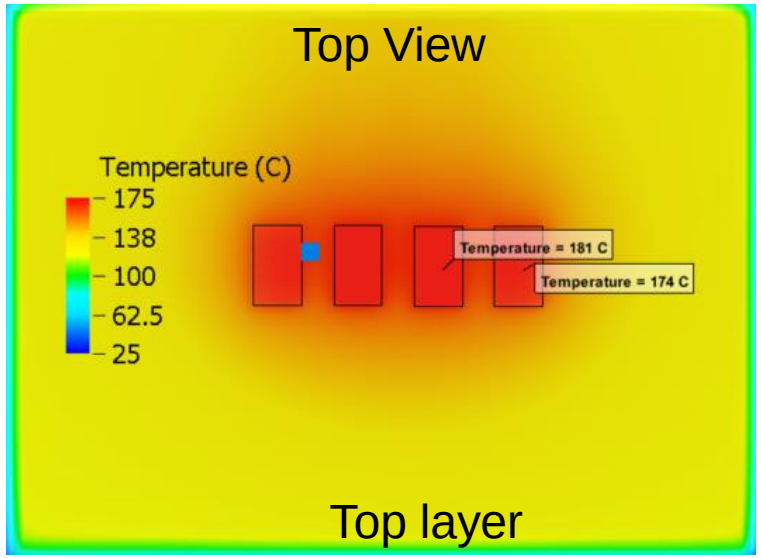


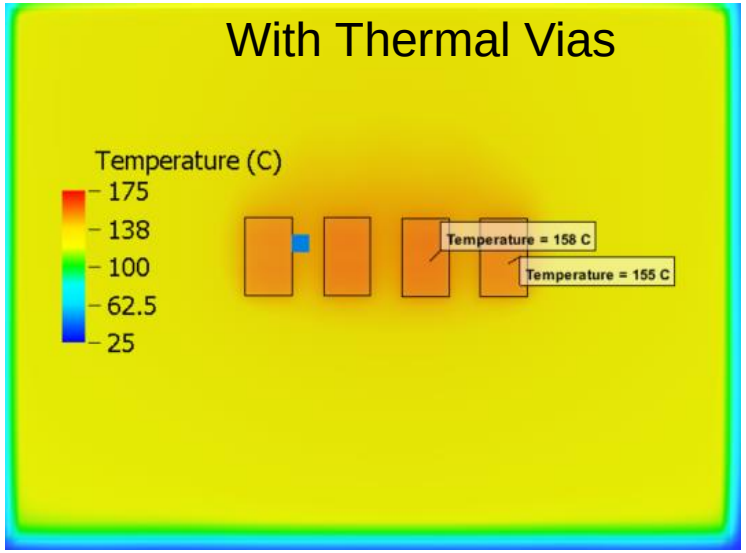
Practical Example layout showing vias for EPC2204

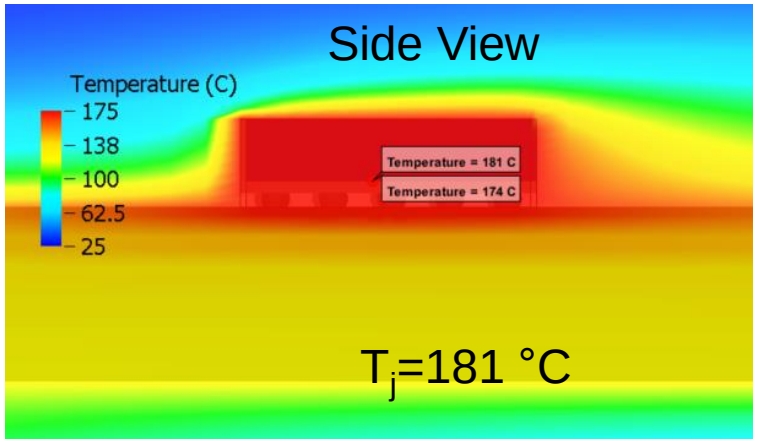
Effect of Vias On Thermal Performance

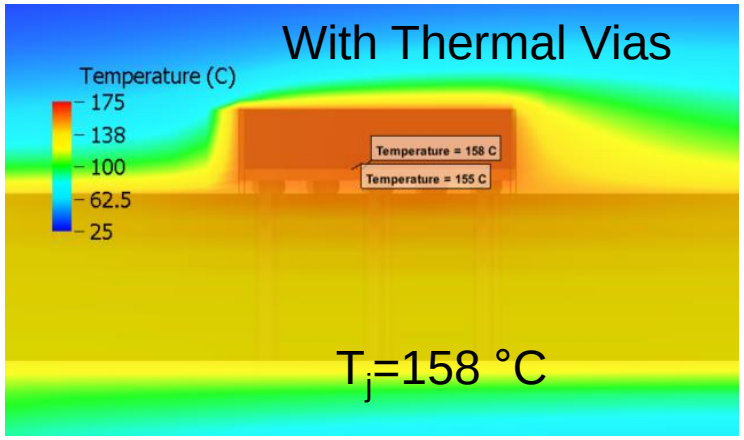
- Vias improve heat conduction into the board
  - High thermal conduction path into the FR4 insulating layers
  - Use heat spreading in copper layers
- Board design without vias has ~18% higher FET temperature rise

Simulations with EPC2204, LLC application
750W, 6 layers 2oz PCB



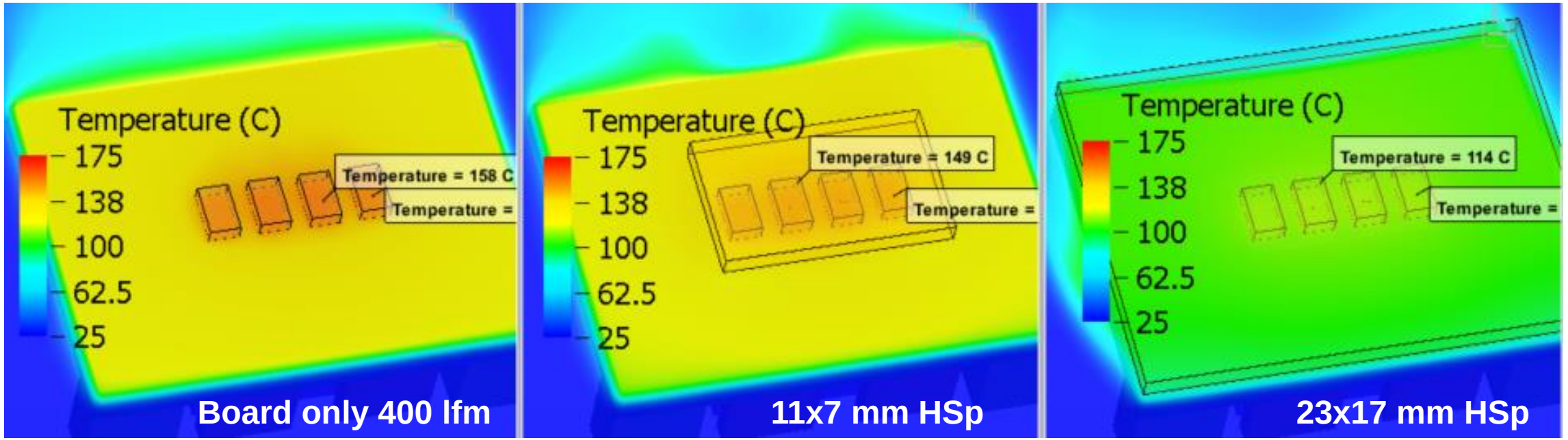






Effect of Heat-Spreader Size

- Larger area heat-spreader is more effective ~52×A_{FETs}
- Small area heat-spreader (~13×A_{FETs}) insufficient for optimal heat spreading



T_j=158 °C

T_j=149 °C

T_j=114 °C

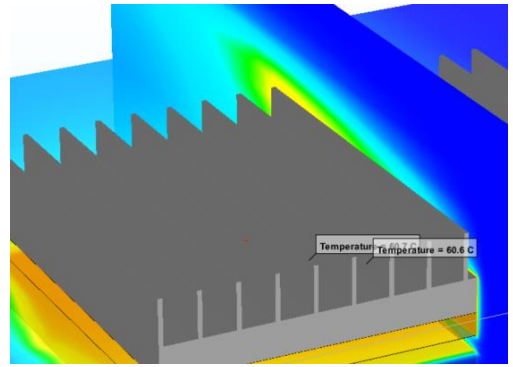
High Performance TIM is Recommended

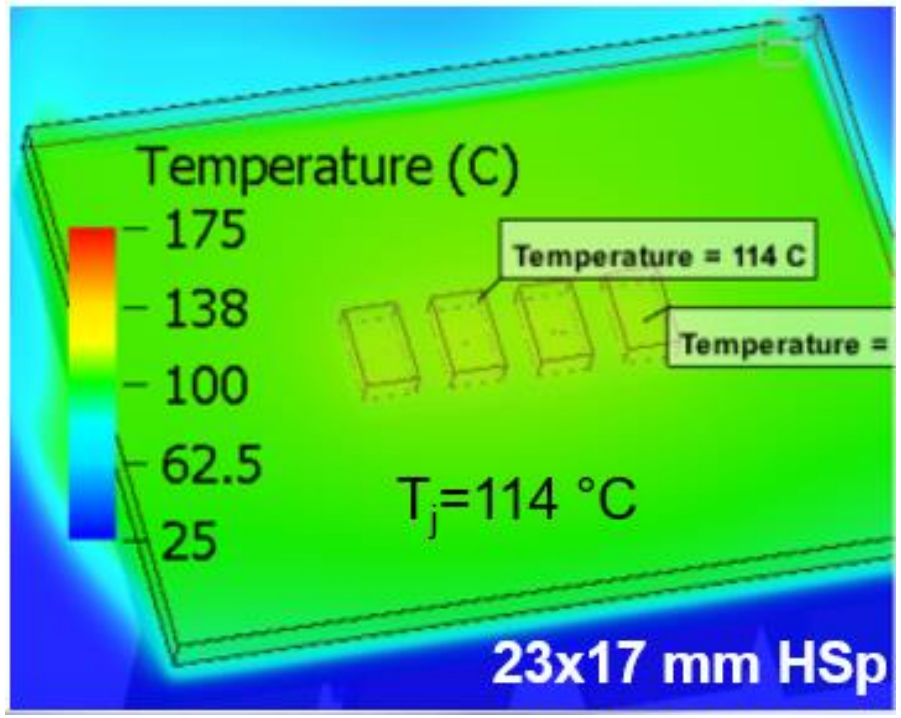
- Case A
  - TIM material: 0.3 mm T-Global A1760 with $\kappa = 17.6 W/m.K$
- Case B
  - TIM material: 0.2 mm, $\kappa = 3\ W/m.K$

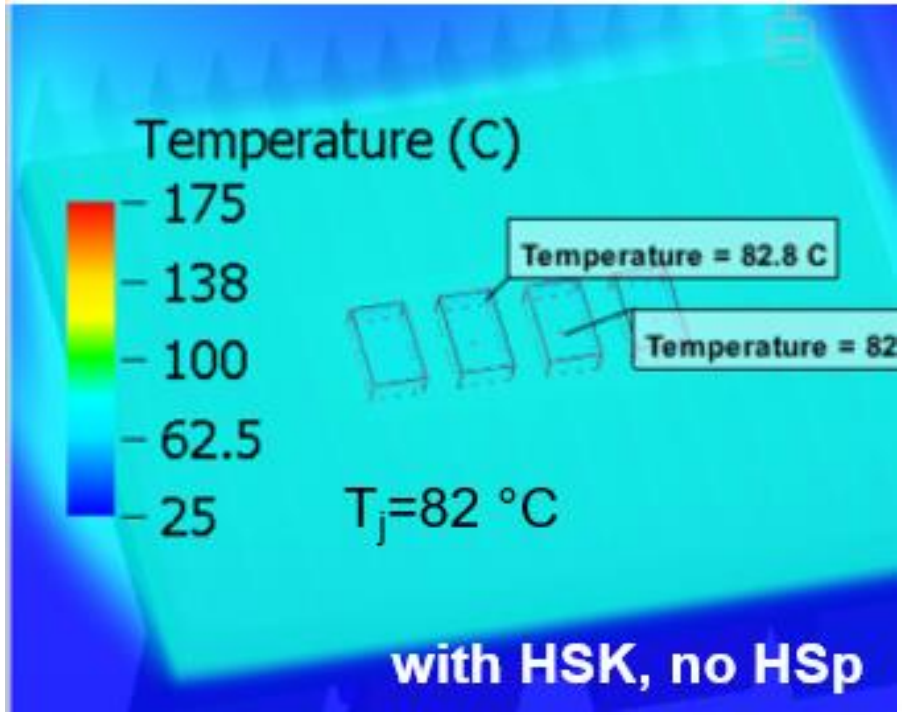
$Configuration$	Case A $T_J\ (°C)$, ΔT(°C)		Case B $T_J\ (°C)$, ΔT(°C)		Increase (°C)
Cu heat-spreader (23x17mm)	114	89	121	96	+ 7
Heatsink (3.5 mm total)	82	57	90	65	+ 8
Heat-spreader +Heatsink (4.5 mm total)	77	52	86	61	+ 9

Effect of Heatsink

- Thermal heat dissipation from the top can be further increased by using a heat sink instead of the heat spreader

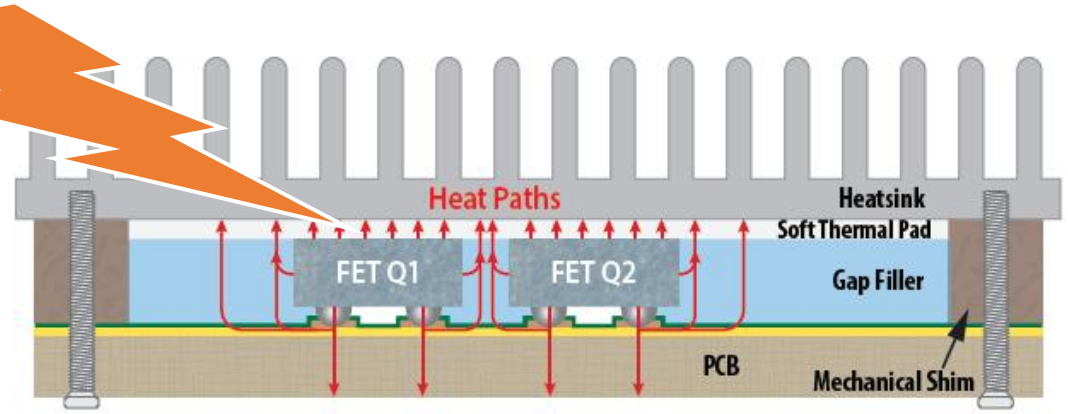






Thermal Challenge

1. Distance between heatsink and FET is critical for performance: 1mm standoffs is typically used
2. Area of heatsink is critical to improve heat spreading effect

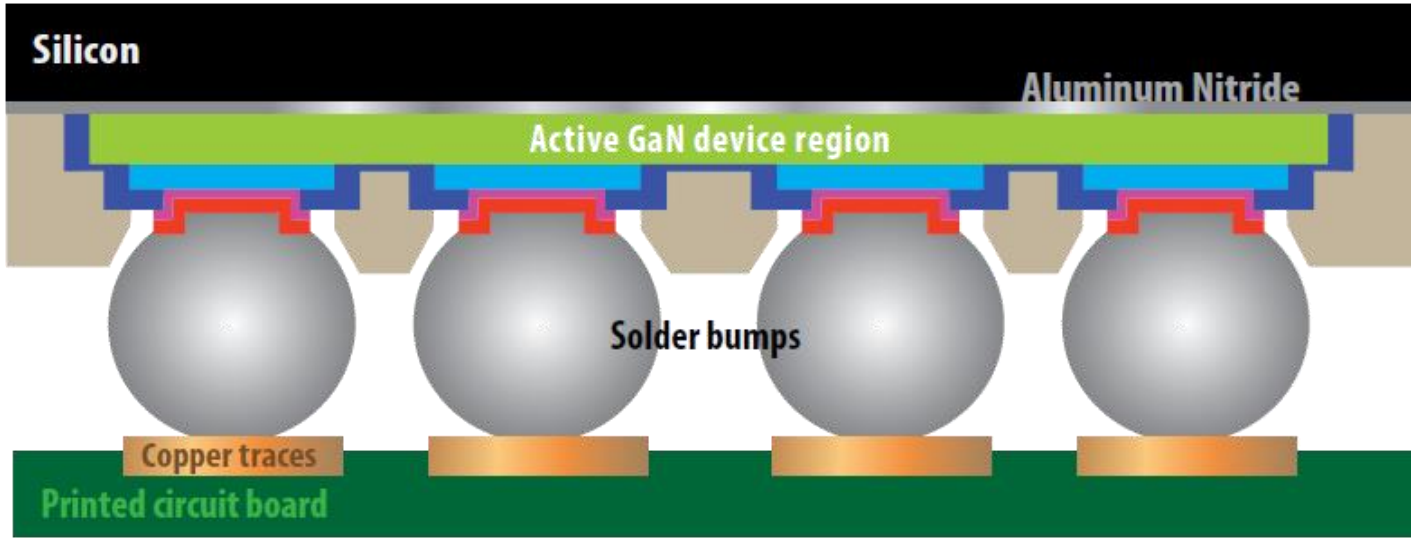


The challenge is to find low profile components that go around the FET to allow the heat sink mounting

The Manufacturing challenge

Wafer Level Chip Scale Package (WLCSP)

- EPC devices are available in WLCSP



Starting Silicon substrate
GaN device

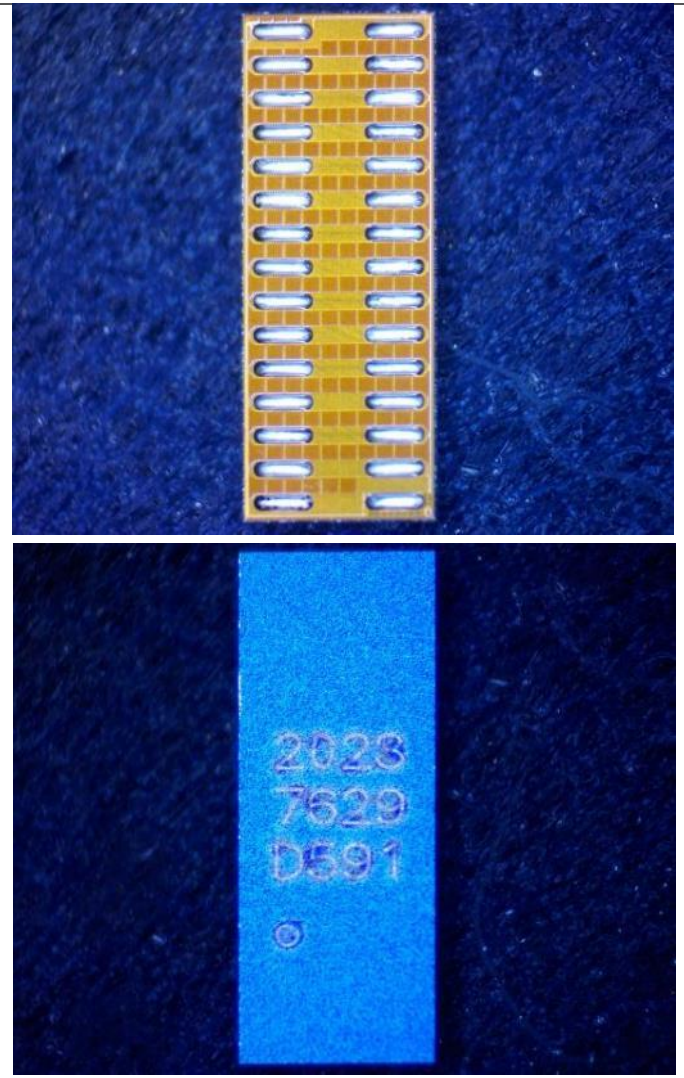
Connections to the
outside world

- This allows for the smallest PCB area utilization and highest power density

Wafer Level Chip Scale Package

- The quality of the solder bump interfacing the eGaN device to the PCB is crucial for a reliable electrical, thermal, and mechanical connection

- The top of the device is the Silicon substrate, it is not part of the active device. However, it is connected to the source potential, so care must be taken when attaching to a heat-sink



EPC2023: 6.05 mm x 2.3 mm

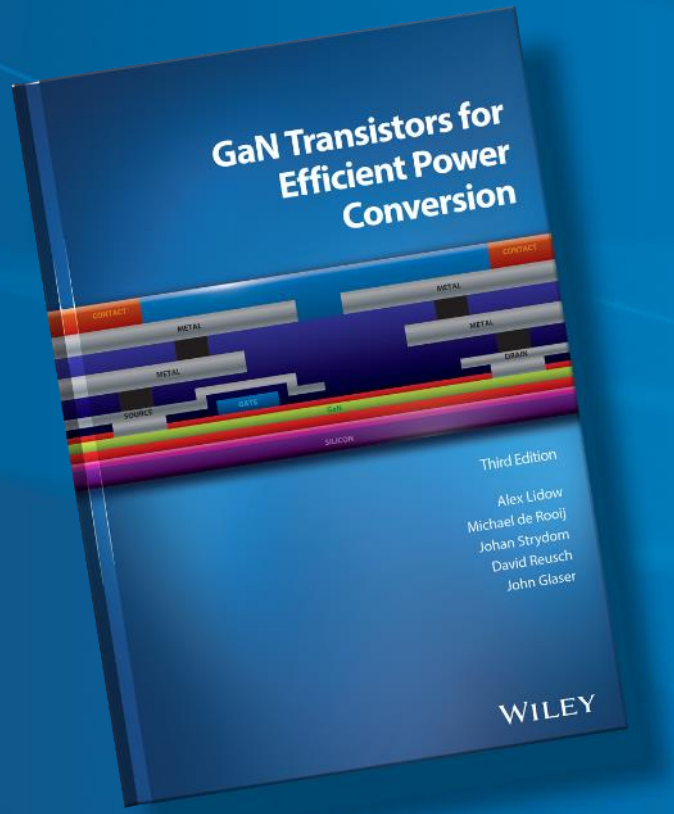
Conclusion

MPS and EPC are pushing the limits of power density and power efficiency for datacenters 48V power

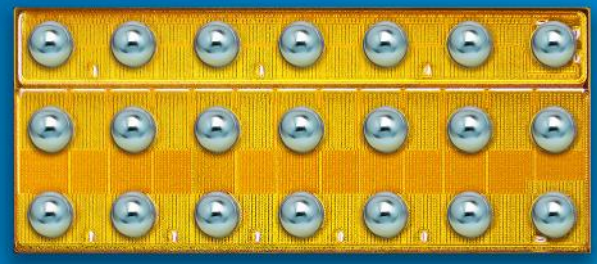
- MPC1100A is the first in a series … more to come!
- EPC eGaN enables MPS roadmap where Si is reaching its limits

EFFICIENT POWER CONVERSION

How To GaN Video Series

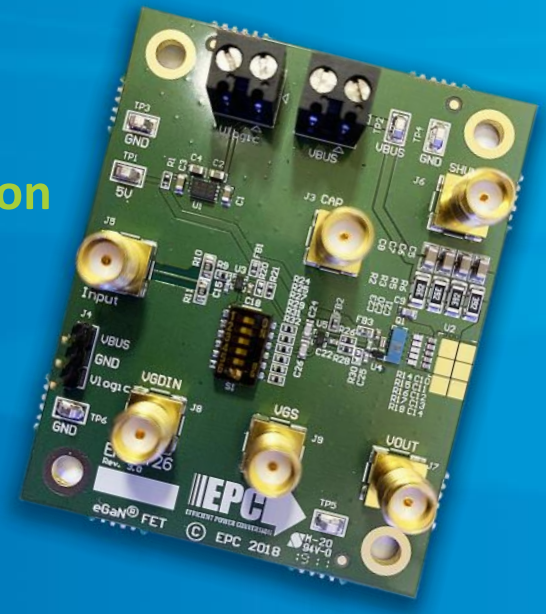


3rd Edition Textbook



eGaN® FETs and ICs

Evaluation Kits



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