Active Short Circuit and Repetitive Short Circuit in 1.2kV SiC MOSFETs

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Introduction

- SiC MOSFET technology is ideal for automotive drive-train applications which can utilize the higher efficiency of SiC to extend the range and/or reduce cost of Battery Electric Vehicles (BEVs)
- Automotive applications can lead to high stress environments under certain operating conditions
  - Hill hold, fault conditions, peak acceleration
  - Adding extra SiC die for peak operating conditions can add cost

It is important to understand the robustness limits of SiC MOSFETs during abnormal high stress conditions

Outline

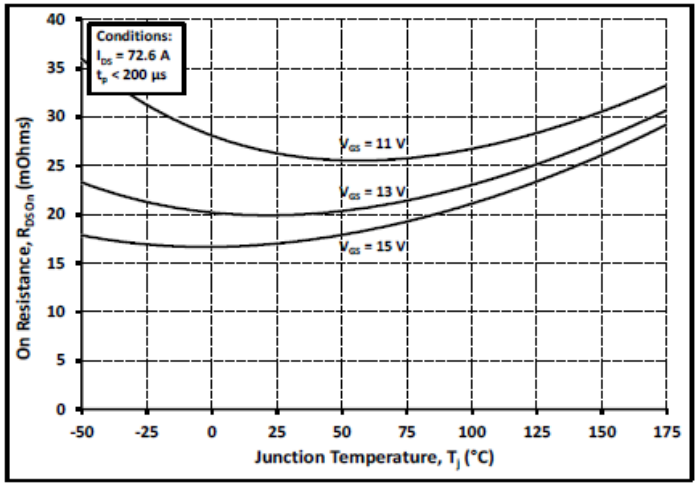
The robustness of a 1.2 kV, 17 mΩ MOSFET will be considered for two different high stress tests

1. Repetitive Short Circuit
2. MOSFET Surge Testing

Device under test

QPM3-1200-0017C Automotive Die

- 1200 V, 17 mΩ SiC MOSFET
  - Pre-released SiC MOSFET for evaluation
- Gate drive voltage: -4 V/ +15V
- Packaged in TO-247-4L package (kelvin) for these tests

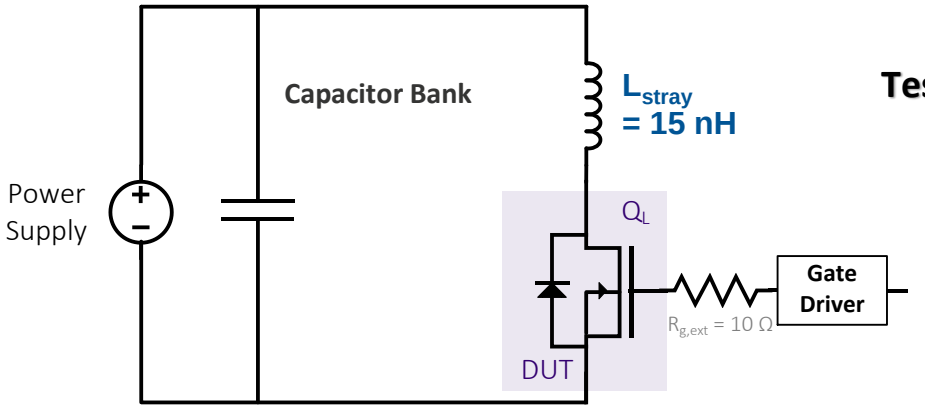


1200V, 17 mΩ SiC MOSFET

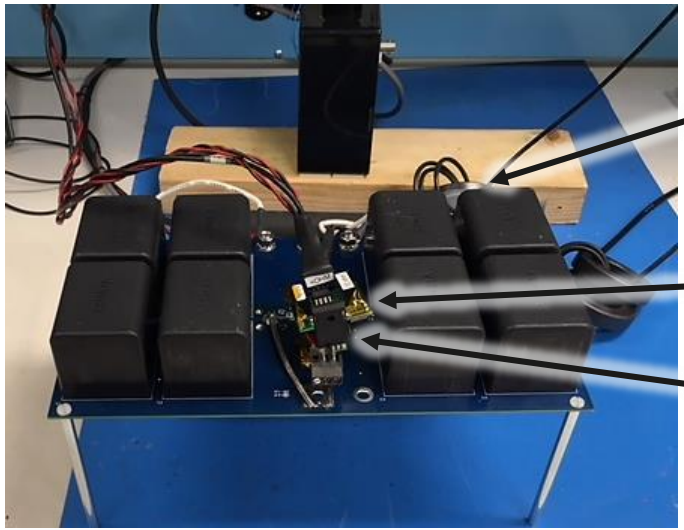
Repetitive Short Circuit

Short Circuit Test Set-up

Test Circuit



Test Set-up



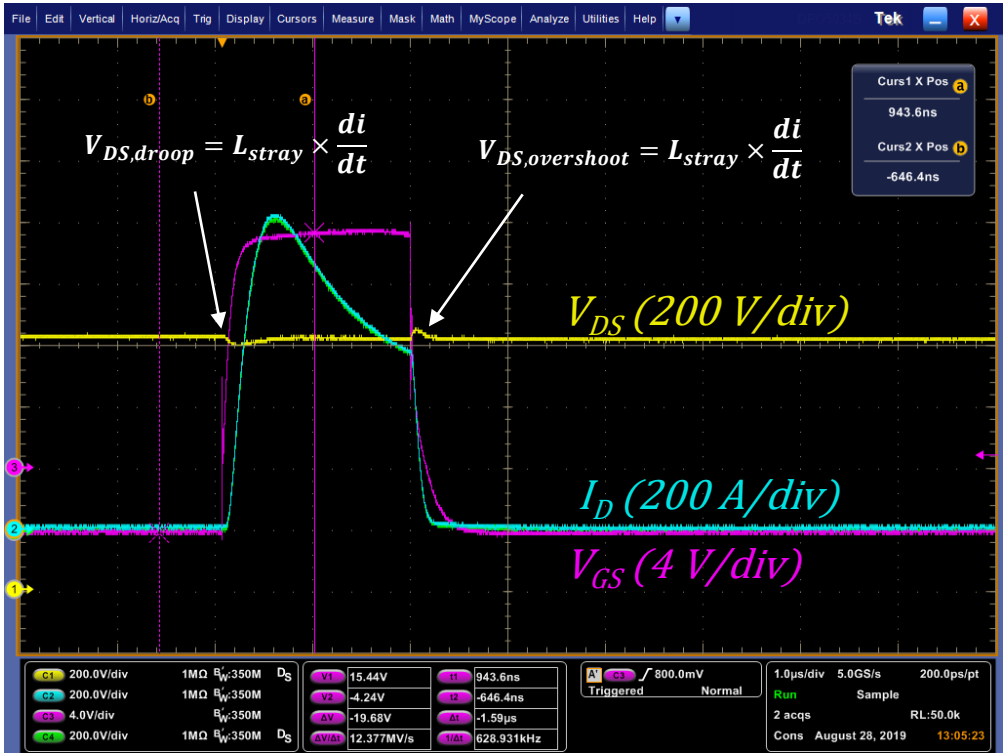
L_{stray} is designed to be as low as possible:

- **Gives the fastest current rise**
- **Decreases the amount of drain to source voltage droop during fault turn-on ($V_{DS,droop} = L_{stray} \times \frac{di}{dt}$)**
- **Prevents the device from going into avalanche ($V_{DS,overshoot} = L_{stray} \times \frac{di}{dt}$)**

Short Circuit Waveform

Test Considerations

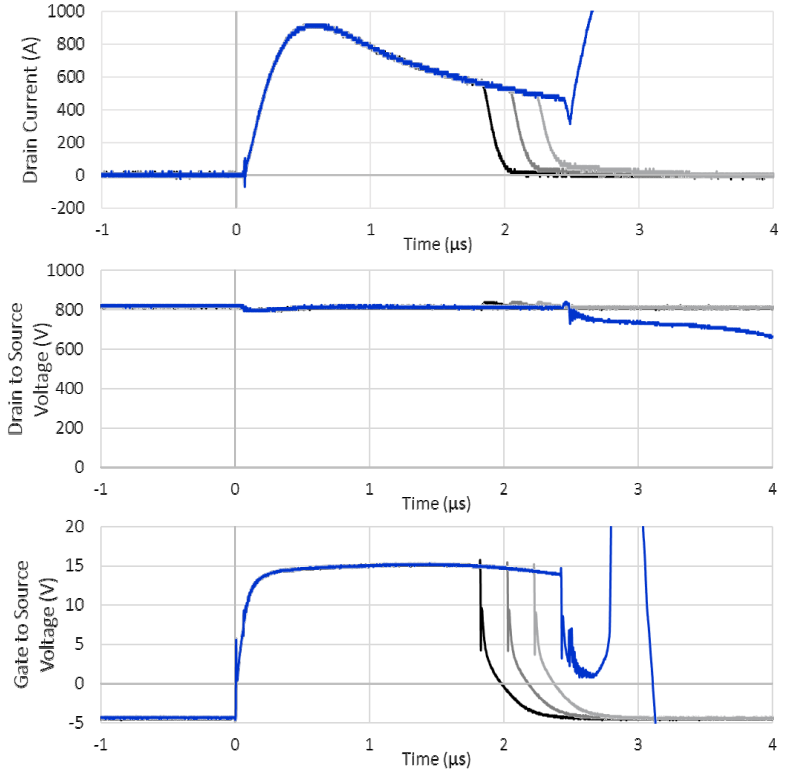
- V_{DS} stays within 15% of the specified voltage (this is controlled by having a very low stray inductance)
- Current levels through the device reach over 10X the rated current



V_{DS} = 800 V, V_{GS} = 15 V, R_g = 10 Ω, T = 25°C

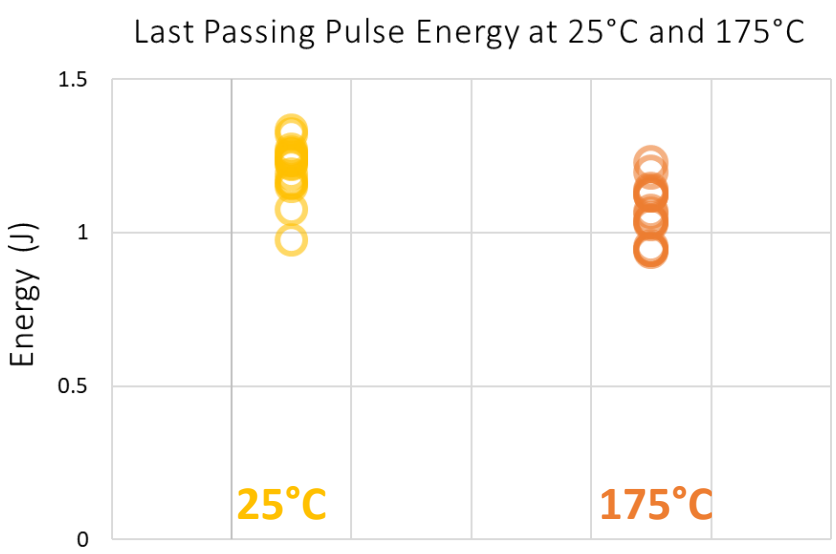
Test Procedure

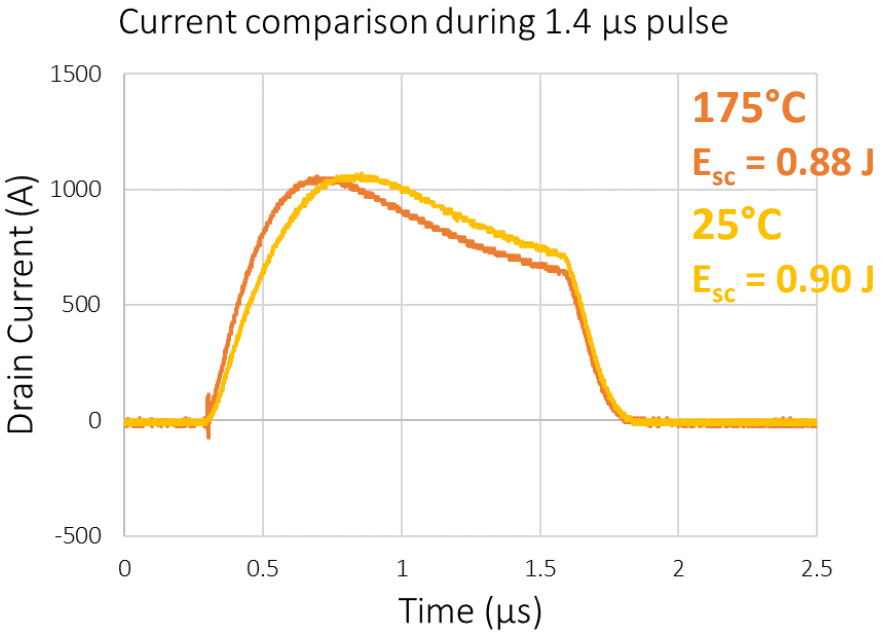
- To get the T_{SCWT} the device is given a short pulse, if the device survives this pulse, the pulse width is increase by 200 ns.
- The pulse width is continually increased until the device degrades
- Static measurements are taken in between each pulse
- T_{SCWT} = last good pulse (last pulse width that the device survives)



V_{DS} = 800 V, V_{GS} = 15 V, R_g = 10 Ω, T = 175°C

Expected Energy Levels during a SC Event





V_{DS} = 800 V, V_{GS} = 15 V, R_g = 10 Ω

1.4 µs was selected as the pulse width for repetitive SC testing

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Repetitive SC Test Overview

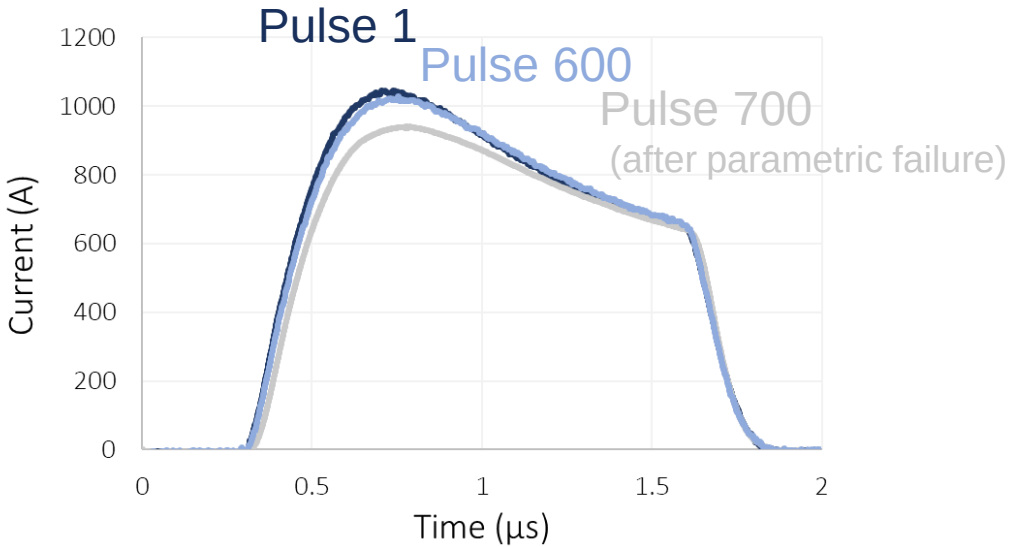
Two devices were pulsed repetitively with a 1.4 µs pulse with post tests after every 100 pulses

DUT 1

25°C, *1000 pulses passed*

DUT 2

175 °C, *600 pulses passed*



V_{DS} = 800 V, V_{GS} = 15 V, R_g = 10 Ω

30s cool down between each pulse

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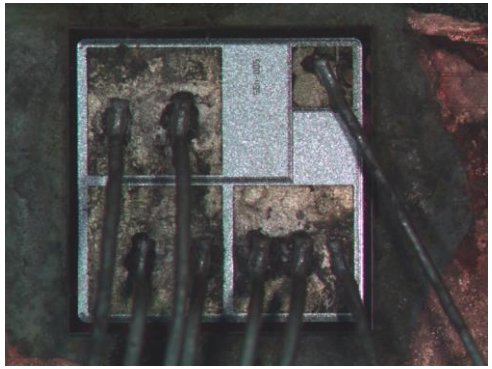
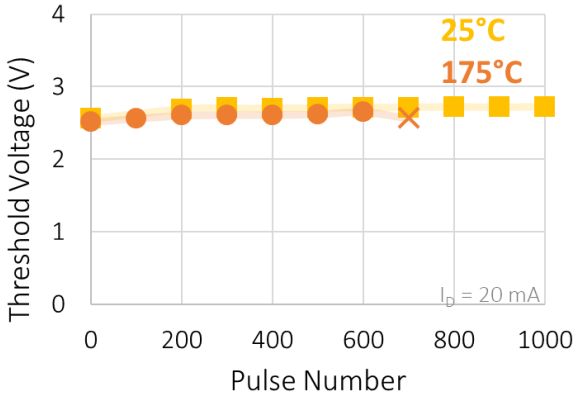
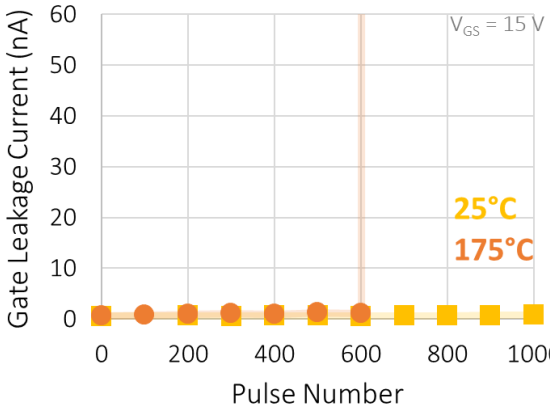
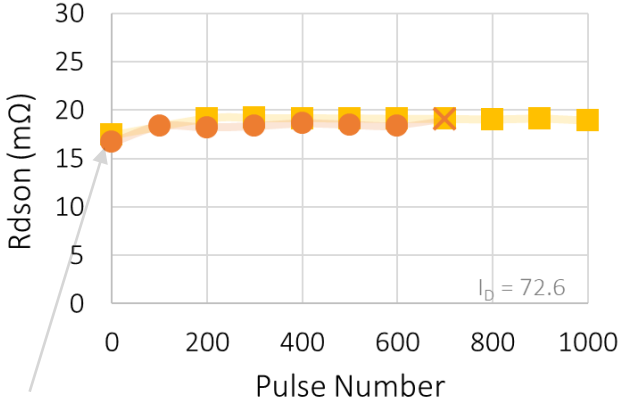
Parametric Test Results

- Pre tests were measured before starting the SC testing (Pulse 0)
- Post tests were measured after every 100 pulses
- At 175°C, device passed 600 pulses but failed post test after 700 pulses









Small increase in Rdson is due to measuring without kelvin for post tests

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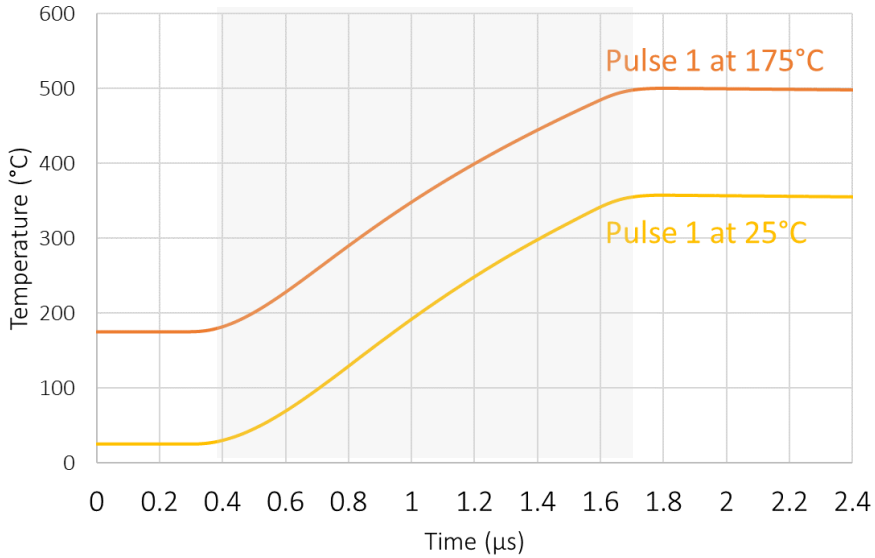
Junction Temperature Estimation

- A Cauer thermal model is created in LTSpice using the thermal impedance measurements from the TO-247-4L package for this 1200 V, 17 mΩ device
- The measured instantaneous power waveform ($V_{DS} \times I_D$) captured during the short circuit event is then input into a thermal simulation to estimate the die junction temperature during the SC event



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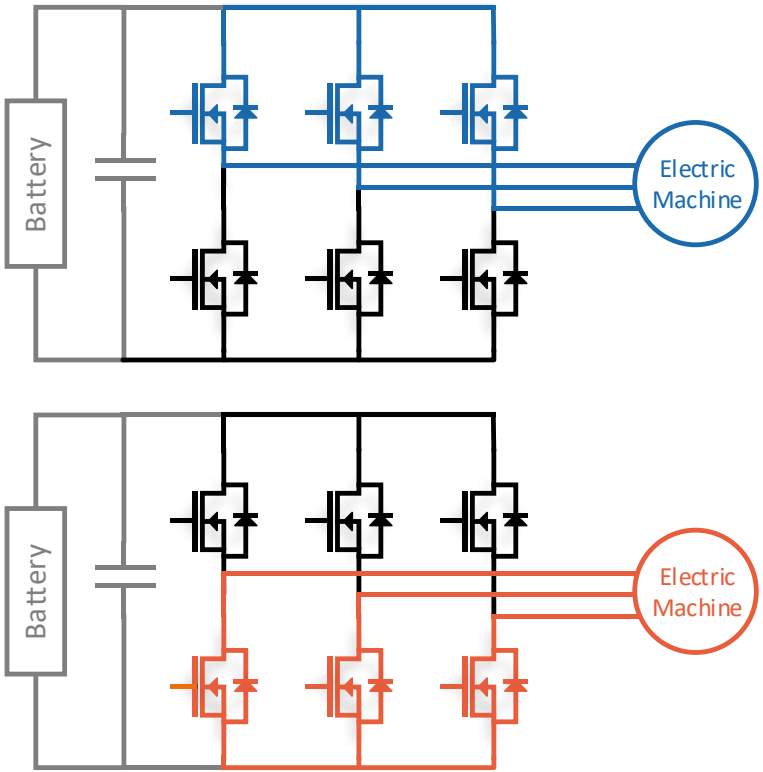
Repetitive SC Summary

- Two devices were repetitively stressed with a 1.4 µs pulse width (one at 25°C and the other at 175 °C)
- At room temperature the device lasted 1000 pulses (and still no signs of failure)
- At high temperature the device started to show signs of degradation after > 600 pulses
- In most applications, it is expected that the device will not go through more than 10 short circuit events

1200V, 17 mΩ SiC MOSFET

Active Short Circuit

Active Short Circuit Overview



Active short circuit is a failure mode operation point

- When a failure in the system is sensed either all of the top switches or all of the bottom switches are shorted
- This is a safe operating mode for the electric machine and keeps the battery from being damaged
- The main cause of concern is that this causes a surge in current in the power semiconductor devices

Device performance in this operation mode can be evaluated using MOSFET surge testing under different gate voltage conditions

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MOSFET Surge Test Overview

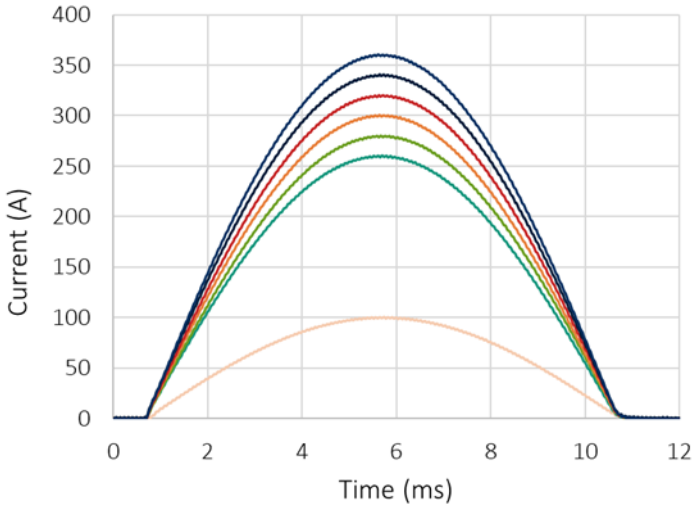
Purpose
To test the surge capability of a SiC MOSFET during channel operation and body diode operation

Set-up
DUT is held at a constant V_{GS} with an isolated power supply. An electronic load is used to create a controlled current half-sine wave through the device

Plan
Device is pulsed for multiple events, under different current stress levels until the device fails

MOSFET Surge Test Plan

1. V_{GS} is held at constant voltage (**-4 V, 0 V, or 15 V**)
2. DUT is given stress pulse with a certain peak current level (half sine wave) with a **10 ms pulse width**
3. Stress pulse is **repeated 20 times** (with the same current level) with a 30s cool down between each pulse
4. Post stress parametric test is used to check for failure
5. Peak stress current level is increased by 20 A
6. Steps 1-5 are repeated until the device fails the post test
7. MOSFET current surge rating is from “last passing current level”



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Surge Waveforms (10 ms, V_{GS} = -4 V)

- Current is increased in 20 A increments until the device fails the post test
- Last passing current level is 340 A (current stress before failing current level)
- Since the channel is off, the current is conducting through the body diode

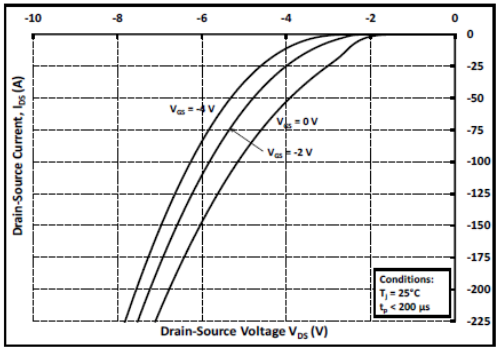
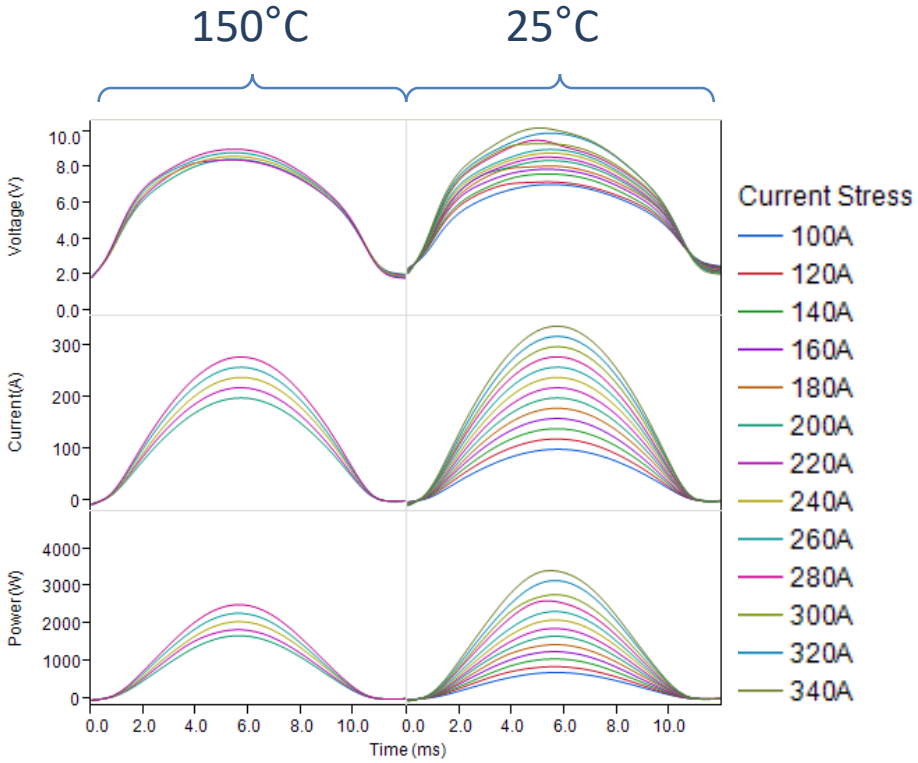


Figure 9. Body Diode Characteristic at 25 ºC



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Surge Waveforms (10 ms, V_{GS} = 15 V)

- When V_{GS} = 15 V the channel is open so conduction can occur through the channel
- At higher currents the body diode starts additionally conducting current in parallel

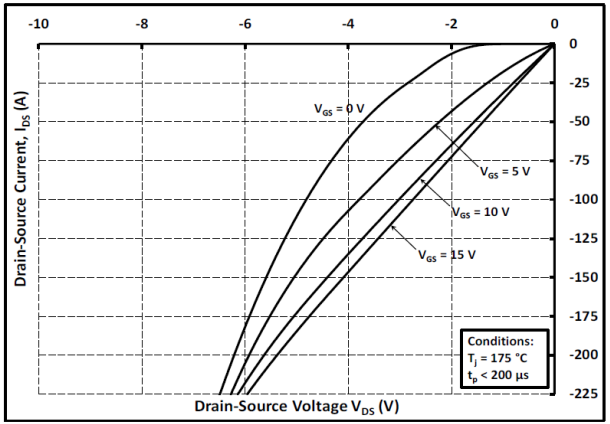
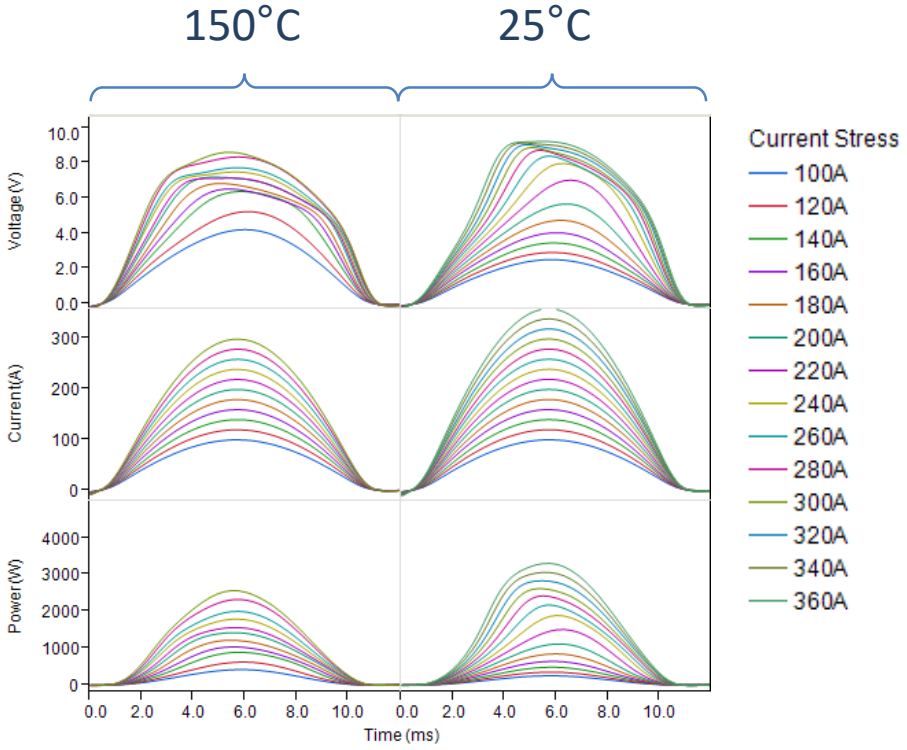


Figure 15. 3rd Quadrant Characteristic at 175 °C



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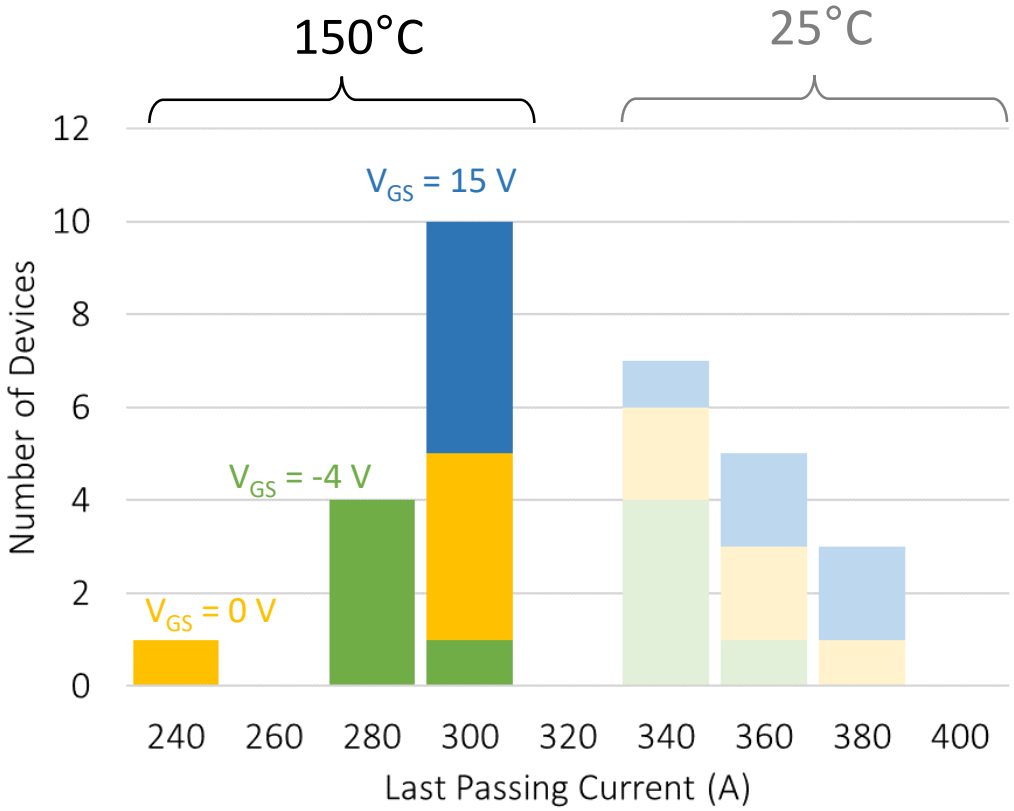
Surge Current Distribution for ***10 ms Pulse Width***



- There is a clear shift in the performance when comparing 25°C to 150 °C
- There is not a large variation for the different gate voltage conditions

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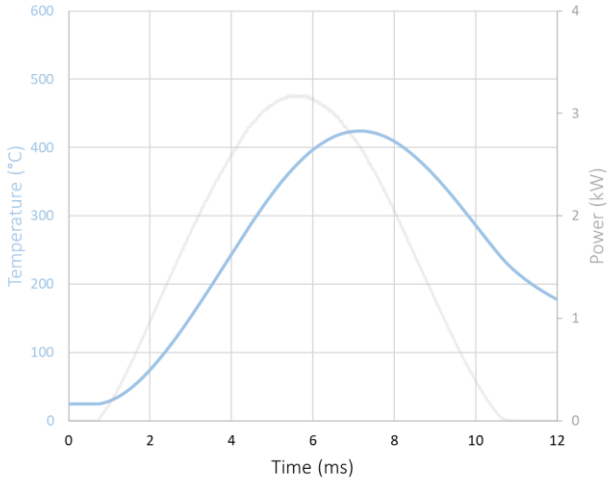
Junction Temperature Estimation for V_{GS} = -4 V (10 ms)

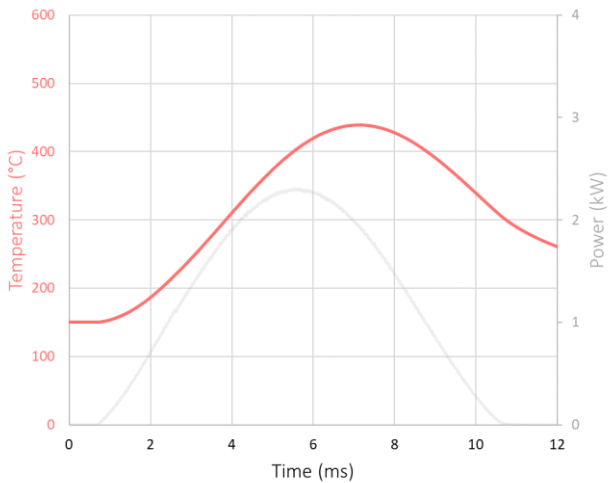
Foster thermal network in LTSpice was used (with surge output waveforms) to estimate the junction temperature during a surge current stress event

Overall temperature reaches similar value in both initial temperature cases

Last good pulse = 340 A
T_c = 25°C



Last good pulse = 280 A
T_c = 150°C



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Summary of ASC Results

Pulse Width	Temperature (°C)	Gate Voltage (V)	Number of Parts Tested	Overall Lowest Passing Current (A)
2 ms	25	-4	5	580
	150	-4	5	500
	25	0	5	580
	150	0	5	500
	25	15	5	600
	150	15	5	520
10 ms	25	-4	5	340
	150	-4	5	280
	25	0	5	340
	150	0	5	240
	25	15	5	340
	150	15	5	200

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Final Summary

- The robustness of a 1.2 kV, 17mΩ device was evaluated for two different high stress conditions
  - Under repetitive short circuit conditions, the device can withstand up to 600 SC pulses when pulsed for 1.4µs at 175°C
  - For MOSFET surge testing, the device can conduct large surges in the reverse conduction current
- Short circuit and active short circuit modes result in high junction temperatures for the die under stress
  - The devices are still able to withstand many of these high temperature events, enabling support for these abnormal operating modes of automotive drivetrain applications