Gate oxide reliability studies using BTI, RVS, and CVS methods on 4H-SiC MOSFETs

Gavin D.R. Hall, Jifa Hao,
Martin Domeij, and Thomas Neyer

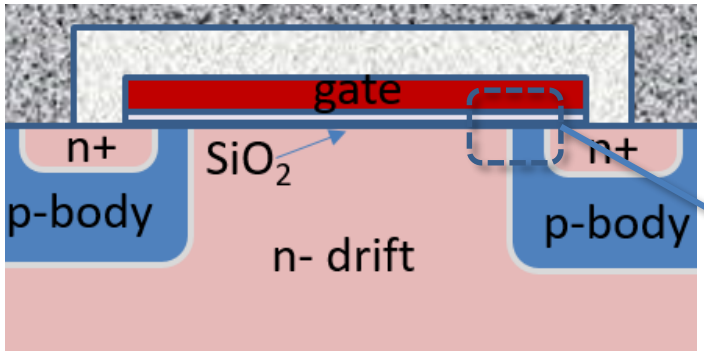
Outline

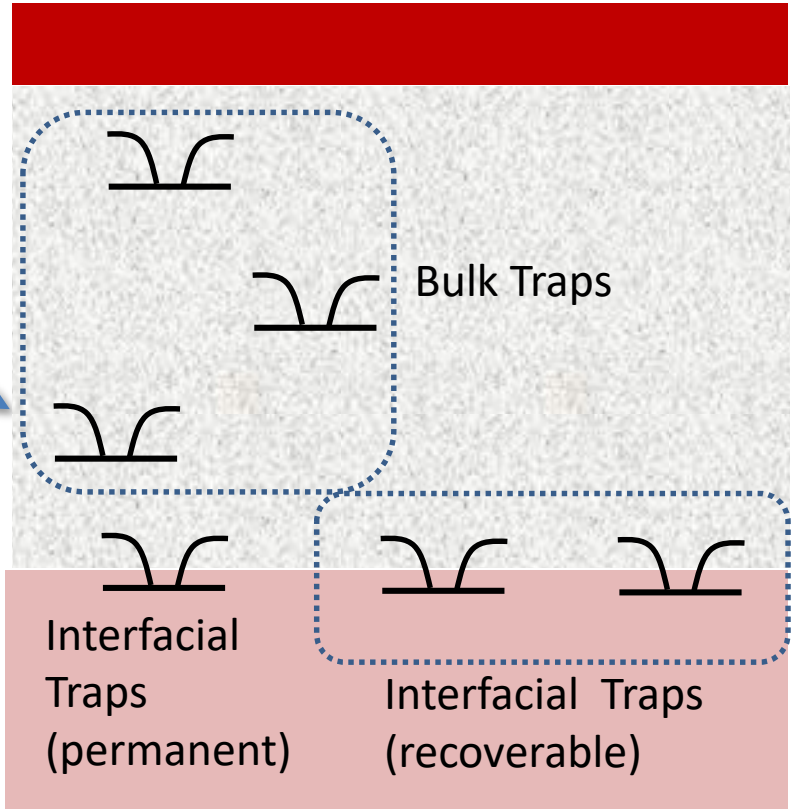
- Introduction
  - The Gate Oxide system in SiC MOSFET
  - Study of the gate oxide → study of time constants & their variability
- Bias Temperature Instability (BTI)
  - Fast and slow time constants and their temperature dependence
- Constant & Ramped Voltage Stress (CVS & RVS)
  - Accelerated testing and hard breakdown
  - Using a “Dual Ramp” Method to decrease time constant
  - Competing Failure Modes & Compensation
- Conclusion & Outlook

Introduction and Background

- Gate Oxide Reliability is Time to Event Data
  → Time Constants & Their Variability
- Regarding Time Constants
  - Performance related
  - Hard breakdown – Sudden change to a non-functional state (TDDB)
  - Fast vs. Slow Time Constants
- Regarding Variation
  - Variation aware analysis → efficient use of data
  - Characterizing variation → enables design

SiC Oxide System: Si / SiO2 / SiC





- Gate oxide performance and reliability influenced by “traps”
- In bulk, interface and regions in between (border)
- Timescales are driven by capture and emission from these sites

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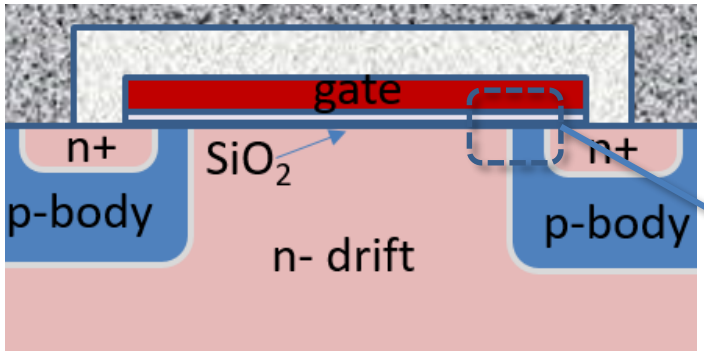
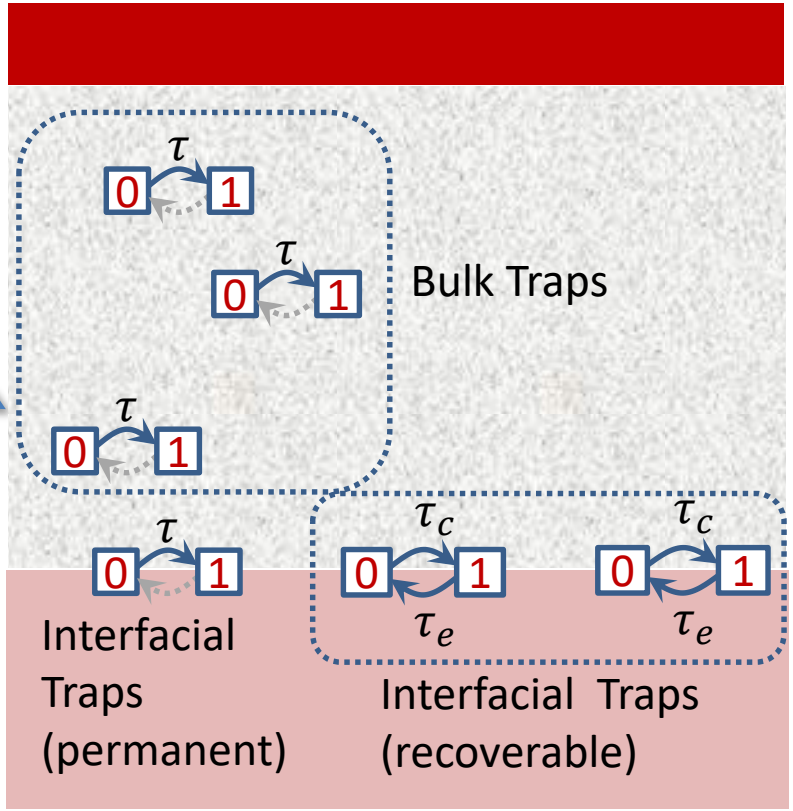


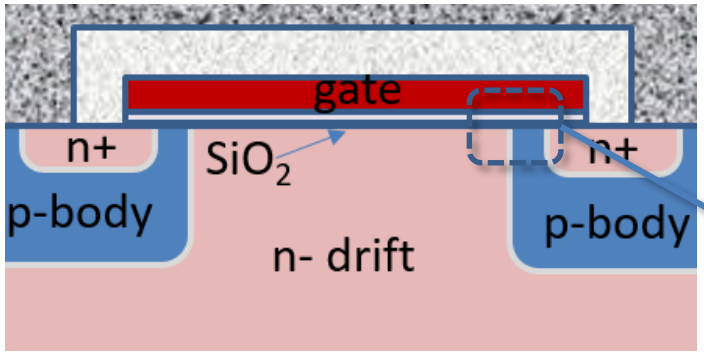


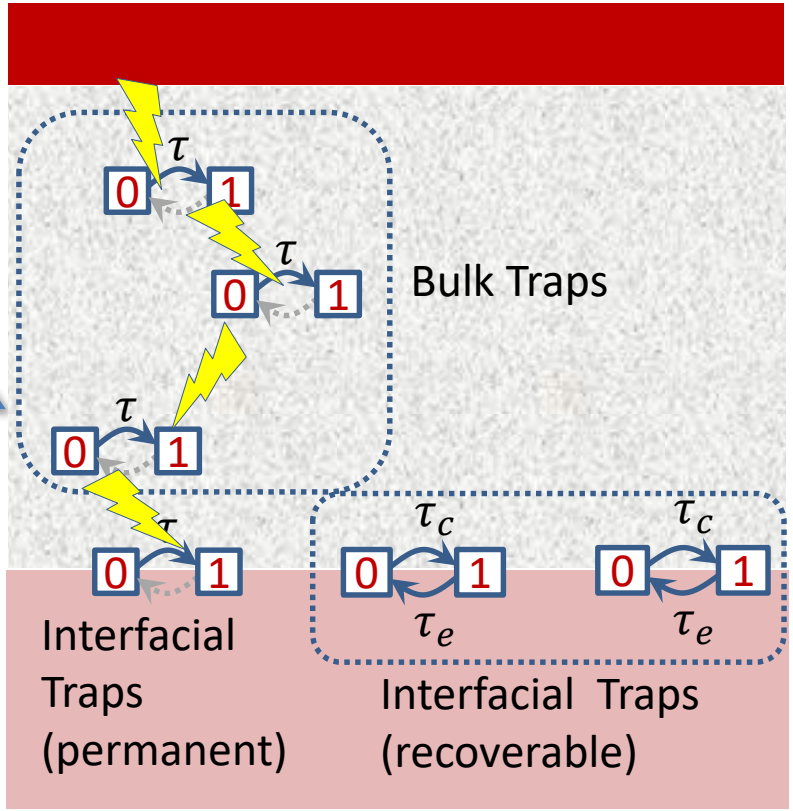
- Some traps have very slow emission times – practically permanent
- Parametric instability can be due to all of these traps' dynamics[*]
- Dielectric breakdown is precipitated by a series of traps leading to thermal runaway (Klein-Solomon Model) [**]

[*] T. Grasser *Bias Temperature Instability for Devices and Circuits* (2014)

[**] D.J. Dumin *Oxide Reliability : A Summary of Silicon Oxide Wearout, Breakdown and Reliability* (2002)

SiC MOSFET Oxide System: Si / SiO2 / SiC





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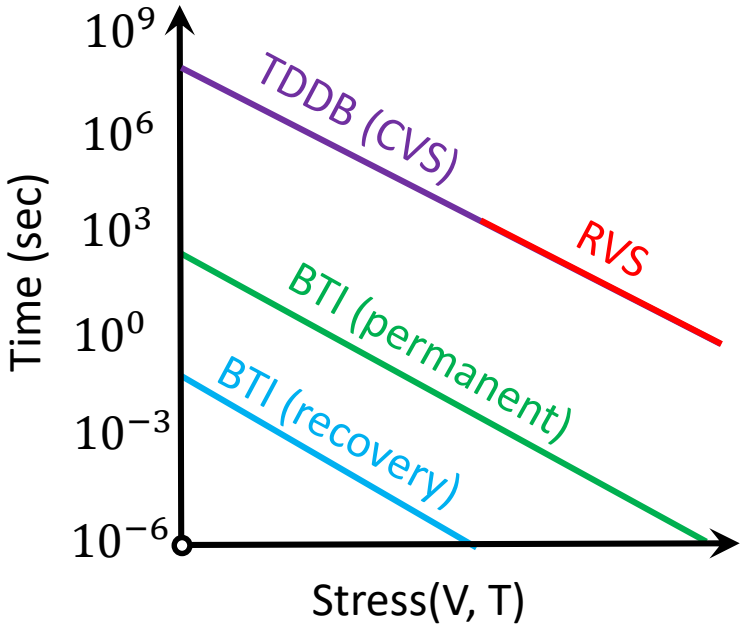
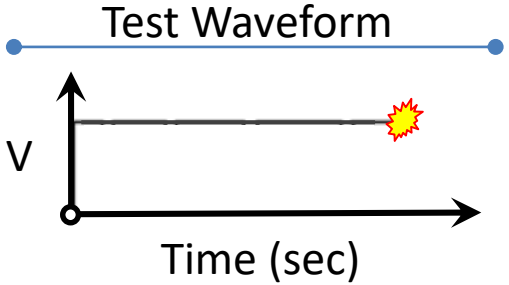
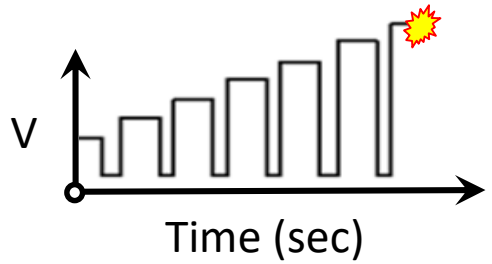
Gate Oxide SiO2 / SiC Time Scales



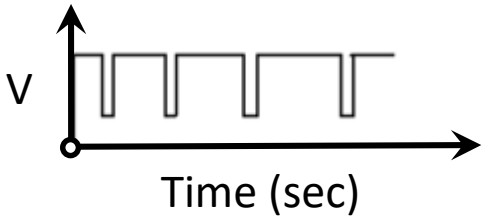
Long Time Scale:
CVS TDDB



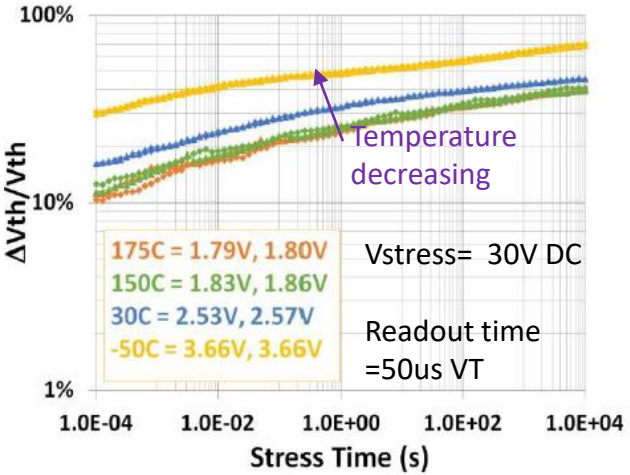
Medium Time Scale:
RVS TDDB



Short Time scale:
BTI (MSM)



Bias Temperature Instability (BTI) SiC MOSFET for various voltage waveforms (DC & Pulsed AC)



- Data shows complex interplay between stress and readout times and the parametric drift
  - Fast trapping appears to have a “negative activation” – hypothesis: very fast emission relative to measurement scale

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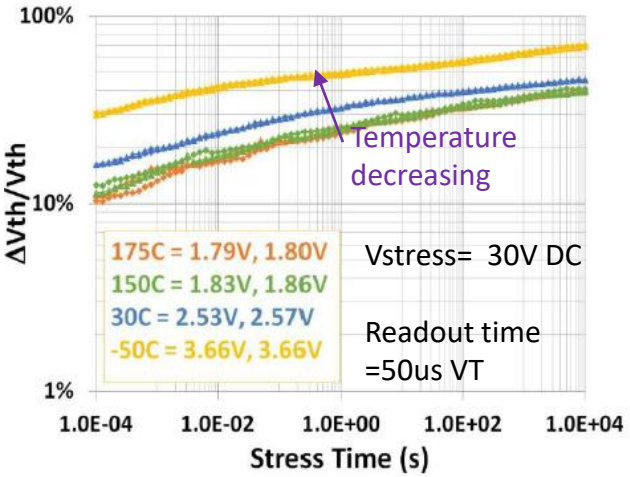

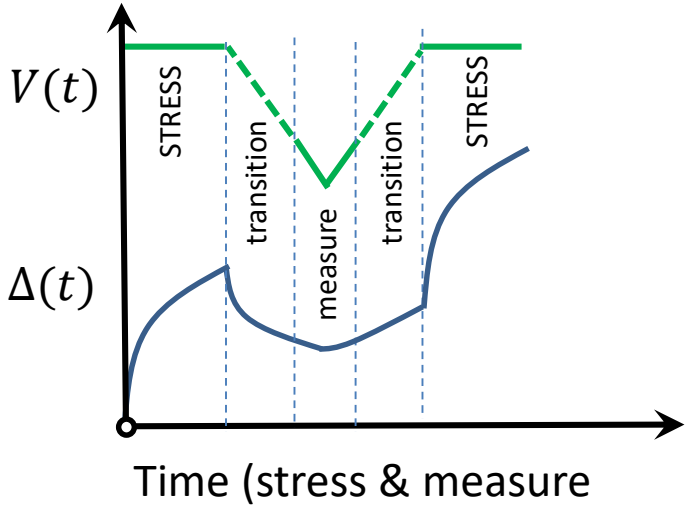

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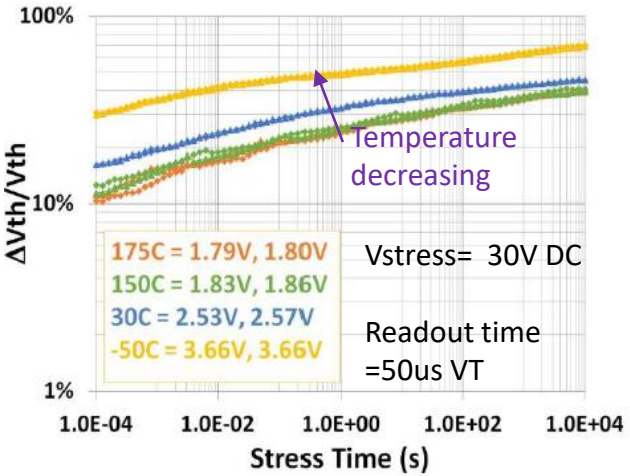

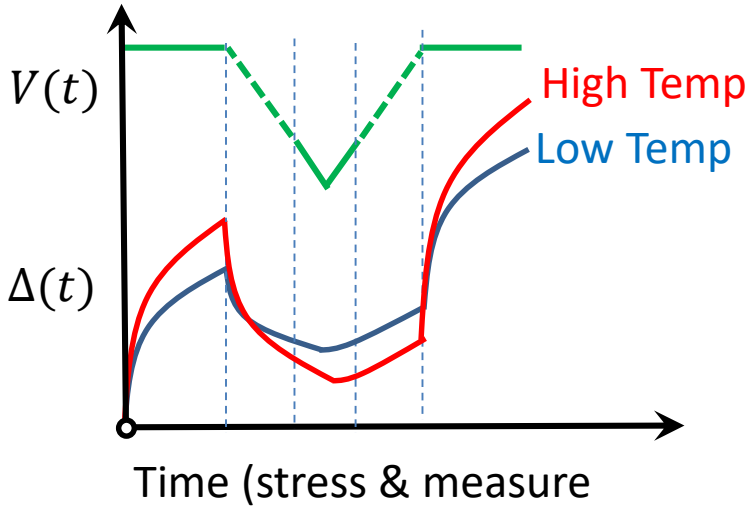

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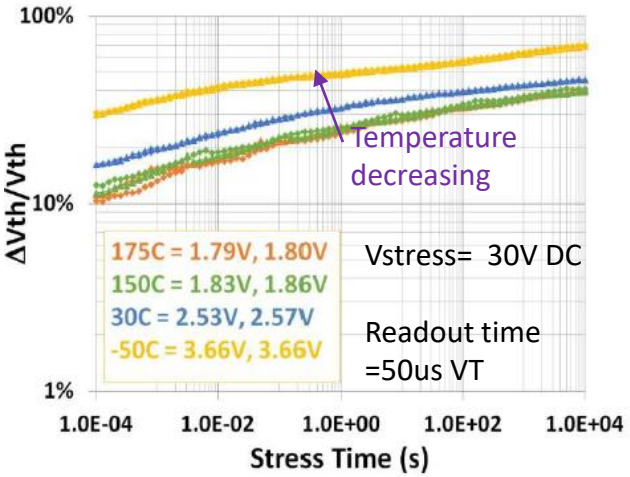

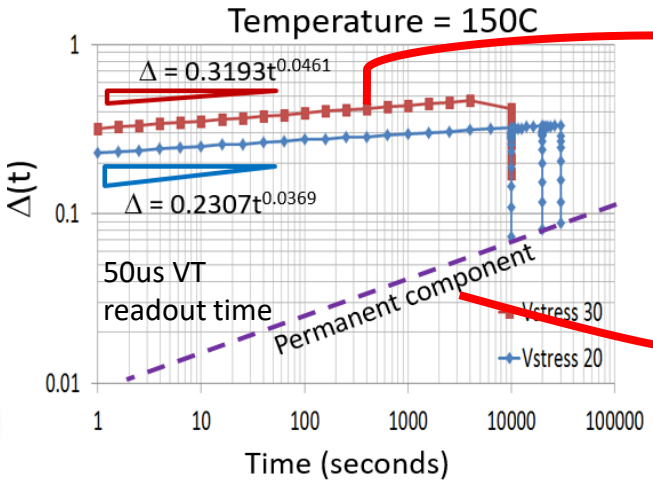

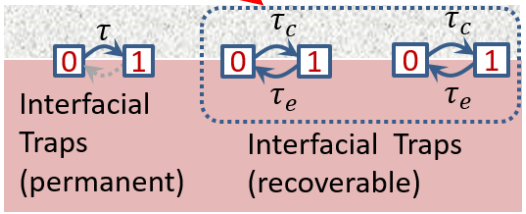

- Data shows complex interplay between stress and readout times and the parametric drift
  - Two very well separated time scales → some traps are filled quickly and recover and others more slowly and remain

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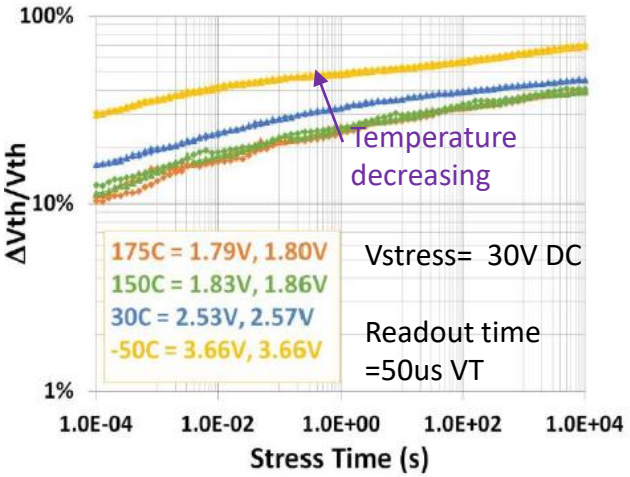

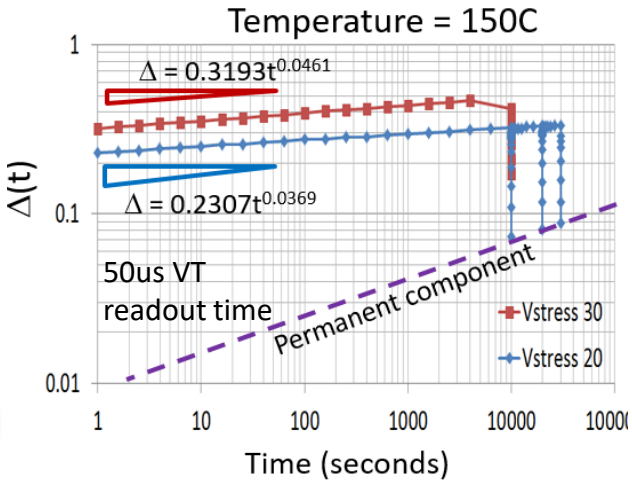

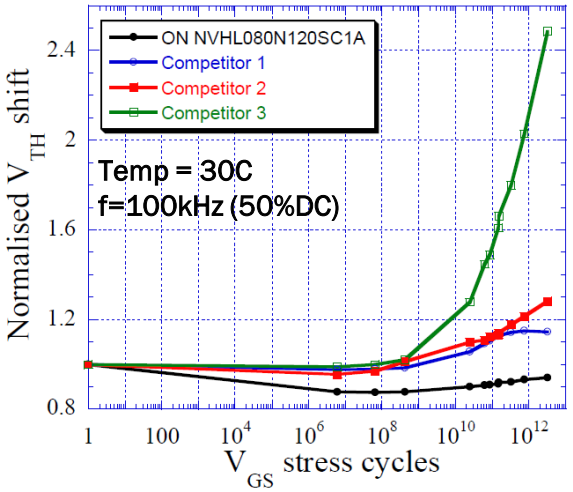

- Data shows complex interplay between stress and readout times and the parametric drift
  - For AC stress → less evidence of trapping
  - may depend on the details of the device and processing

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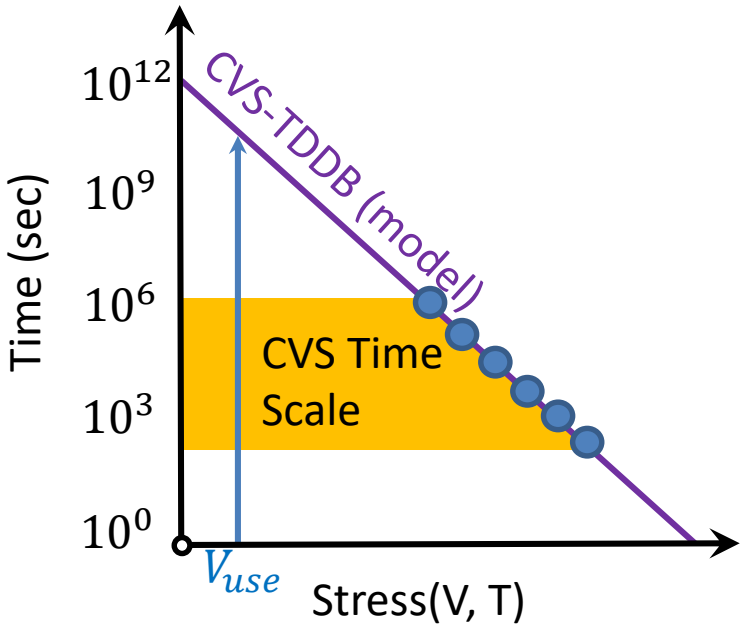
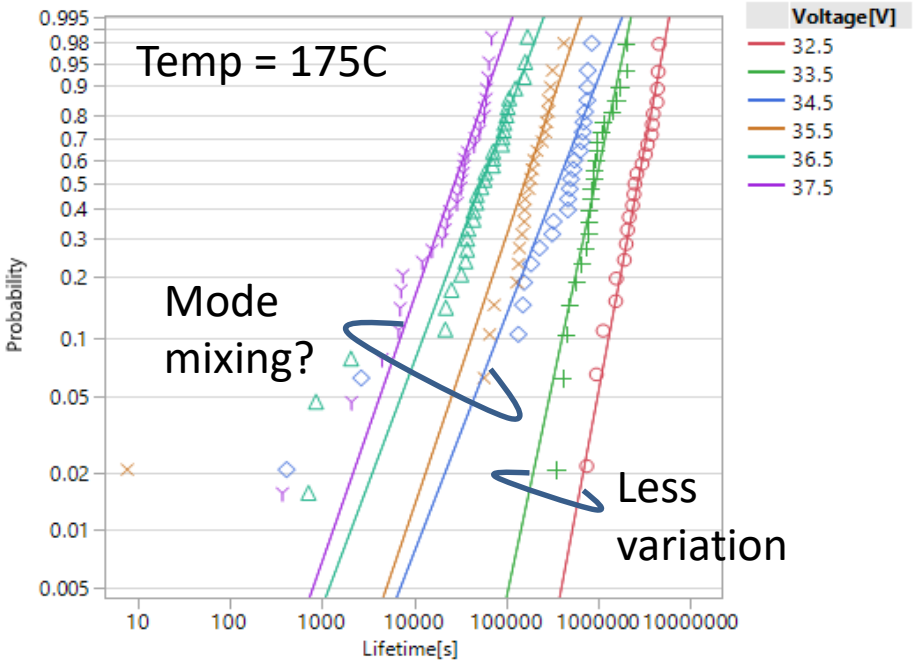
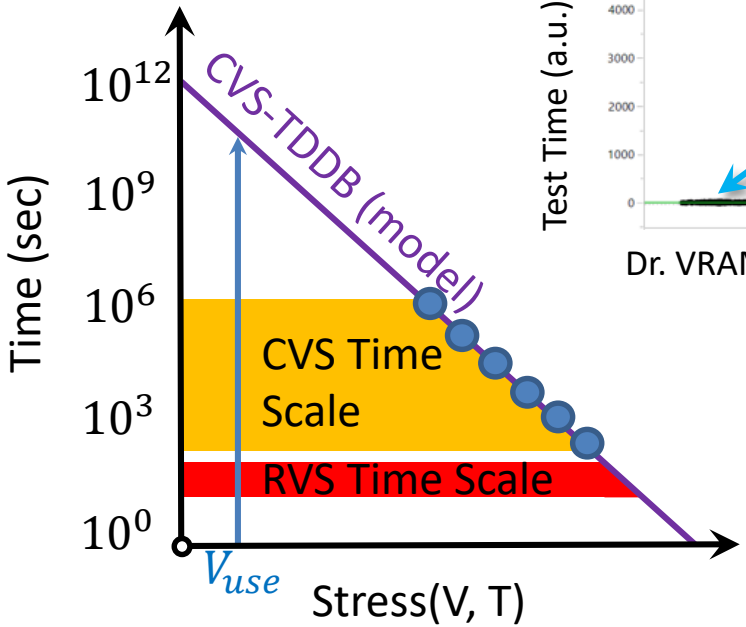
SiC MOSFET TDDB (CVS) @ 175C

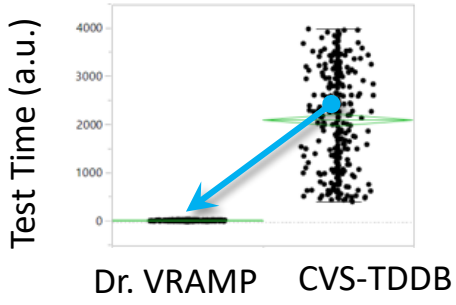




- TDDB model extracted from moderately accelerated voltages at moderate temperature (175C)
- Low voltage data is well behaved, however, at larger voltages there is some evidence of *increased variability* → evidence of *mode mixing*?

SiC MOSFET Dr.VRAMP (RVS)





To Transform CVS to RVS[*]

TDDB Model: $R_{CVS}(t/\tau(V))$

Integrate over changing CVS time scale: $R_{CVS}(\int dt/\tau(V(t)))$

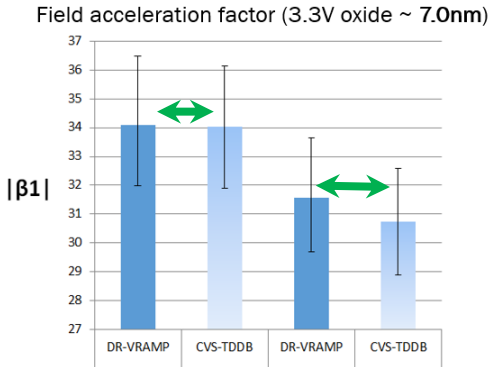
Perform change of variables to get a new distribution $R_{RVS}(V)$

[*] W. Nelson "Accelerated Testing" (1990)

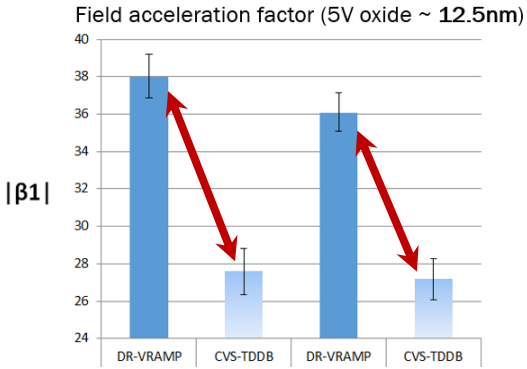
- TDDB timescales can be accelerated further using a ramped voltage stress (RVS)
- Since the model remains "2-dimensional" we will need at least 2 ramp rates to perform a regression to obtain the full AFT model
- Hence we have **D**ual **R**amp **V**oltage-**Ramp** or "DR. VRAMP"

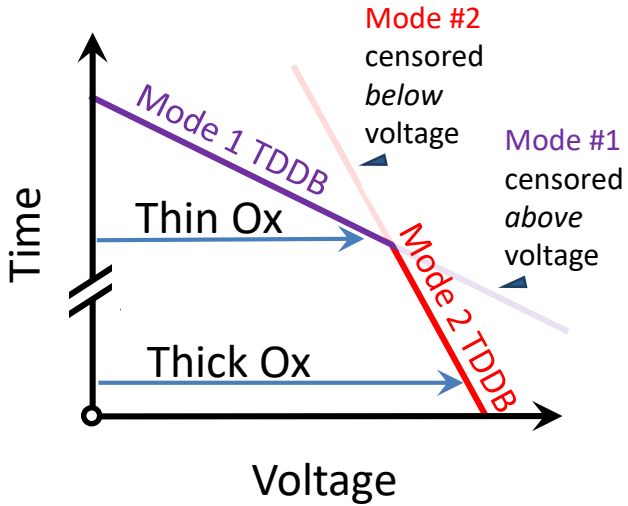
Dr. VRAMP Initial Proof of Concept : Si / SiO2 / Si System

7nm oxide shows TDDB slope
=Dr. VRAMP slope



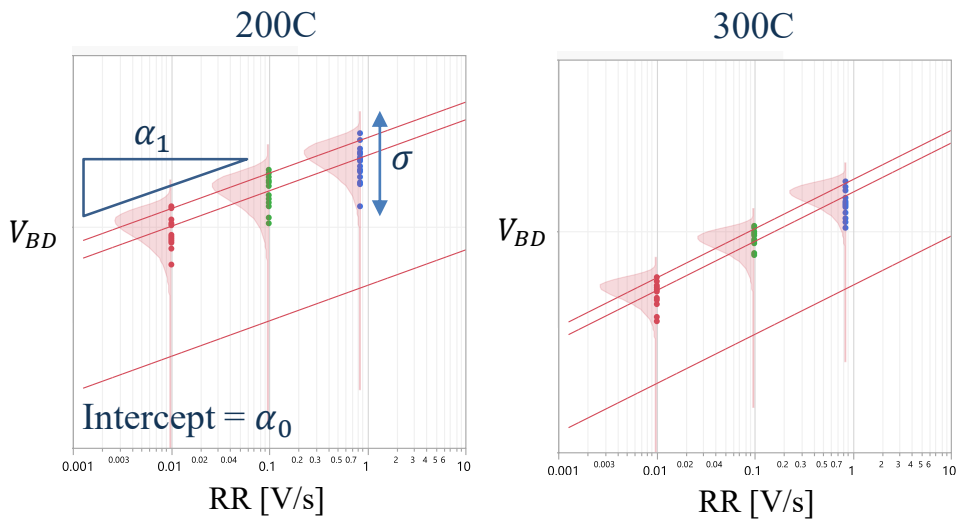
12.5nm oxide shows TDDB slope
is less than Dr. VRAMP slope





- Result : thin oxides → same acceleration model between TDDB / Dr. VRAMP,
- However: thicker oxides show consistently higher slope factor for Dr. VRAMP
- Hypothesis : 2 Modes of TDDB, one low voltage and one high voltage
- Risk is the “over prediction” reliability from the Dr. VRAMP test, without modification … can we make it work?

Results For Si / SiO2 / SiC MOSFET Dr.VRAMP (RVS)



regression

Obtain RVS model estimates: $V_{BD} = \alpha_0 + \alpha_1 RR$

	Temp [C]	Parameter	Estimate	L95	U95	Parameter	Estimate	L95	U95
DR VRAMP Regression	200	alpha1	0.0200	0.0171	0.0230	alpha0	3.79	3.78	3.80
	250	alpha1	0.0231	0.0204	0.0258	alpha0	3.77	3.76	3.78
	300	alpha1	0.0278	0.0254	0.0301	alpha0	3.75	3.74	3.75
	350	alpha1	0.0282	0.0237	0.0327	alpha0	3.71	3.69	3.72

Apply conversion formulas [*]

$\beta_0 = \alpha_0/\alpha_1 + \log \alpha_1$

$\beta_1 = 1 - 1/\alpha_1$

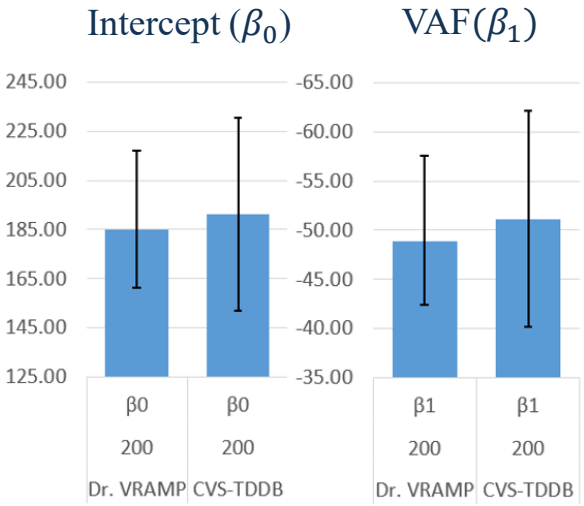
Obtain TDDB model estimates: $\log TTF = \beta_0 + \beta_1 \log V$

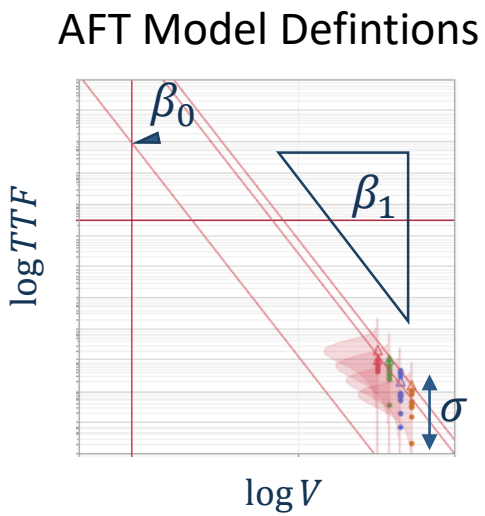
	Temp [C]	Parameter	Estimate	L95	U95	Parameter	Estimate	L95	U95
TDDB Estimates	200	beta1	-48.88	-57.53	-42.45	beta0	185.10	217.22	161.27
	250	beta1	-42.34	-48.05	-37.82	beta0	159.50	180.48	142.90
	300	beta1	-35.02	-38.34	-32.22	beta0	131.33	143.39	121.16
	350	beta1	-34.45	-41.13	-29.60	beta0	127.86	151.92	110.41

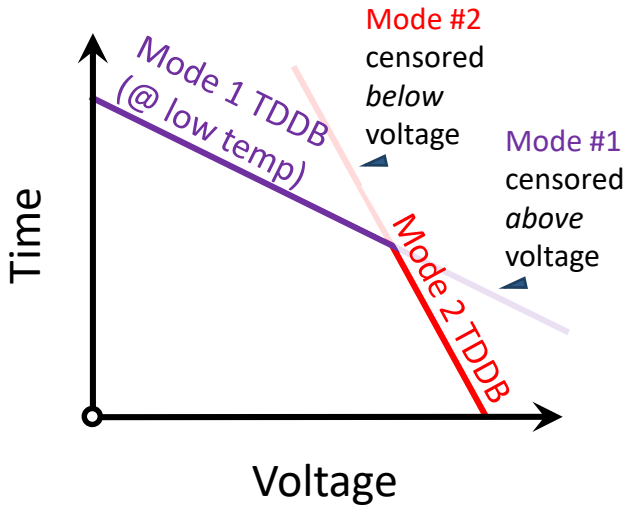
- Dr. VRAMP (RVS) data collected to compare with TDDB
- Several temperatures used : temperature acceleration for test time reduction and perhaps better alignment between TDDB and RVS
- Lower voltage to breakdown → less likelihood of competing risks at higher accelerations

[*] See appendix for derivations

Results Summary : SiC MOSFET Dr.VRAMP (RVS) vs. CVS-TDDB @ 200C







- Result: High temperature data shows perfect alignment between CVS-TDDB and Dr. VRAMP estimates for acceleration model
- Conclusion: Additional accelerating factor of temperature allows for lower voltage stress to breakdown
- Theory: Increasing temperature shifting the failure from the oxide boundary to the bulk. → hypothesis is encouraged by measured changes in transport.

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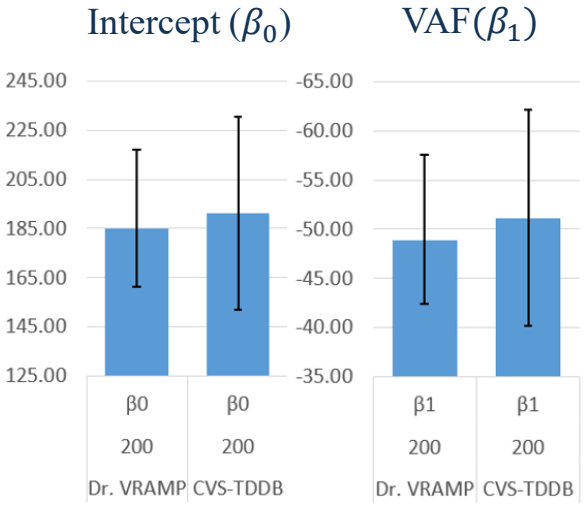

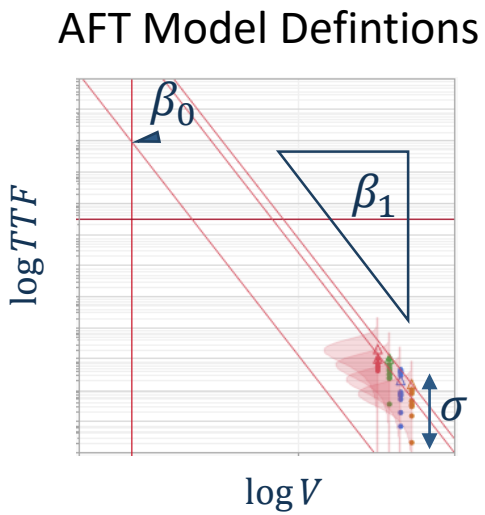

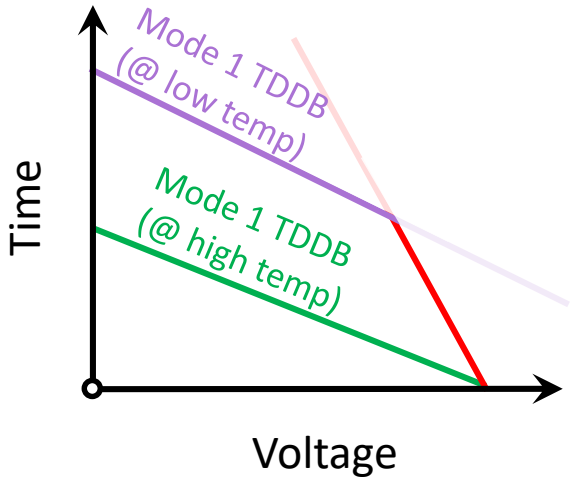

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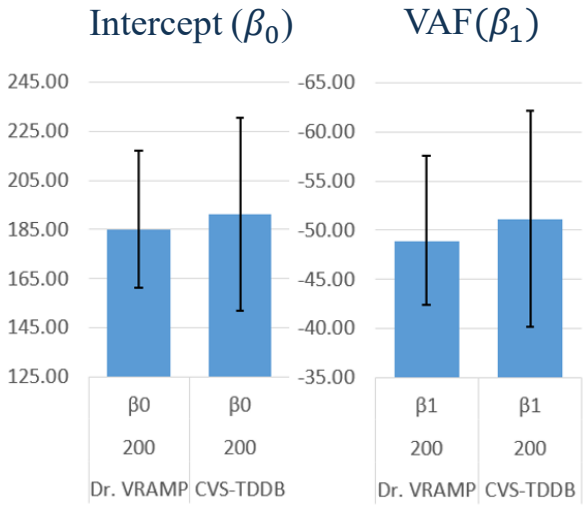

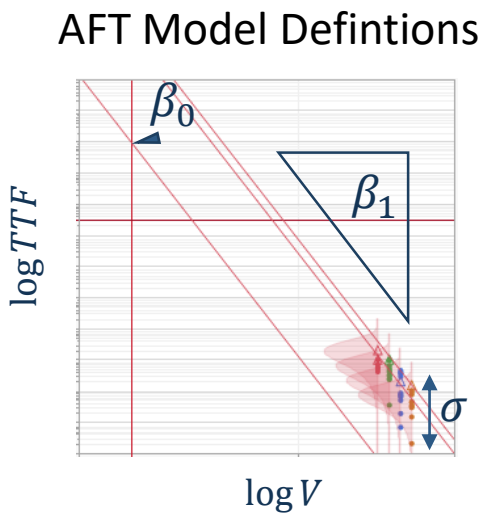

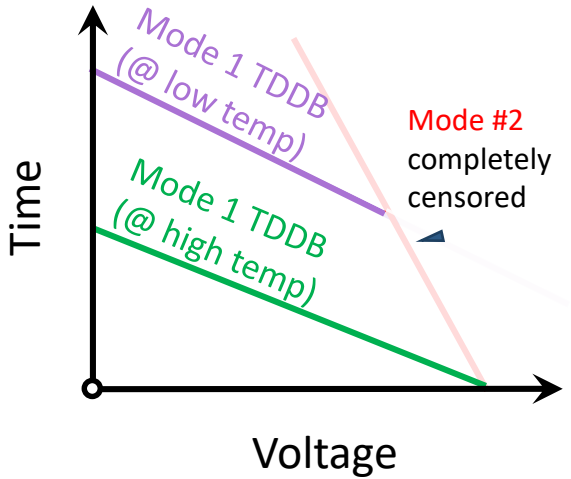

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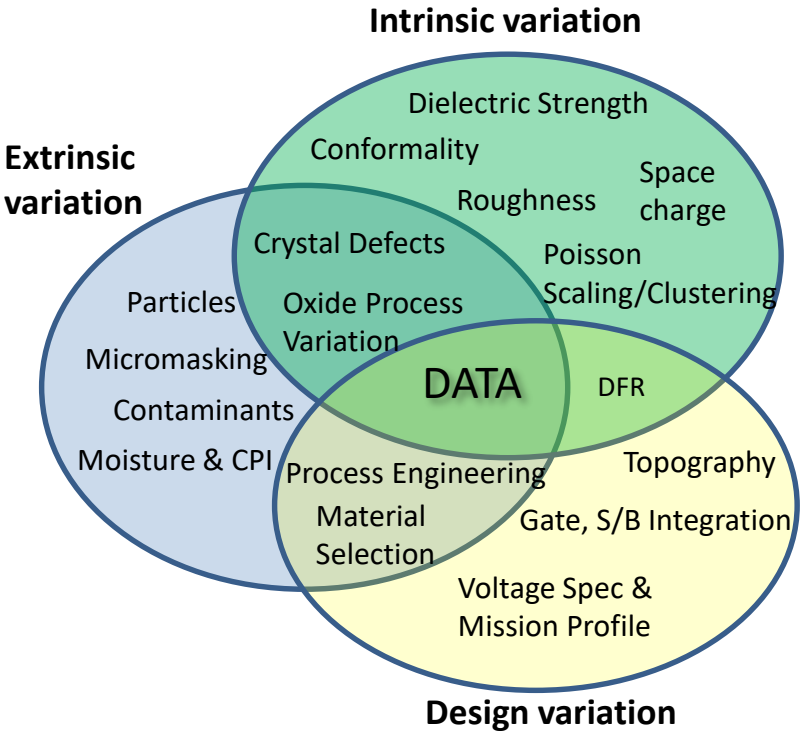
Discussion : Sources of Variation & Impact

SiC MOSFET – Possible Variation Types



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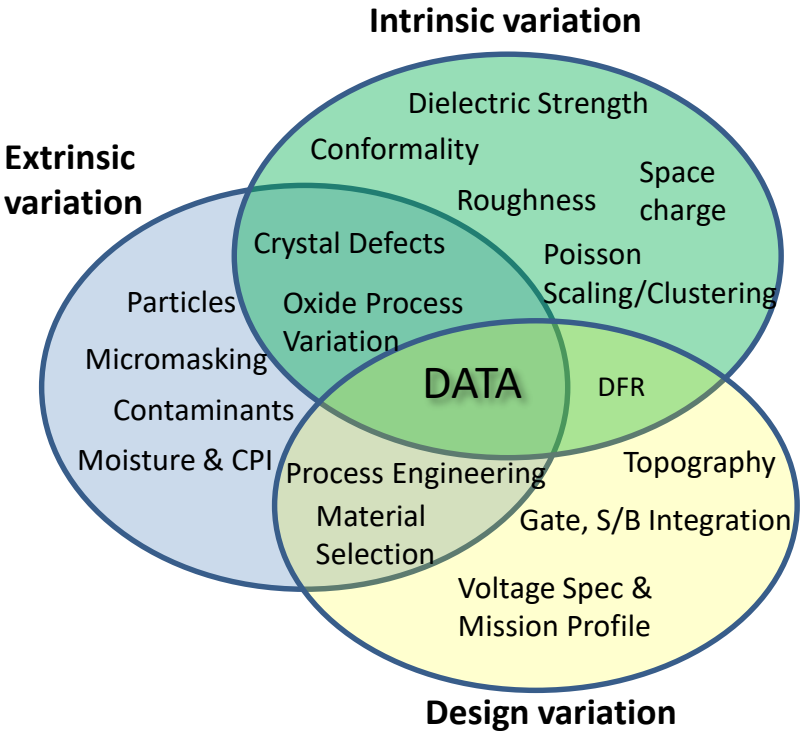
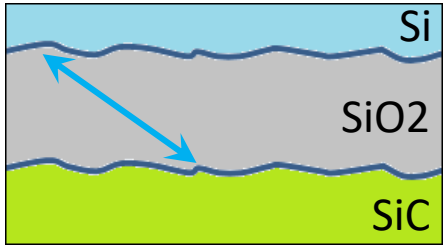
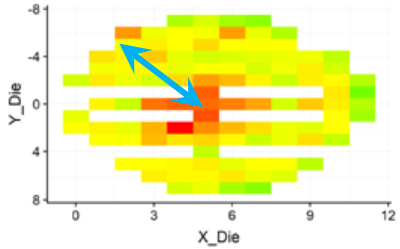


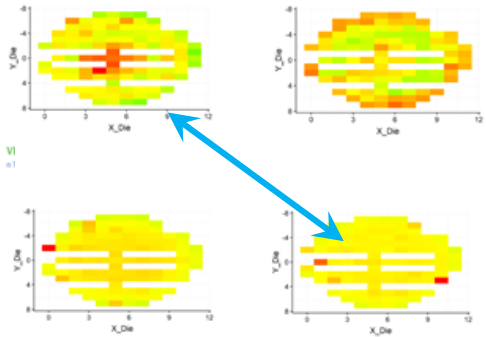
Local Variation: Within DUT



Global Variation : DUT to DUT

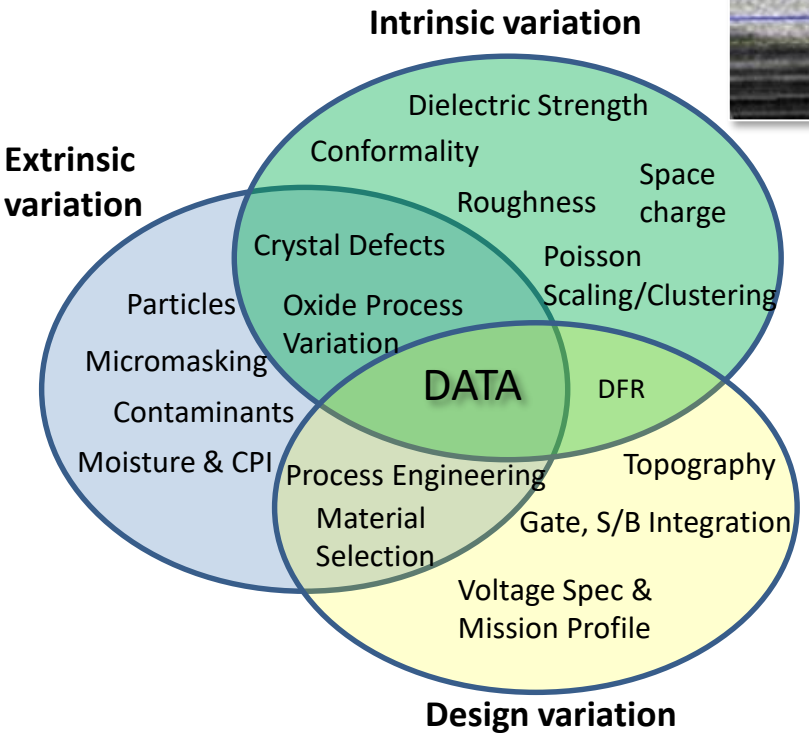


Global Variation : Waf-to-Waf

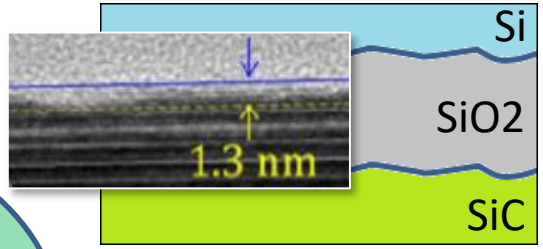


Discussion : Sources of Variation & Impact

SiC MOSFET – Possible Variation Types



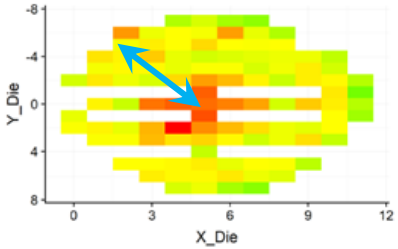
Local Variation: Within DUT



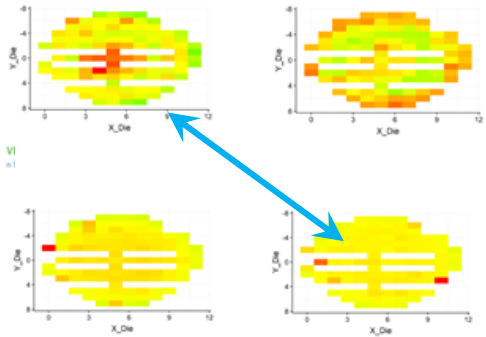
In general, Impact of variation depends on scale

If there is symmetry across scales, local var ~ global var

Global Variation : DUT to DUT



Global Variation : Waf-to-Waf

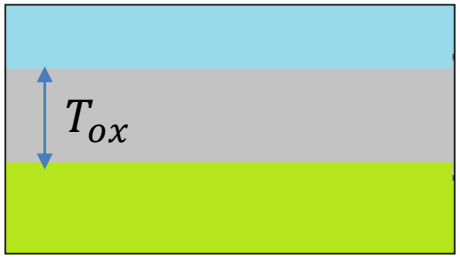


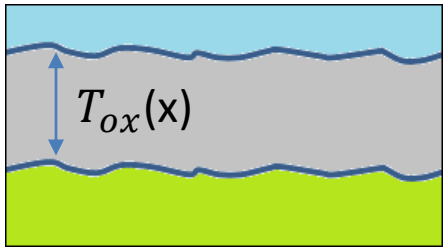
Discussion : Sources of Variation & Impact

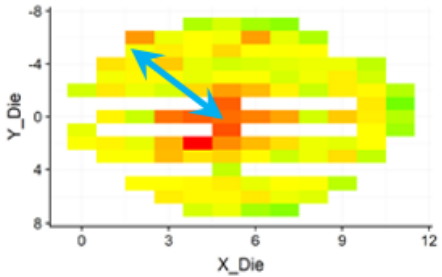
"Perfect Variation"
Weibull TTF
$\beta \propto T_{ox}$

Sum over local variation
"roughness"
$\beta < T_{ox}$

Sum over global variation
$\beta \ll T_{ox}$
→ multimodal?







$R \sim Weibull$

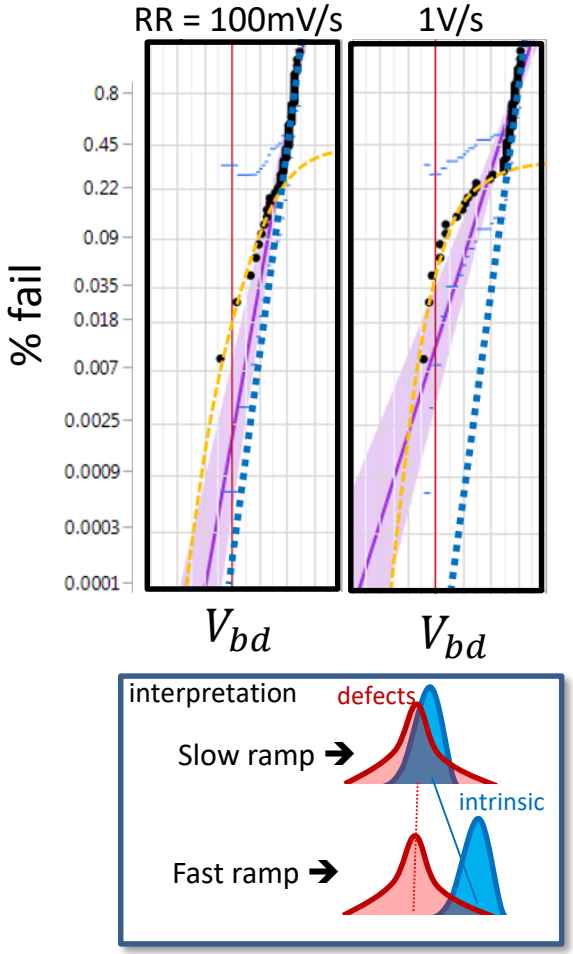
$R_{eff} \sim \langle R \rangle_{Tox}$

$R_{eff} \sim \langle \langle R \rangle_{Tox} \rangle$

- All samples may be considered within specification
- Each summation leads to an increase in variance
- Why not "group" the data? Decrease in MSE → inefficient use of data

Discussion : Sources of Variation & Impact

- Limited sample size in many cases due to cost & time constraint
  - Use all data available to decrease MSE and make the most of the data
- Motivation to increase sample size → improve understanding of defects
  - Defects are often understood by “what they are not”
  - i.e. a better understanding of the intrinsic variability improves the detectability of defects … and vice versa.
  - Larger sample size, using Dr. VRAMP enables multi-modal analysis in a reasonable time-frame
- Key motivation: safety margin
  - Better characterization leads to improved safety margins for the application



Conclusions and Outlook

- SiC Gate Oxide reliability characterization is a matter of capturing a wide variety of time scales and their impact:
  - Performance changes to breakdown
- These time-constants can be understood by using BTI, CVS and RVS
  - Some time-constants are rather swift and require special test methods (e.g. BTI)
  - Other time constants require using the principle of acceleration to reduce them to a practical test time (CVS)
  - Additional acceleration can reduce CVS time-scales further and enable a fast systematic characterization of defect-driven vs intrinsic breakdown
- Variation is endemic to the system and must be taken into account to properly characterize the intrinsic behavior while making economic use of sample data

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