A History and Prospective View of Integrated Inductors

(A MEMS Perspective)

Mark G. Allen

Moore Professor of Electrical and Systems Engineering; and
Director, Singh Center for Nanotechnology
University of Pennsylvania

Outline

- Lithographic magnetics – the initial applications
- Integrated inductors and Moore's Law
- The advent of MEMS and fabrication technologies for three-dimensional structures
- Scaling and frequency – the need for multiscale inductor cores
- An approach to the future?

Early Integrated Magnetics: Thin Film Tape Heads

United States Patent Office — 3,344,237 — Patented Sept. 26, 1967

(filed 1961)

1

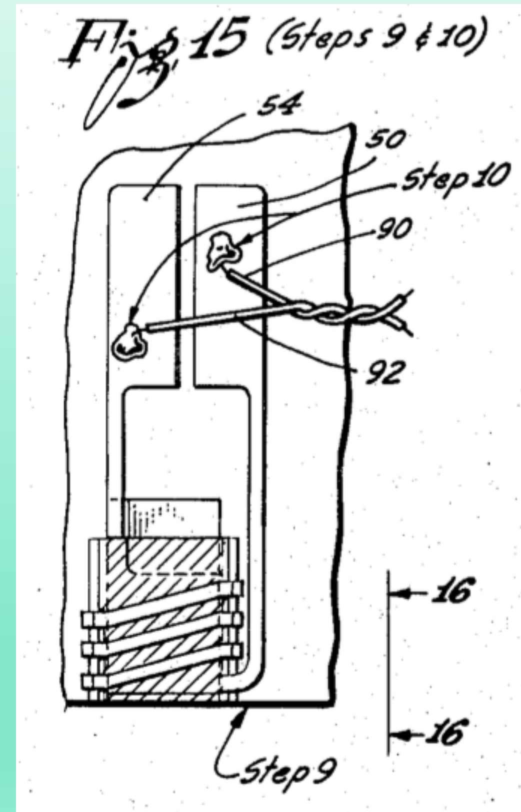
3,344,237
DEPOSITED FILM TRANSDUCING APPARATUS AND METHOD OF PRODUCING THE APPARATUS
David Paul Gregg, Culver City, Calif., assignor to Minnesota Mining and Manufacturing Company, St. Paul, Minn., a corporation of Delaware
Filed Apr. 19, 1961, Ser. No. 104,071
16 Claims. (Cl. 179—100.2)

2

duced in comparison to the current required in the heads now in use.

Another advantage of the head constituting this invention results from the use of only two laminations to form the magnetic circuit. Furthermore, each of these laminations is formed from a thin film of magnetic material. The laminations are disposed in a direction transverse to the direction of movement of the medium such as the tape rather than in the direction of movement of the tape, as in the heads now in use. All of these factors are in-

…a magnetic head for providing a transducing action between the recording of magnetic information on magnetic medium such as a tape and the production of electrical signals… The invention is particularly concerned with heads produced by vacuum deposition and electroplating of different materials…



Inductors and Moore's Law

- Transistors* and capacitors can be fabricated using planar processes; many inductor geometries require more complex three-dimensional processes
- Magnetics require a specialized set of permeable core materials and high current conductors
- Magnetics scale poorly**
  - The storage of magnetic energy scales as the volume $[s]^3$
  - The storage of electrostatic energy scales as area $[s]^2$
  - Magnetics dominate the 'big' world, but what about the small scale?

➢ We have not seen a Moore's Law for inductors! (and therefore for integrated power supplies)

*FinFETs and other state-of-the-art transistors are no longer strictly planar   **See, e.g., W. Trimmer, *Sensors and Actuators* **19**, 267-287 (1989)

The advent of Microelectromechanical Systems (MEMS) in the 1980s spurred a vast expansion in new microfabrication technologies

A definition of MEMS (there are many): The use of microfabrication techniques to create structures, sensors, and actuators in silicon and other materials, potentially in addition to electronic devices

Nathanson, 1967

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-14, NO. 3, MARCH 1967

The Resonant Gate Transistor

HARVEY C. NATHANSON, MEMBER, IEEE, WIL
ROBERT A. WICKSTROM, AND JOHN RA

Abstract—A device is described which permits high-Q frequency selection to be incorporated into silicon integrated circuits. It is essentially an electrostatically excited *tuning fork* employing field-effect transistor "readout." The device, which is called the resonant gate transistor (RGT), can be batch-fabricated in a manner consistent with silicon technology. Experimental RGT's with gold vibrating beams operating in the frequency range 1 kHz $< f_0 <$ 100 kHz are described. As an example of size, a 5-kHz device is about 0.1 mm long (0.040 inch). Experimental units possessing Q's as high as 500 and overall input-output voltage gain approaching +10 dB have been constructed.

The mechanical and electrical operation of the RGT is analyzed. Expressions are derived for both the beam and the detector characteristic voltage, the device center frequency, as well as the device gain and gain-stability product. A batch-fabrication procedure for the RGT is demonstrated and theory and experiment corroborated. Both single- and multiple-pole pair band pass filters are fabricated and discussed. Temperature coefficients of frequency as low as 90–150 ppm/°C for the finished batch-fabricated device were

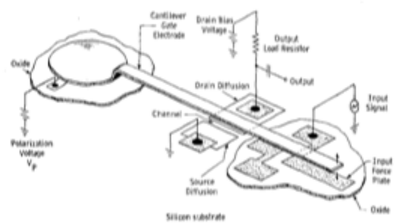
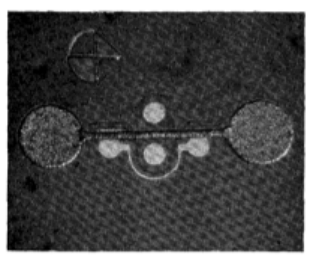


Fig. 1. Geometry and circuit connections of an RGT with a C-F resonant beam.



Petersen, 1982

PROCEEDINGS OF THE IEEE, VOL. 70, NO. 5, MAY 1982

Silicon as a Mechanical Material

KURT E. PETERSEN, MEMBER, IEEE

Abstract—Single-crystal silicon is being increasingly employed in a variety of new commercial products not because of its well-established electronic properties, but rather because of its excellent mechanical properties. In addition, recent trends in the engineering literature indicate a growing interest in the use of silicon as a mechanical material with the ultimate goal of developing a broad range of inexpensive, batch-fabricated, high-performance sensors and transducers which are easily interfaced with the rapidly proliferating microprocessor. This review describes the advantages of employing silicon as a mechanical material, the relevant mechanical characteristics of silicon, and the processing techniques which are specific to micromechanical structures. Finally, the potentials of this new technology are illustrated by numerous detailed examples from the literature. It is clear that silicon will continue to be aggressively exploited in a wide variety of mechanical applications complementary to its traditional role as an electronic material. Furthermore, these multidisciplinary uses of silicon will significantly alter the way we think about all types of miniature mechanical devices and components.

miniaturized mechanical devices and components must be integrated or interfaced with electronics such as the examples given above.

The continuing development of silicon micromechanical applications is only one aspect of the current technical drive toward miniaturization which is being pursued over a wide front in many diverse engineering disciplines. Certainly silicon microelectronics continues to be the most obvious success in the ongoing pursuit of miniaturization. Four factors have played crucial roles in this phenomenal success story: 1) the active material, silicon, is abundant, inexpensive, and can now be produced and processed controllably to unparalleled standards of purity and perfection; 2) silicon processing itself is based on very thin deposited films which are highly amenable to miniaturization; 3) definition and reproduction of the device shapes and patterns are performed using photographic

Lithographically-Defined Micromotors – Electrostatic and Magnetic

Sensors and Actuators, 20 (1989) 41–47

1989

IC-processed Electrostatic Micromotors

LONG-SHEN FAN, YU-CHONG TAI and RICHARD S. MULLER

Berkeley Sensor and Actuator Center, Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, CA 94720 (U.S.A.)

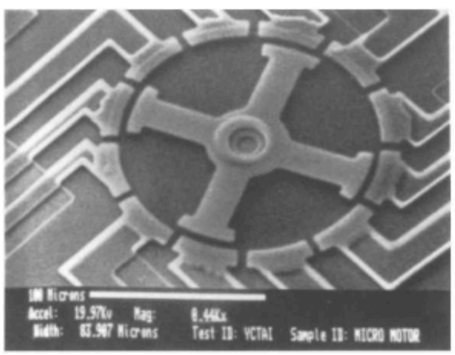


Fig. 9. SEM photograph of a 12-stator, 4-rotor-pole micromotor. The gap between the stator and rotor is 6 μm.

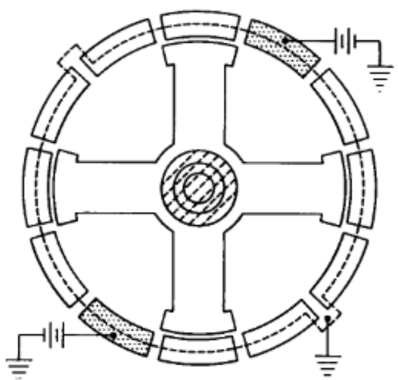


Fig. 11. Stator-pair drive configuration. Only a pair of the stators is biased and the ground plane is grounded.

JOURNAL OF MICROELECTROMECHANICAL SYSTEMS, VOL. 2, NO. 4, DECEMBER 1993

1993

A Planar Variable Reluctance Magnetic Micromotor with Fully Integrated Stator and Coils

Chong H. Ahn, Yong J. Kim, and Mark G. Allen, *Member, IEEE*

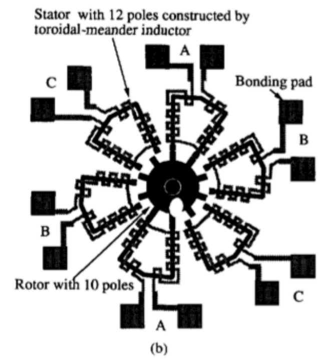


Fig. 4. Structure of conventional and modified variable reluctance motors. (a) Schematic diagram of the magnetic core of a conventional magnetic variable reluctance motor showing the yoke frame; (b) schematic diagram of modified planar variable reluctance magnetic motor fabricated in this research. The structure consists of 12 stator poles and 10 rotor poles in three phases. Each magnetic core is separated from the others.

Early '90s: Many groups began applying these 'new' MEMS technologies to inductor fabrication – and began looking towards full integration

APEC 1994

A Comparison of Two Micromachined Inductors (Bar-Type and Meander-Type) For Fully Integrated Boost DC/DC Power Converters

Chong H. Ahn and Mark G. Allen
School of Electrical and Computer Engineering
Microelectronics Research Center
Georgia Institute of Technology
Atlanta, GA 30332-0250 U.S.A.

Abstract **- Two micromachined integrated inductors (bar-type and meander-type) are realized on a silicon wafer by using modified, IC-compatible, multilevel metallization techniques. Efforts are made to minimize both the coil resistance and the magnetic reluctance by using thick electroplated conductors, cores, and vias. In the bar-type inductor, a 25 μm thick nickel-iron permalloy magnetic core bar is**

voltage of several tens of volts or more, which is higher than commonly available integrated circuit power supply levels.

Inductive-based switched DC/DC converters are composed of switching control circuits and flyback inductive components. In realizing a DC/DC converter in an integrated fashion, integrated circuits for the switching function are already feasible; however, few planar integrated

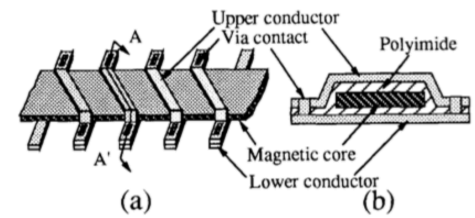


Fig. 1. Schematic diagram of the planar bar-type inductive component: (a) schematic view; (b) A-A' cut view.

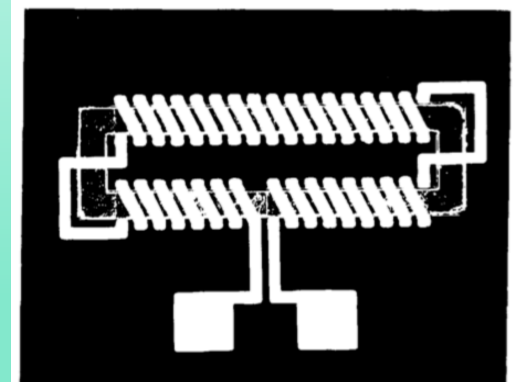


Fig. 2. Photomicrograph of the fabricated bar-type inductor.

Inductors and Moore's Law

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How can we address magnetics scaling in switching converters?

wikipedia.com

How can I get (a lot of) energy from one point to another?

Strategy 1 – use a big bucket; or
Strategy 2 – run really fast

In a switching converter, in general, as the switching frequency *increases*, the required size of the energy storage elements (e.g., inductors) *decreases*

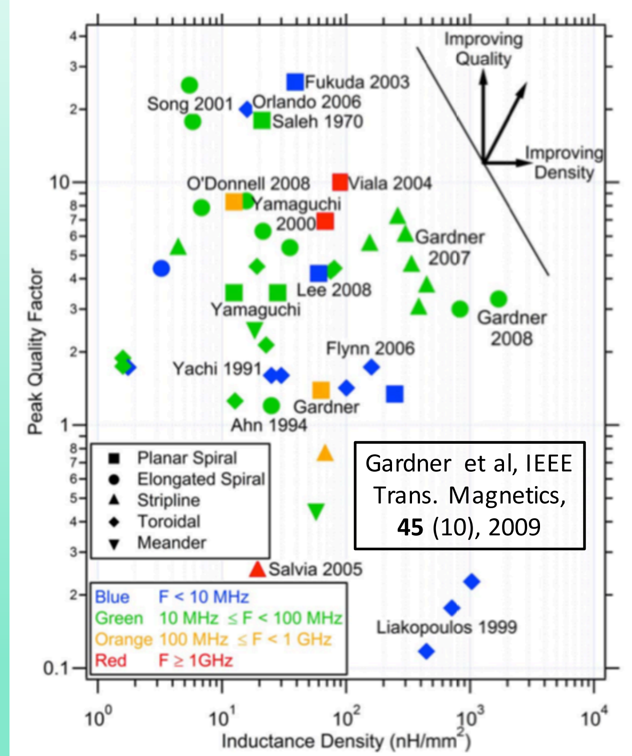

Fig. 1. Graph of inductance density versus peak Q-factors of integrated inductors on Si substrates from published on-chip inductor measurements. The colors represent the frequency of the peak Q-factor.

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➢ Can we have a Moore's Law for integrated power supplies?

*FinFETs and other state-of-the-art transistors are no longer strictly planar

See, e.g., Trimmer, W., *Sensors and Actuators* **19, 267-287 (1989)

The Power Supply In a Package/ Power Supply On a Chip

APEC 2010

Technology Roadmapping for Power Supply in Package (PSiP) and Power Supply on Chip (PwrSoC)

Raymond Foley[1], Finbarr Waldron[2], John Slowey[1], Arnold Alderman[3], Brian Narveson[4] and Sean Cian Ó'Mathúna[2]

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California, USA

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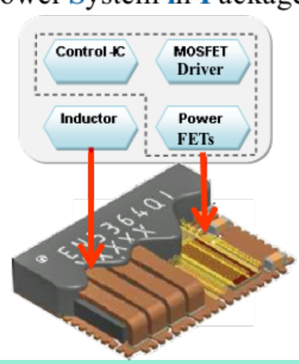
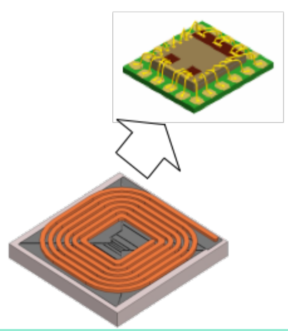
PSiP:

Power System in Package



PwrSoC:

Power System on Chip



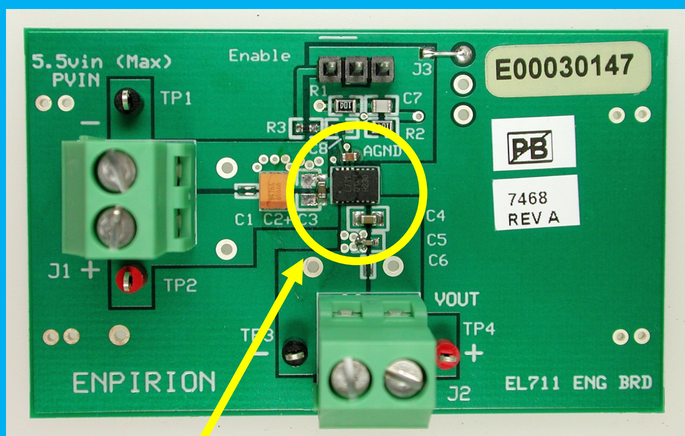
From the results of the analysis carried out on the selected samples (and with reference to the findings of Phase I of this work), the authors consider future developments in this product technology over the medium term will be:

- A gradual reduction in footprint & size
- Significant improvements in current density
- A gradual downward trend in voltage ratings driven by ASICs, microprocessors, and FPGAs voltage requirements
- Pressure for enhanced efficiency or to maintain efficiency with greater density
- A steady increase in switching frequency up to ~ 10MHz
- No significant change in functionality
- A gradual decrease in cost /Amp
- A gradual increase in the use of higher-density assembly technologies (flip-chip)
- Greater use of over-molded lead frame based packaging

In the longer-term, higher levels of integration on chip will lead to the ready commercial availability of true Power-Supply-on-Chip products with very high levels of integration.

Emerging Power Supplies - In Package and On Chip

PwrSoC 2012



EL711 –
First PowerSoC DC-DC (1A) Converter

Where are we going from here?

Switches are getting better!

- Frequency of operation previously limited by stability and loss in the semiconductor switches
- Wide bandgap switches and new switching architectures are addressign this problem
- There is ‘room’ to operate reasonable power switches into the tens of MHz range and beyond

Integrated inductors still have limitations…

- Magnetic core losses increase with frequency
- ‘Thick’ cores still required for higher current applications
- Electrically conducting magnetic cores may suffer from eddy current losses
- Ferrite magnetic cores may suffer from reduced saturation flux density
- Air core devices may skirt these issues, but require even higher switching frequencies

One Approach: Multiscale Electrodeposited Lamination Technology

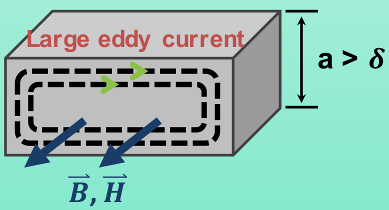
Skin depth: $\delta = \frac{1}{\sqrt{\pi \mu \sigma f}}$

μ : permeability [H/m]
σ : conductivity [1/Ωm]
f : frequency [Hz]

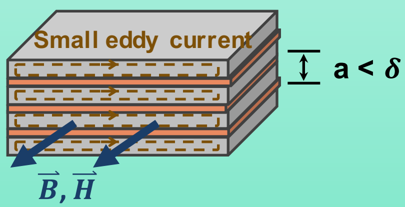
Need to simultaneously achieve two size scales

Large magnetic volume for high power (0.1-1 mm scale)

Suppressed eddy-currents at MHz frequency (1-10 um scale)

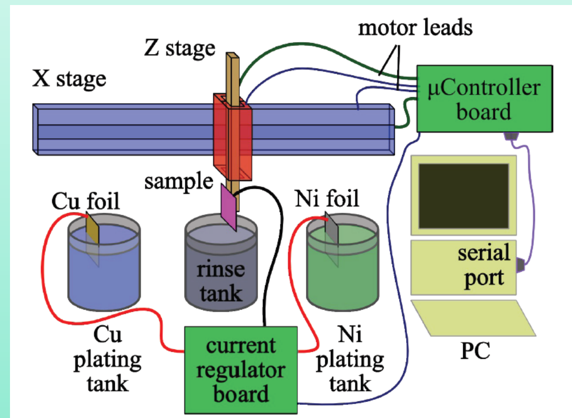


Non-laminated core

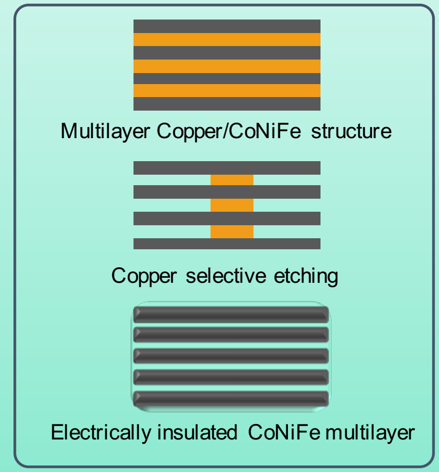


Laminated core

Magnetic material
Insulating material

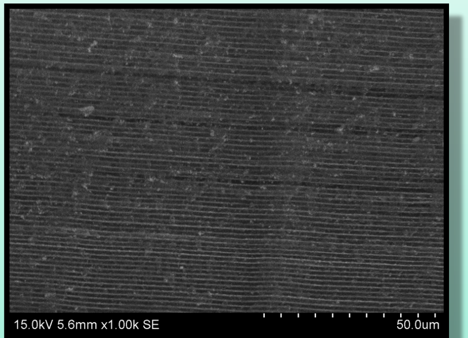


Automated multilayer electroplating setup

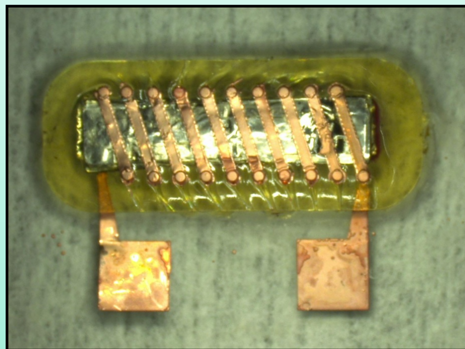


Laminated core fabrication

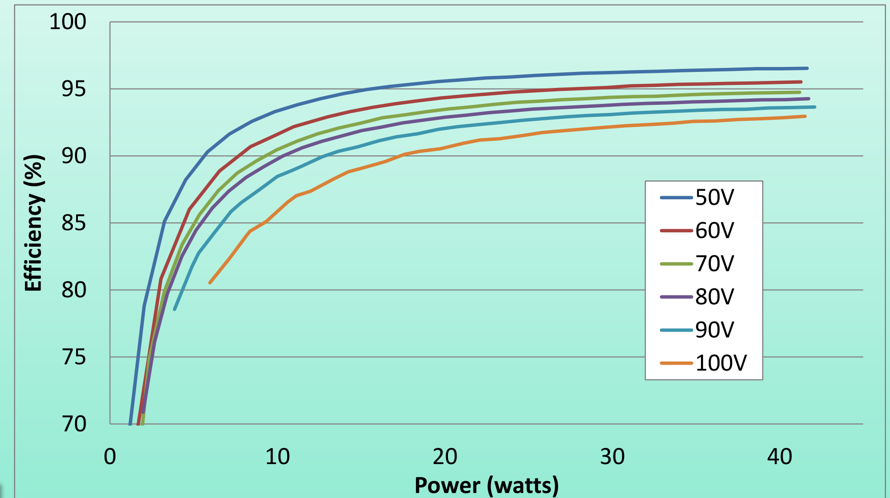
Electroplated Laminated Inductors

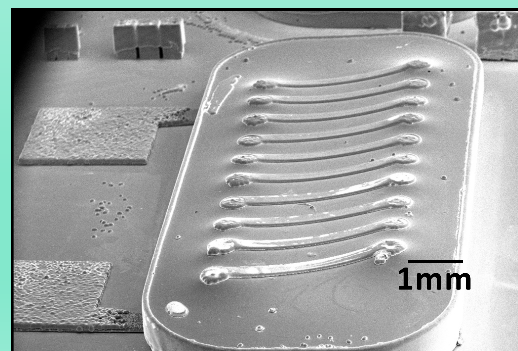


100-layer CoNiFe laminations with lamination thickness < 1 µm



microfabricated 10-turn inductor with CoNiFe multilayer core.





- Tested in power converter circuit at MIT
- Power converter operating condition
  - 50 - 100V input operation, 3-8 MHz switching frequency, 10-45 W output power
- Efficiency of 97% at 50V input, and 93% at 100V input

Toward Integrated Multilayer Electrodeposited Inductors on a Chip

- ✓ We can create the individual laminations in the thicknesses required
- ✓ We can create overall lamination stacks in the thicknesses required
- ✓ We can create integrated, lithographically defined windings
- But: we have this complicated interlayer etching process that is less compatible with CMOS fabrication. Can we get rid of it?
  - We need to have the interlamination material conducting so we can electrodeposit the next magnetic layer
  - We need to have the interlamination material insulating so we block eddy currents
  - Can we exploit a material with a conductivity that's between these two extremes to do both jobs?

We can create the core in a single electrodeposition sequence

2020

JOURNAL OF MICROELECTROMECHANICAL SYSTEMS, VOL. 29, NO. 6, DECEMBER 2020

Fully Additive Fabrication of Electrically Anisotropic Multilayer Materials Based on Sequential Electrodeposition

Michael Synodis, Jun Beom Pyo, *Graduate Student Member, IEEE*, Minsoo Kim, *Member, IEEE*, Hanju Oh, *Member, IEEE*, Xuan Wang, and Mark. G. Allen, *Fellow, IEEE*

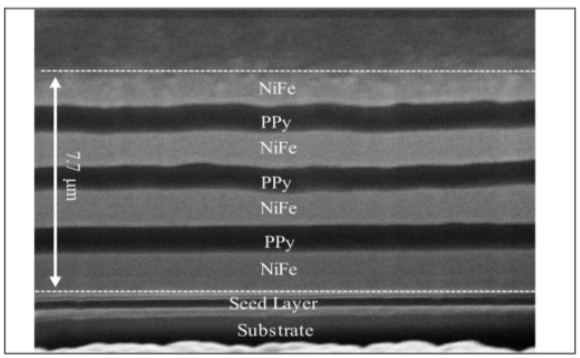


Fig. 7. SEM Cross-sectional image of 3 sets of laminations with an added top layer of NiFe.

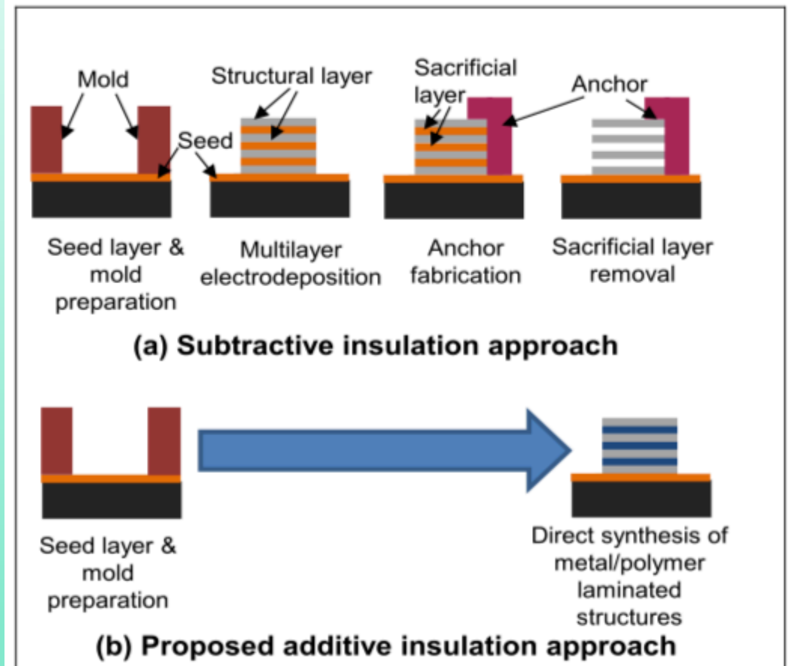
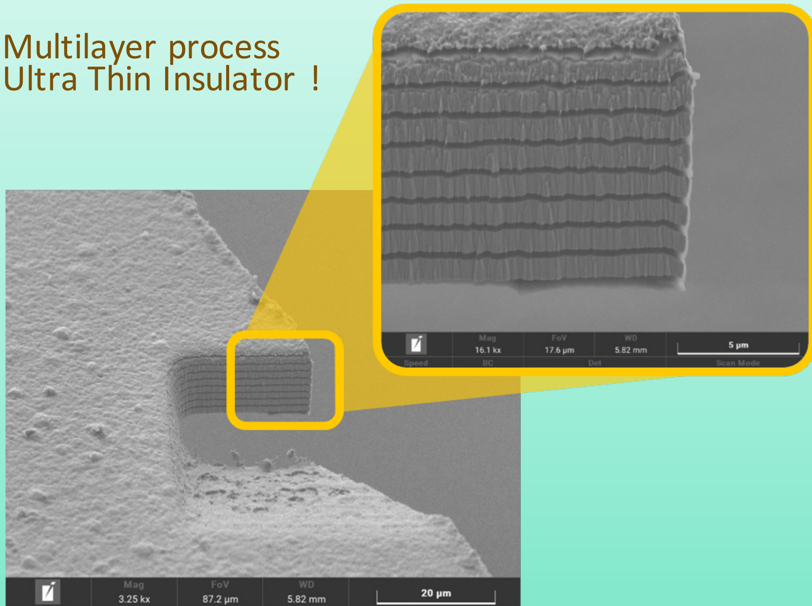


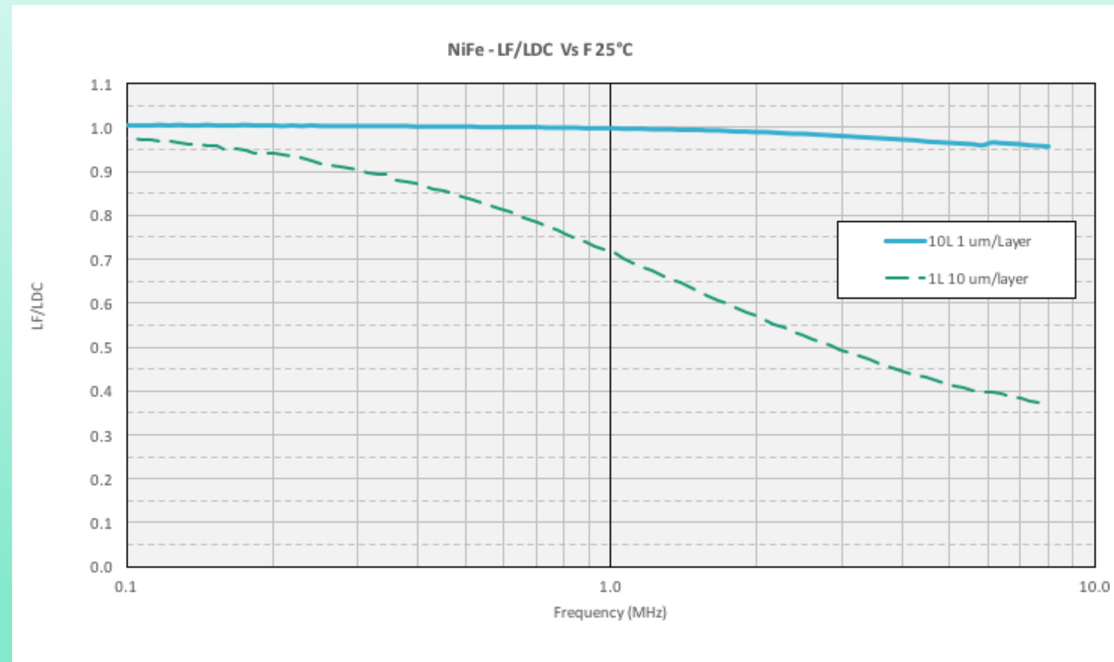
Fig. 1. Schematics of multilayer composite fabrication processes based on (a) subtractive interlayer insulation and (b) additive, polymeric insulation.

Inductor Commercialization

ENACHIP

Multilayer process
Ultra Thin Insulator !

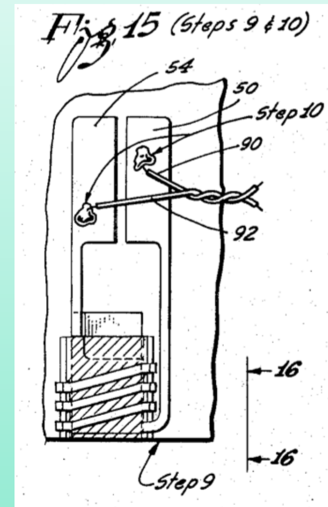




Inductors made from continuously electroplated multilayer cores possess preserved high frequency performance

Conclusions

- The time is right for an explosion of activity in PwrSoC
- A key enabler is the ability to integrate high power inductors
  - This resulted from many years of fabrication technology development!
- Multiple approaches to integrated inductors have reached technological maturity for commercialization
  - I focused on one approach in this talk, but there is a rich literature on this topic
- If you want to learn more, come join us for PwrSoC 2021 in Philadelphia this fall!



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- Xuan Wang

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- Matt Wilkowski

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*Author declares an equity position in EnaChip