

Industry Session 15: PwrSoC for Next-Gen Power

Si-IPD: Review of continuous improvements with regard to the new challenges in PwrSoC

Mohamed Mehdi Jatlaoui, Principal
Murata Integrated Passive Solutions
mohamed.jatlaoui@murata.com

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Outline

1- Introduction

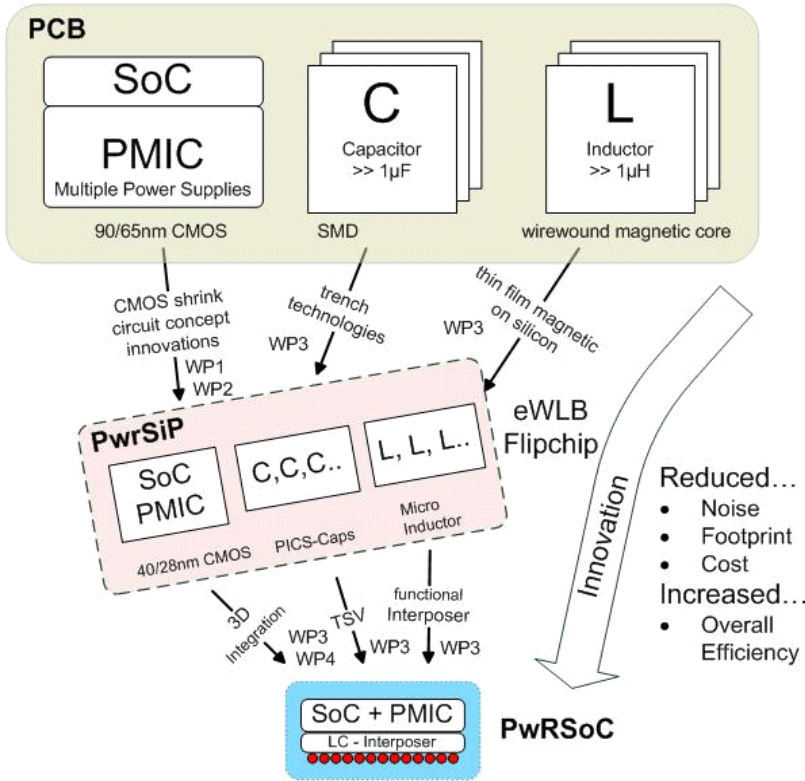
2- Silicon Capacitors technology

3- 3D Silicon capacitors for power applications

- PDN application (Mobile & HPC)
- LiDAR application (Automotive)

4- Summary

1- Introduction



- Major Drivers in power electronics
 - High efficiency
 - Cost-effective
 - High level of integration
- Innovations in:
 - Integrated power passives
 - Capacitors
 - Inductors
 - Nano CMOS Technologies
 - Advanced packaging

1- Capacitors technologies

Long Lifetime, Down Sizing

High Capacitance GRM Series
(2.5V~100V, ~220uF)

Polymer Electrolysis ECAS Series
(2.5V~25V, ~470uF)

EDLC DMF Series
(~1000mF, 4.2V)

Low ESL LLL/LLD Series
(~4.3uF, 9.2uF)

Automotive Grade GCM Series
(ISO9001, AEC-Q200, TS16949)

Consumer
LED lighting, TV, Air conditioner
Smartphone, Tablet, Wearable

Safety Recognized DE Series
(13 countries Safety Approved, X2/Y1/Y2)

Industry
Factory Automation, PLC,
Inverter

SNUBBER (SHIZUKI) MIC-UV Series
(~1,600V, ~4uF)

High Power EVC Series
(~1,600V, ~4uF)

DC-LINK (SHIZUKI) MEC-DL/HV Series
(~1,200V, ~1,600uF)

High Power Conversion

High Reliability

Metal Terminal KRM Series
(25V~1kV, ~100uF)

Implant Class D GCR/GCH Series
(ISO13485)

Embedded GRU/LLU Series
(110um~, Cu VIA Connection)

Ultra Small Size GRM01/02 Series
(008004, 01005)

Non Magnetic MA Series
(MRI application)

Multilayer RDE Series
(~220uF, ~2kV)

PA High Q GQM Series
(250V~500V, 1GHz~10GHz)

Ultra High Voltage DHS/DHK Series
(DC10~50kV, AC10~25kV)

Optical Transceiver GMA/GMD Series
(Wire Bonding, Au Electrode)

High Voltage DHR Series
(6kV~10kV)

Ultra High Voltage, Communication

High Density

Miniaturization

Low profile

Low ESL



Low ESR

High Reliability

Mechanical strength

High Stability

Outline

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2- Silicon Capacitors technology

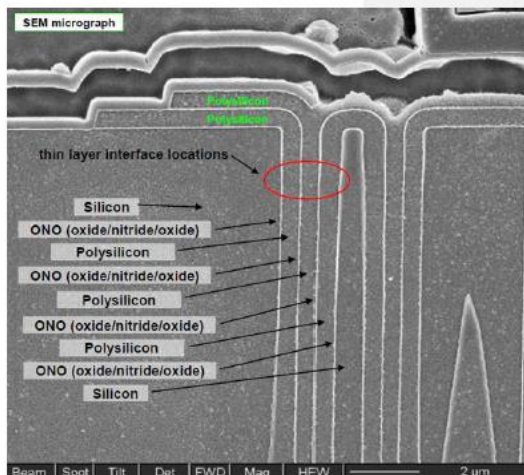
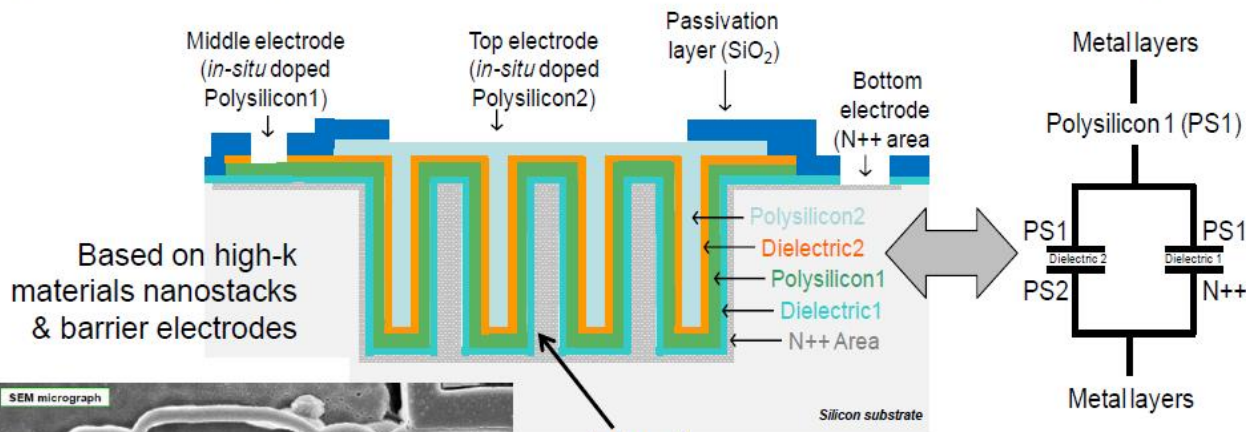
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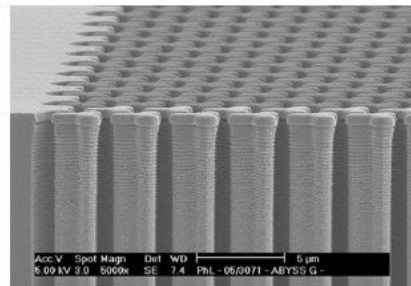
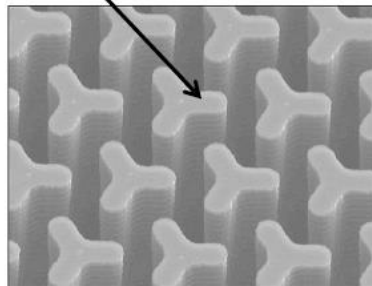
4- Summary

2- Silicon Capacitors Technology

2 parallelized capacitors in a MIMIM architecture to increase the capacitance value



Tripod



Tilted SEM view



Miniaturization

New market opportunities enabled by reduction in product size



Electrical characteristics

Wide frequency range, temp. stability, low leakage, low ESR, low ESL



Reliability

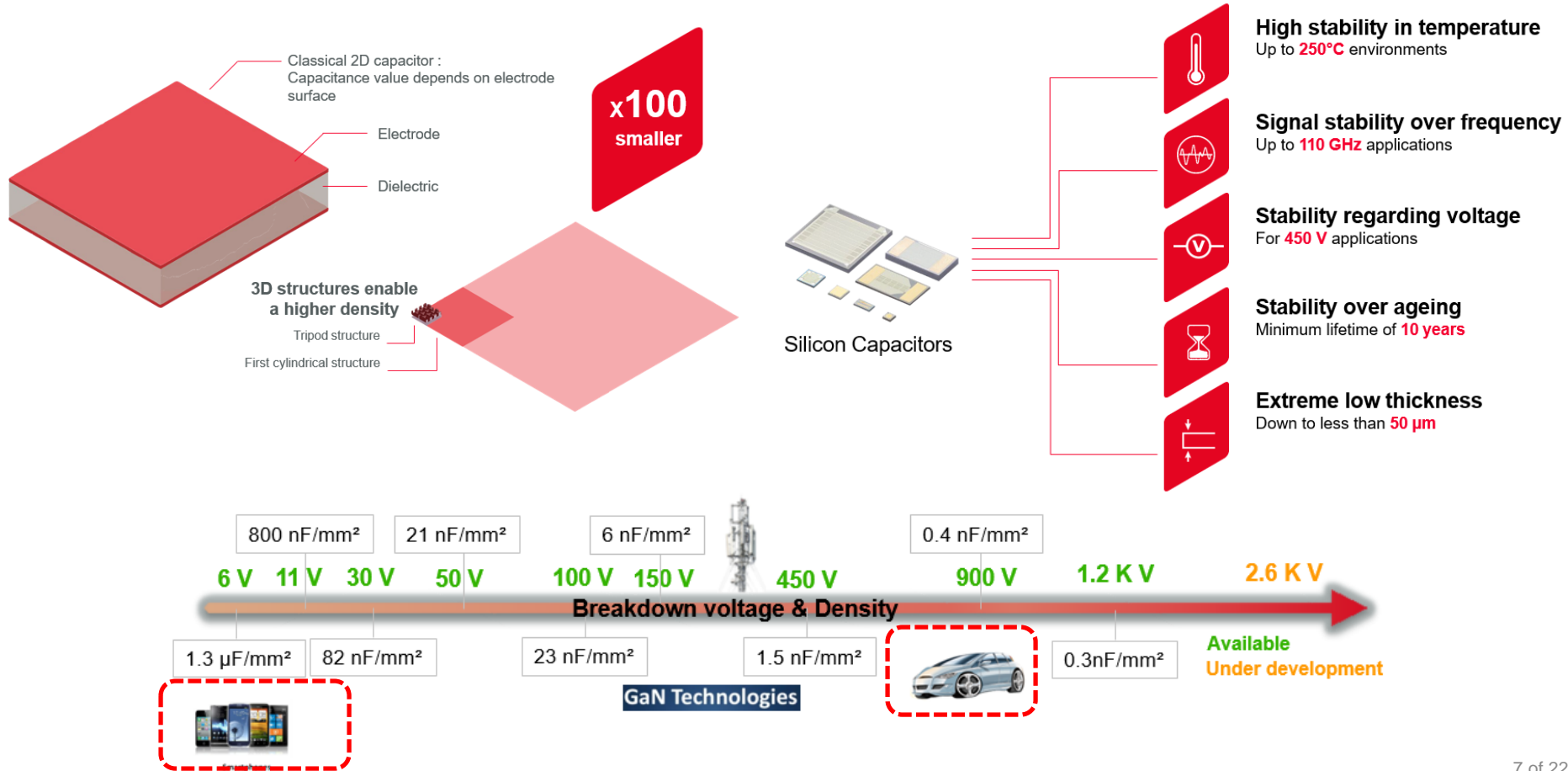
Low failure rates even at high temperatures with predictable failure modes



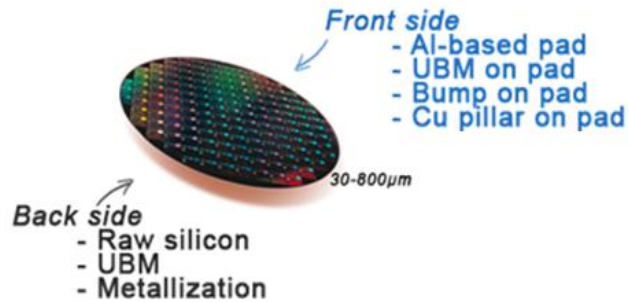
Other key advantages

Non-magnetic, customized products

2- Key features

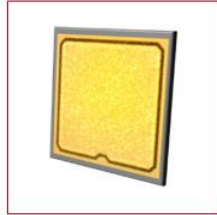
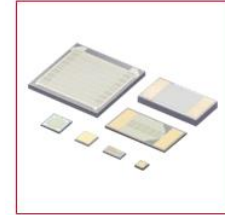


2- Different configurations



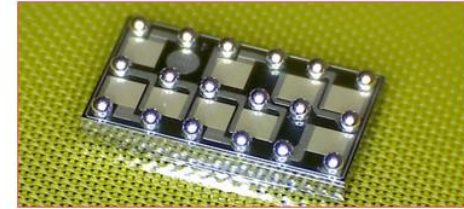
Stand alone and standard components :

horizontal and vertical capacitors



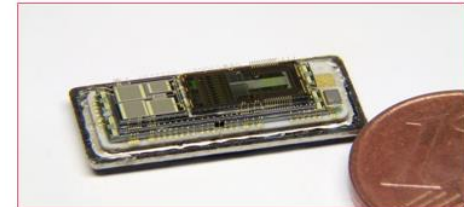
Component arrays:

combination of several passive components into a single silicon die

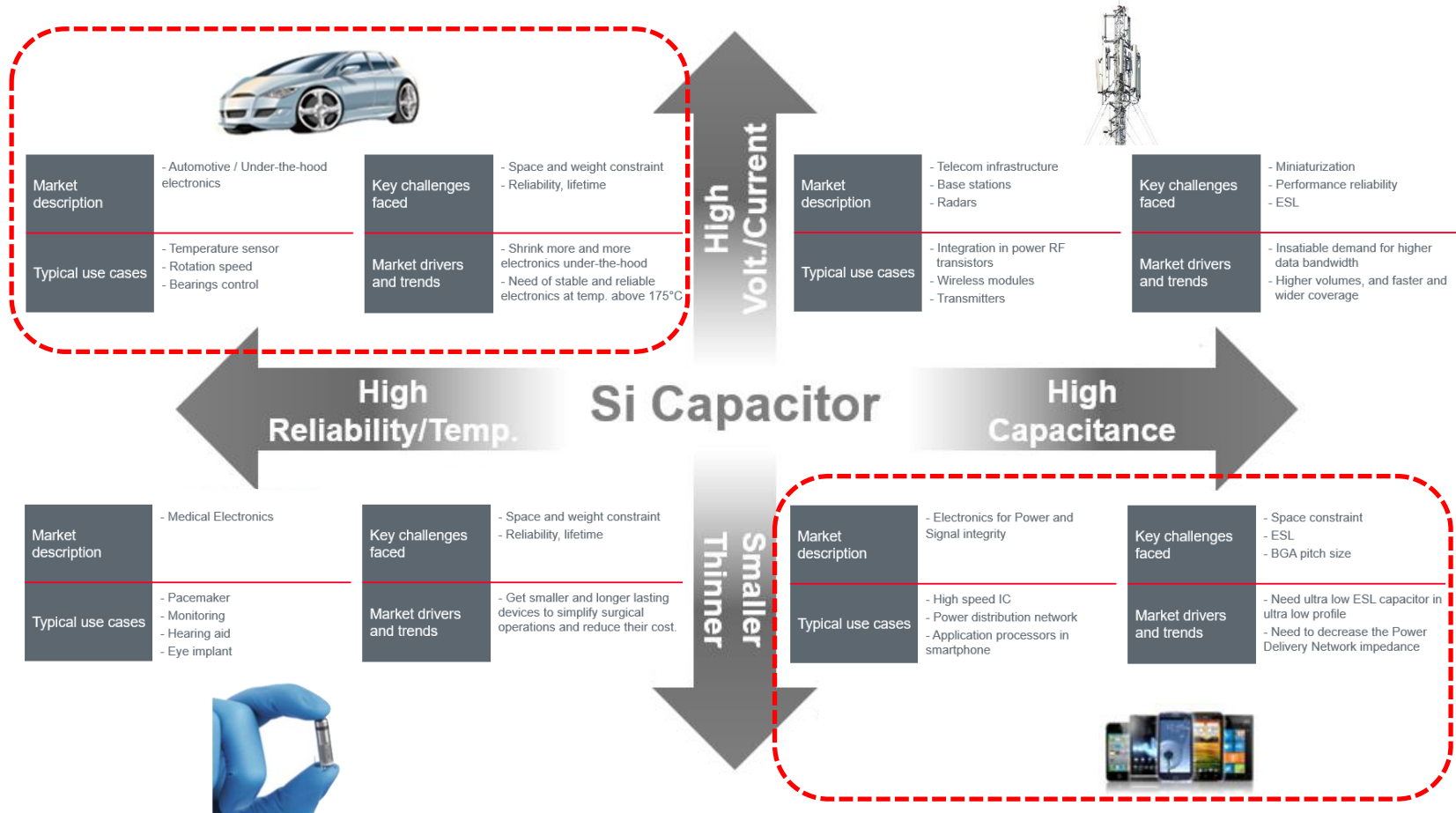


Interposers:

use of semiconductor assembly technologies to build high performance 3D structures



2- Market Drivers and challenges



Outline

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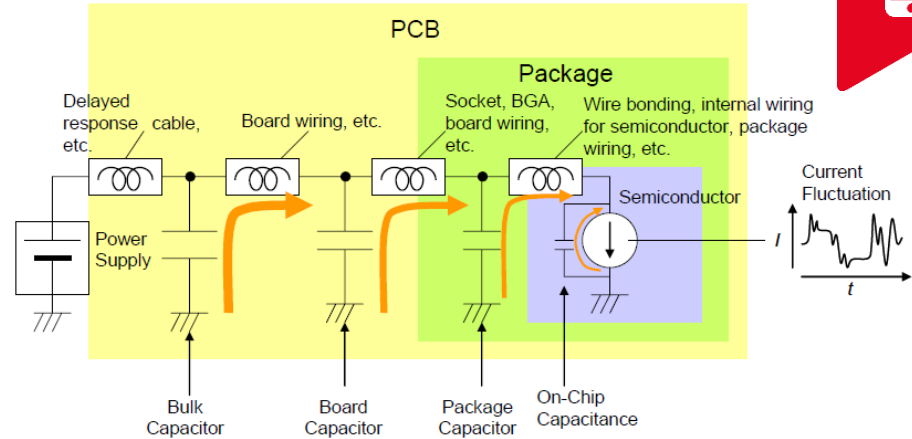
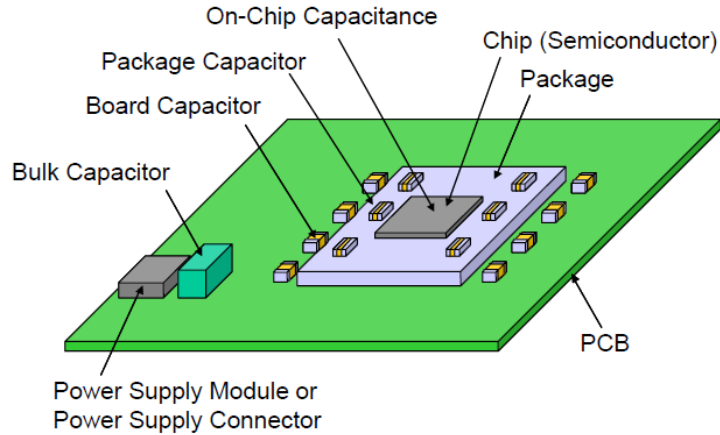
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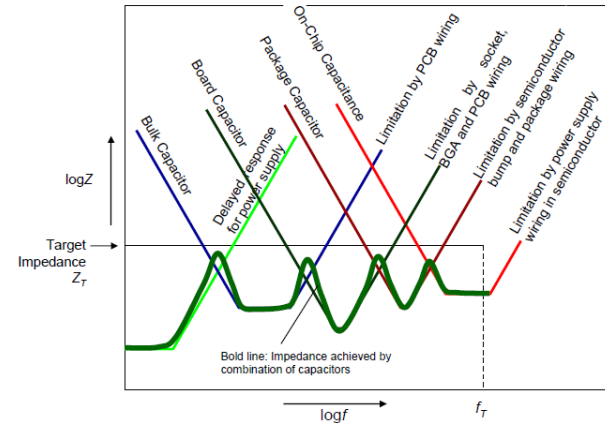
- PDN application (Mobile & HPC)
- LiDAR application (Automotive)

4- Summary

3- PDN Applications



- Power supply impedance must be made small over a wide frequency range
- One capacitor cannot achieve the necessary impedance, multiple capacitors are positioned hierarchically to achieve the target power supply impedance
- Due to space constraints, on-chip capacitance is not enough to reduce impedance at high frequencies.



3- PDN Applications_Requirements



Thickness



FOWLP / FOPLP

- Fine L/S (\rightarrow Fine BGA pitch)
- Low profile



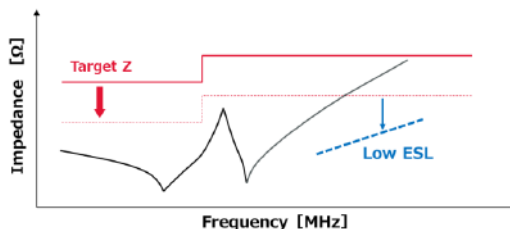
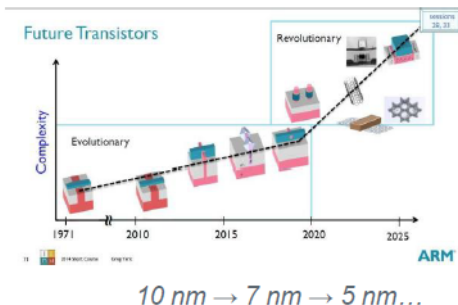
Low profile capacitor is needed

ESL

Microfabrication of process



Lower target impedance

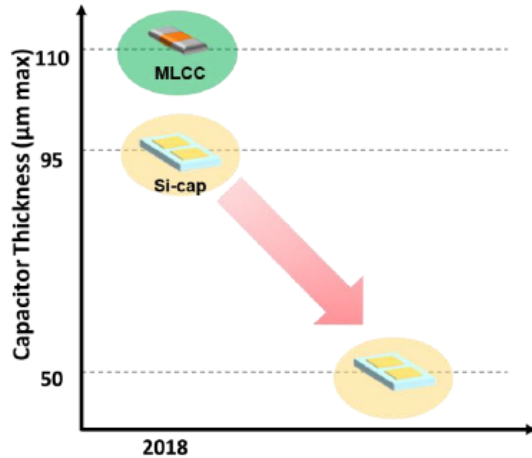


Low ESL capacitor is needed

3- PDN Applications_Improvements

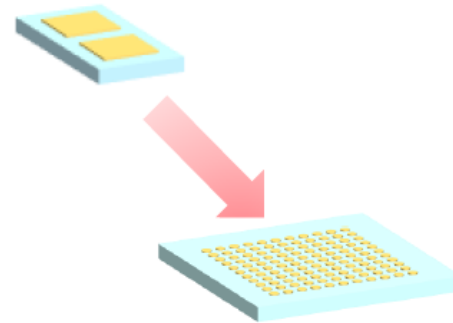


● Low profile



- Achieve low thickness ($\sim 50 \mu\text{m}$)
- Higher robustness

● Multi-terminal

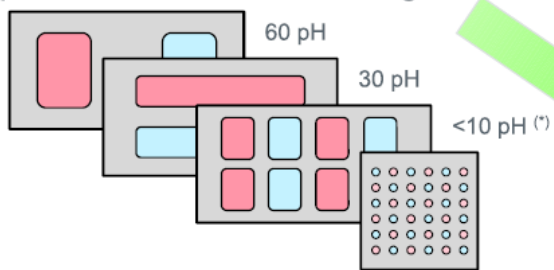


- Design many terminals on capacitor
Extremely low ESL < 10pH

3- PDN Applications_Benefits



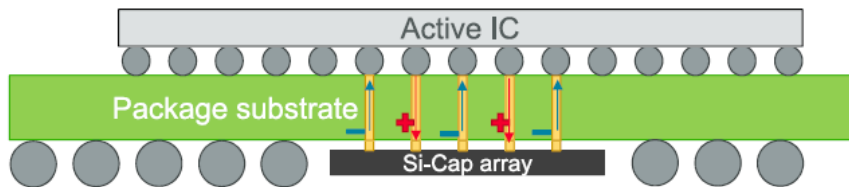
- Si-Cap intrinsic ESL is lower using fine bump pitch



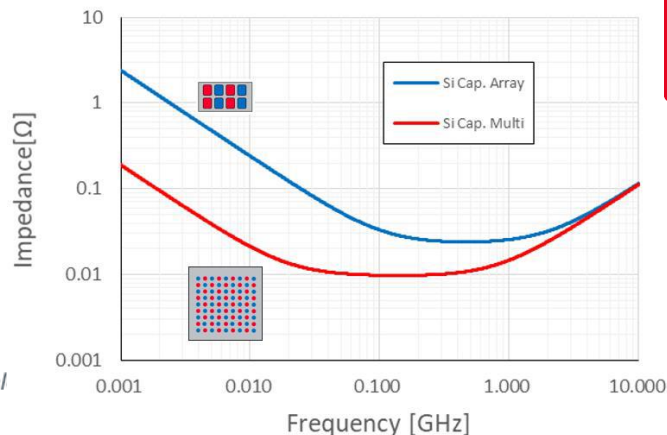
(*) theoretical two terminal equival

- Assembly ESL is reduced

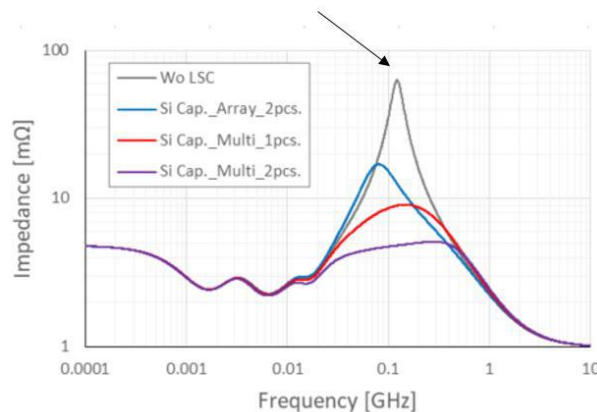
Multi-term generate smaller current loop → lower ESL
Particularly with multi-terminals (shorter distance between pads)



Typical Assembly Schema_Cross section view



Z_{peak} : anti-resonance between Chip and Board



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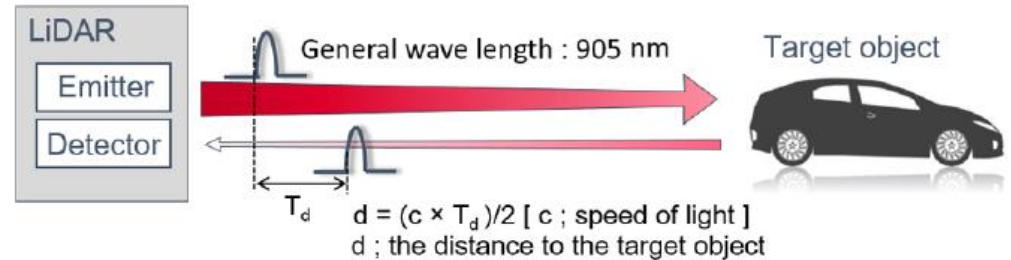
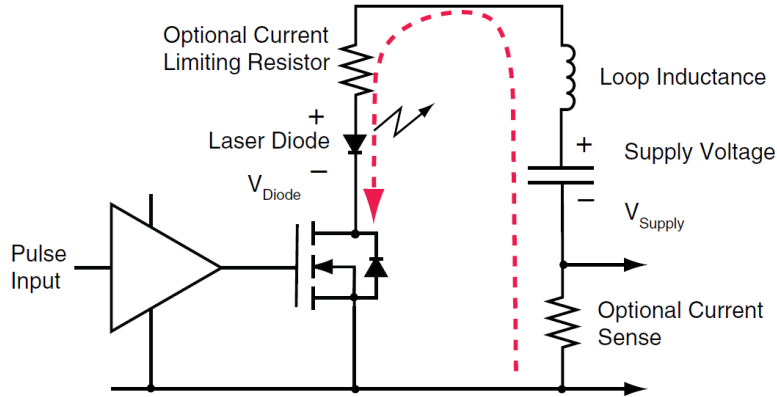
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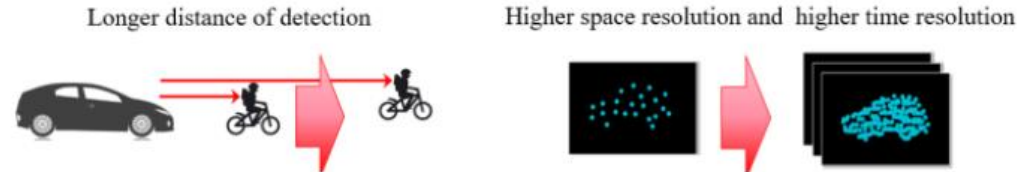
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4- Summary

3- LiDAR Applications



- In a LIDAR system to increase resolution current needs to be switched as quickly as possible through the laser diode.
- Gan FET's have very low input capacitance and can switch on very fast



3- LiDAR Applications_Requirements

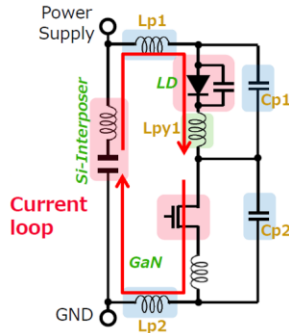


General requirements for LiDAR

- Longer range detection
- Higher space and time resolution
- Compliance with eye safety standards

General requirements for laser pulse

- Higher peak power
- Shorter pulse width
- Stability of pulse
- High reliability



Equivalent Circuit with Parasitic Contribution

Needs for Capacitor

- Withstand higher voltage : 120V as applied voltage
- Higher capacitance value : $\sim 10\text{nF}$
- Low ESL: 100pH for whole circuit
- Stable capacitance value vs temperature (up to 105°C)
- Availability of Wire-bonding

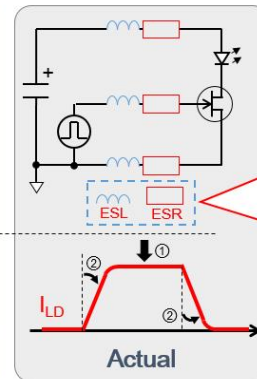
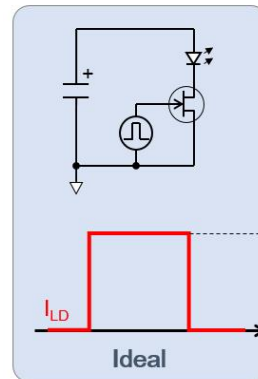
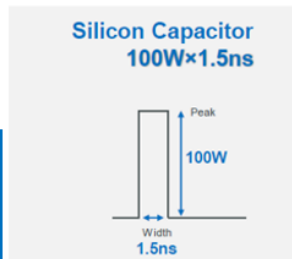
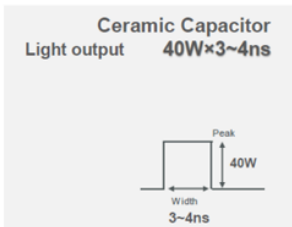
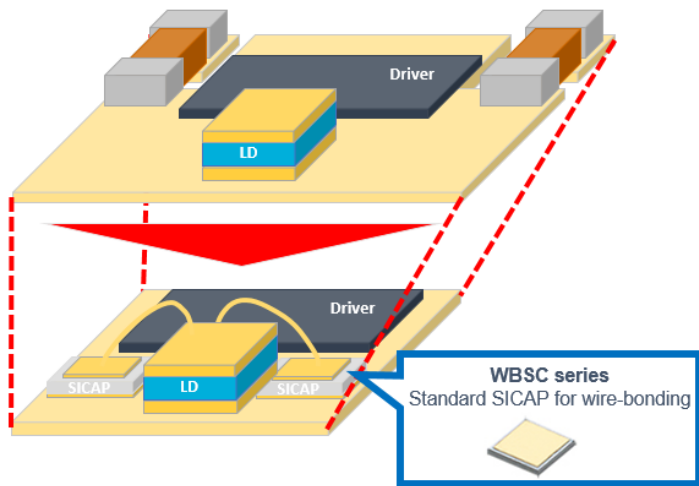
Needs for Interposer

- Withstand higher voltage : 80V as applied voltage
- Low ESL: 100pH for whole circuit

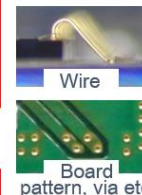
3- LiDAR Applications_Improvements



Design optimization by using SICAP for lower loop ESL & miniaturization.



Factors of parasitic impedance

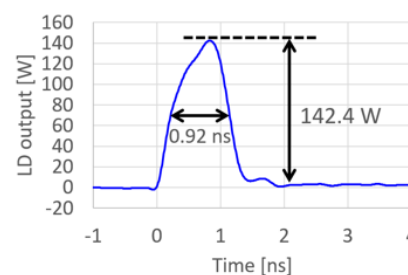
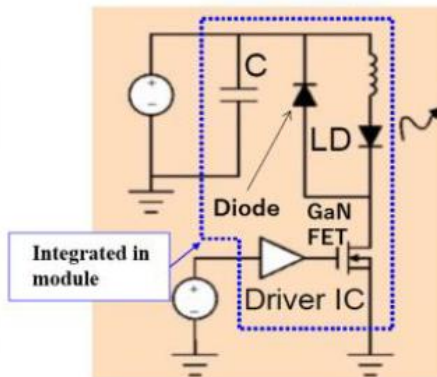
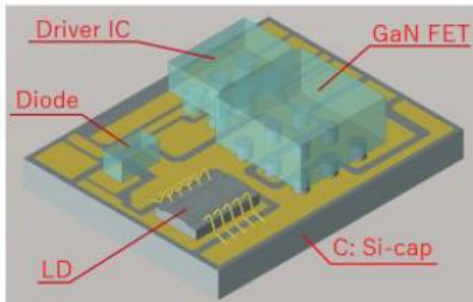


Capacitor
ESL & ESR

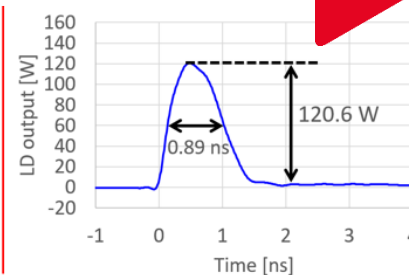
- Effect ① : Decrease LD current peak
Effect ② : Decrease LD current change rate

➡ Lower peak power & longer pulse width

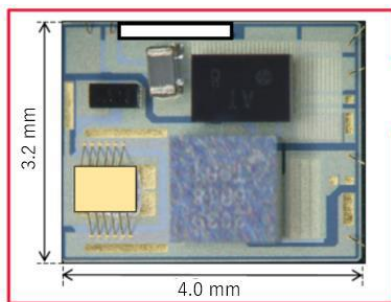
3- LiDAR Applications_Benefits



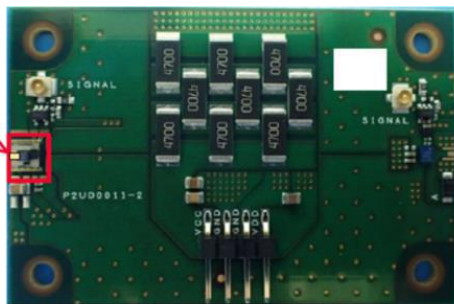
(a) Switching LD driver module



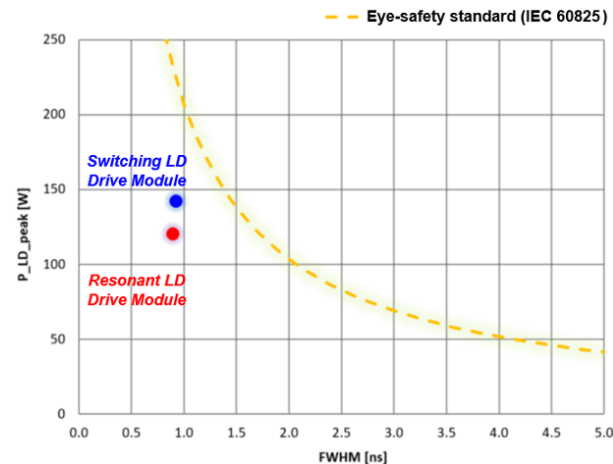
(b) Resonant LD driver module



Si-IPD



PCB



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- PwrSiP and PwrSoC are pushing passive devices to their technological limits
- Many parameters to take into account: specific to the passive component but also in relation with the surrounding environment (packaging, parasitic)
- Silicon technology presents a good alternative to classical solutions
- PDN applications (Mobile & HPC)
 - Requirements in terms of high density, low profile and low ESL
 - Silicon capacitors flexibility: process, materials, design, interconnects and assembly
 - Challenges in integration, testability, measurements (very low parasitic), simulations (electrical and mechanical robustness)
- LiDAR applications (Automotive)
 - High voltage, low ESL loop, Thermal stability
 - Silicon capacitive interposer presents innovative solution from electrical and assembly point of view
 - Challenges: automotive reliability standard (AEC-Q100) and Eye safety (IEC 60825)

Thanks a lot for your time and attention!

Any questions and/or comments?