PwrSoC at an Inflection Point: from R&D to Market Relevance

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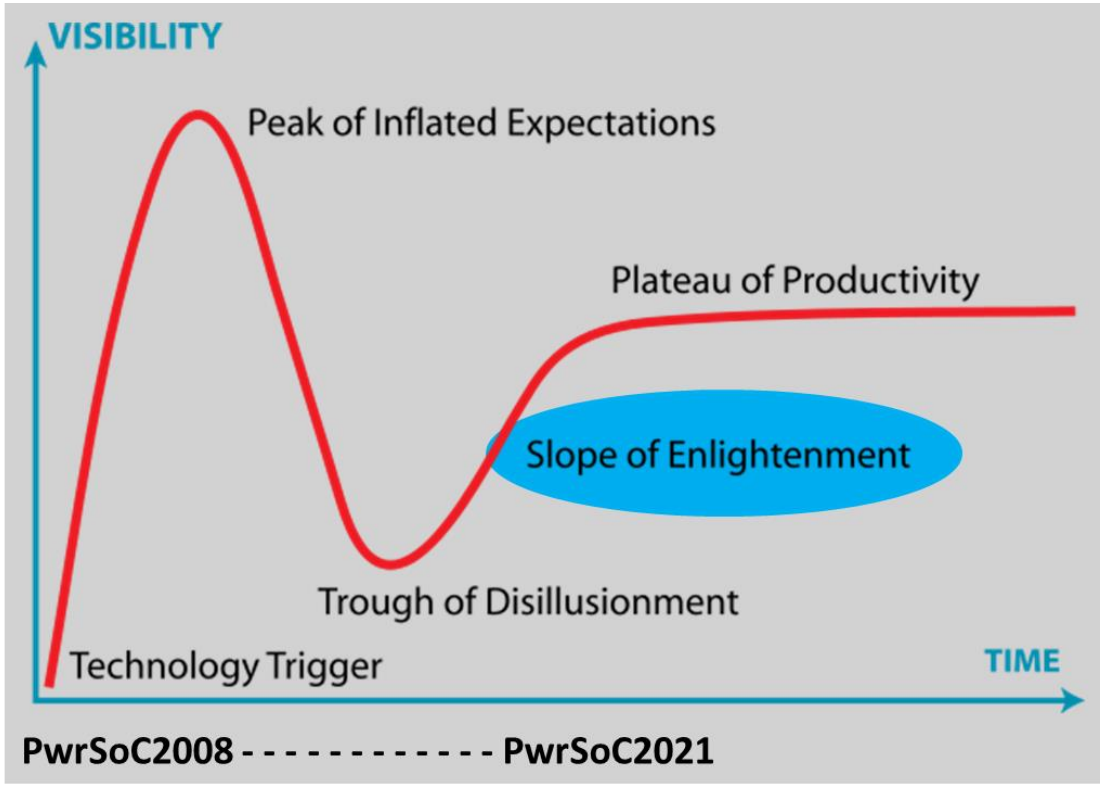
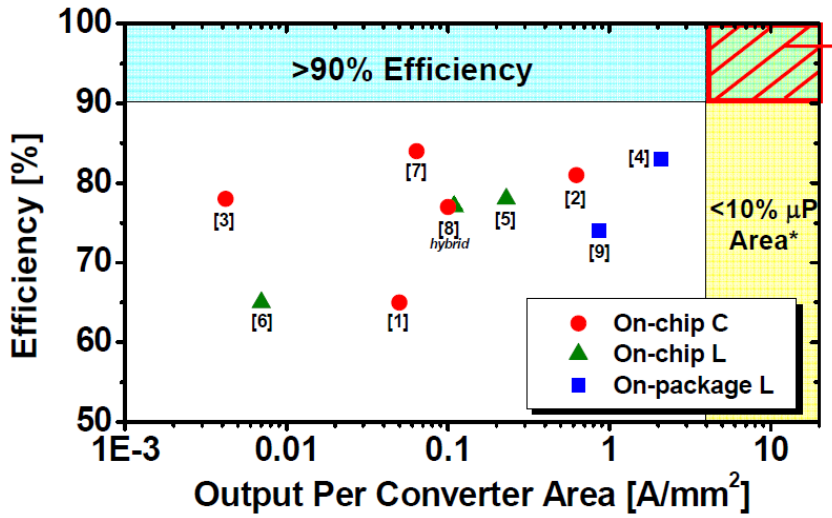
Agenda

- Where are we in the PwrSoC journey?
- Drivers and Enablers
- The key parameters
  - Efficiency
  - Size
  - Cost
- Conclusions

Where are we in the technology cycle?



Previous Work on On-Chip Voltage Conversion



WE ARE ALMOST THERE... after 10 years!

[1] Le, ISSCC10, 32nm
[2] Ramadass, ISSCC10, 45nm
[3] Kwong, ISSCC08, 65nm
[4] Hazucha, JSSC05, 90nm
[5] Wibben, JSSC08, 130nm
[6] Abedinpour, ISSCC06, 180nm
[7] Patounakis, JSSC04, 250nm
[8] Kim, JSSC12, 130nm
[9] Sturken, ISSCC12, 45nm

*Assumption: 1V, 200W, 500mm^2

- **Typically 3 approaches : (1) linear (2) switched-capacitor (3) buck**
  - **Linear regulator not suitable for high-voltage power delivery**
- **Difficult to achieve high efficiency & current density simultaneously**

4

PWR SOC 12

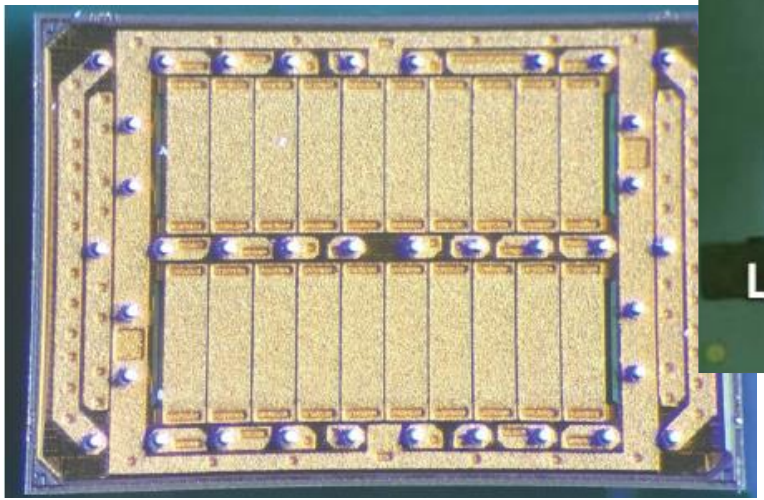
Deep Trench Capacitors for Switched Capacitor Voltage Converters

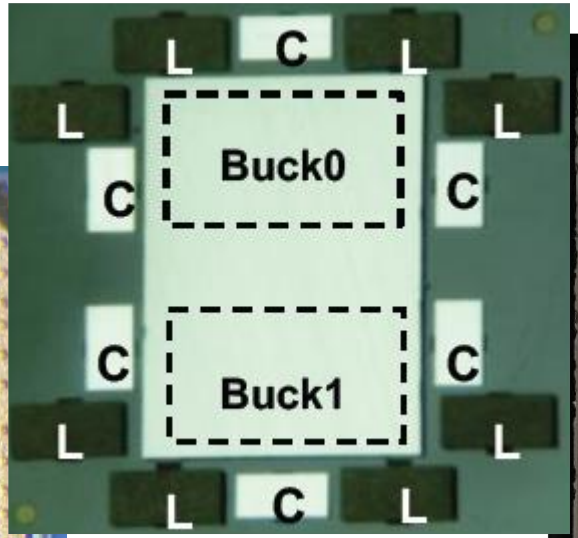
Jae-sun Seo, Albert Young, Robert Montoye, Leland Chang

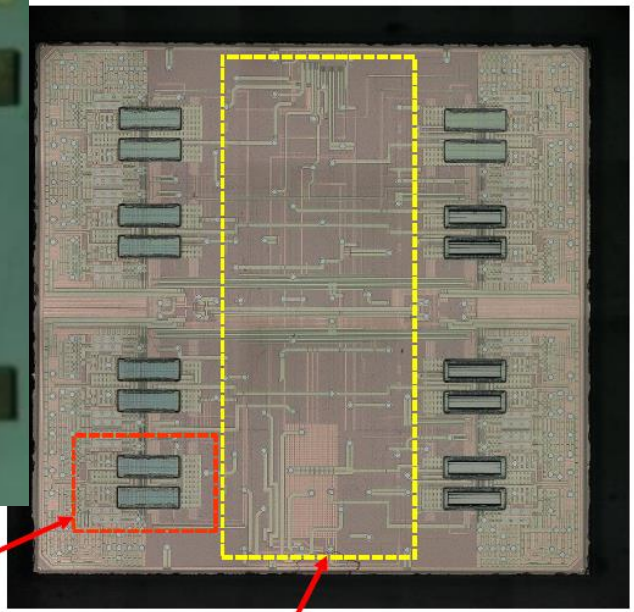
IBM T. J. Watson Research Center

For full history of PwrSoC see APEC 2020 presentation: F. Carobolante "Power Supply on Chip as a key enabler for high performance applications"

Ferric, Dialog and Huawei show fully integrated PwrSoC's







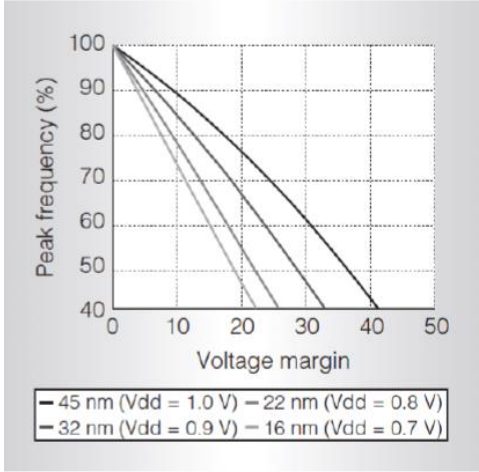
2-phase VR cell with integrated magnetic thin film inductor

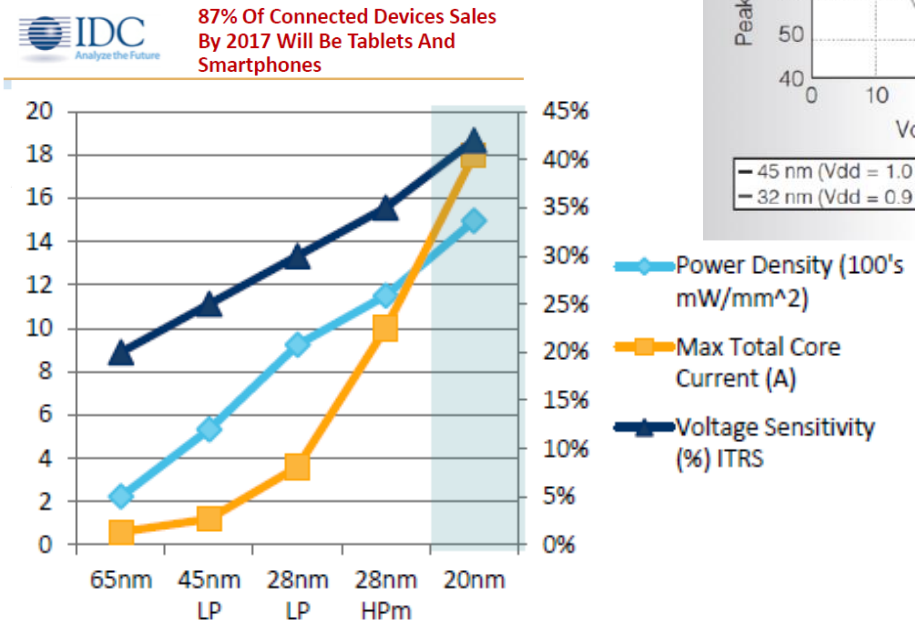
Master controller/Common analog circuits/DFT circuits

The mobile phone points to the need for PwrSoC

Applications driving Power Integration

- Energy harvesting and Internet of Things (IoT)
  - Compact, low power, heterogeneous integration
- High Performance Computing
  - Performance and efficiency constraints
- Mobile devices
  - Limited space, highest performance, efficiency

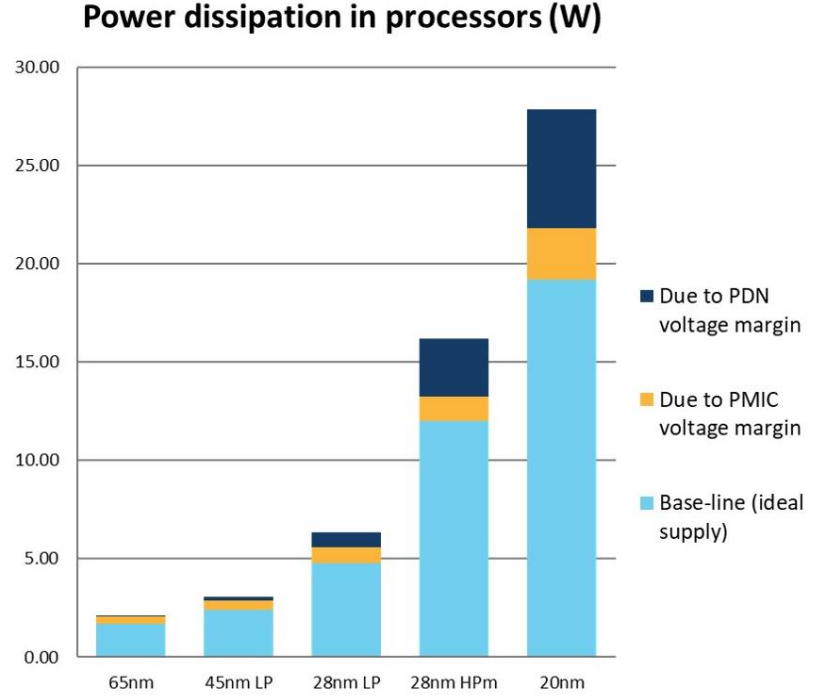


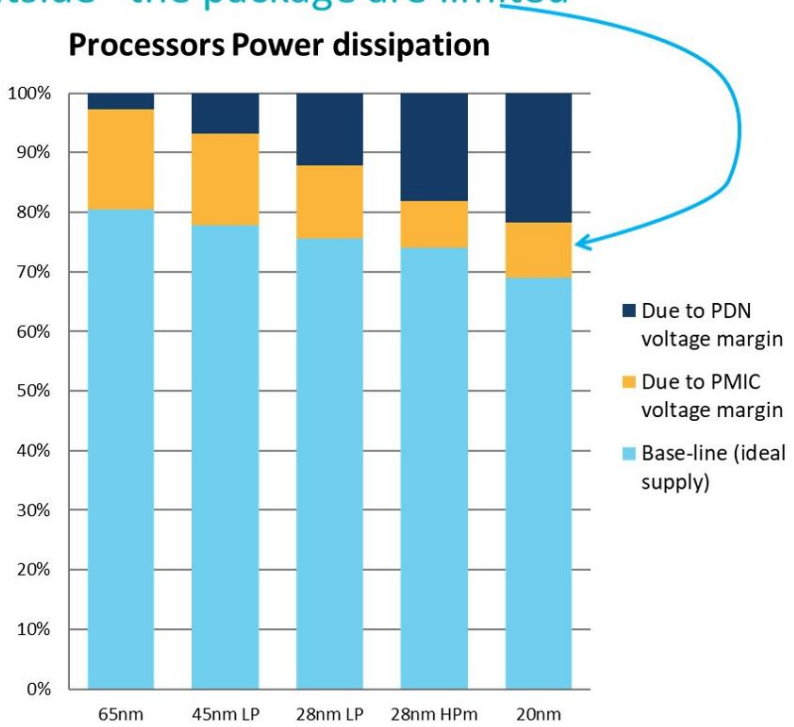


F. Carobolante: "Power Supply on Chip: from R&D to commercial products"

Inefficiency grows due to lower load impedance and fast transients

Gains achievable from Power Management "outside" the package are limited





Power Dissipation grows more than quadratically with supply voltage (~V^3)

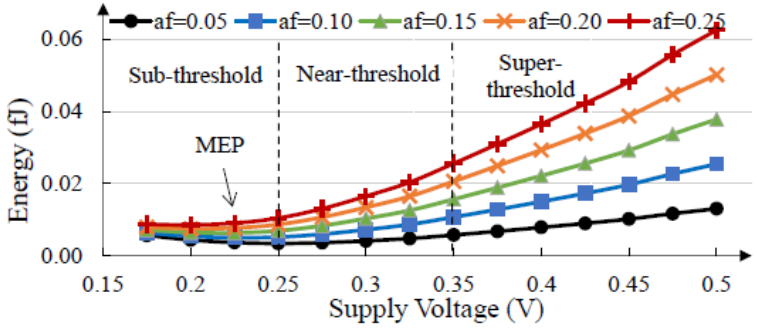


Figure 4. Energy consumption of a 20-stage inverter chain versus supply voltage at different activities factors (af) for FinFET 7nm normal V_{th} device.

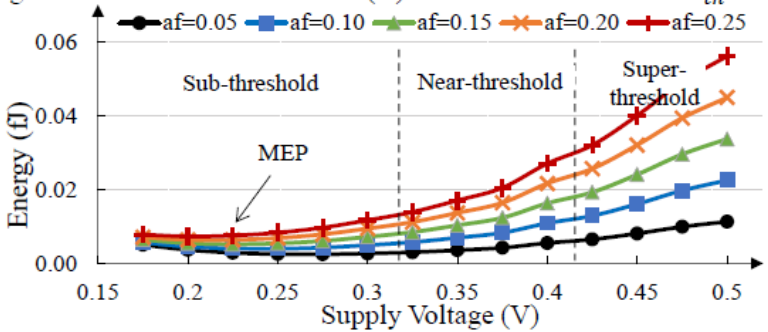
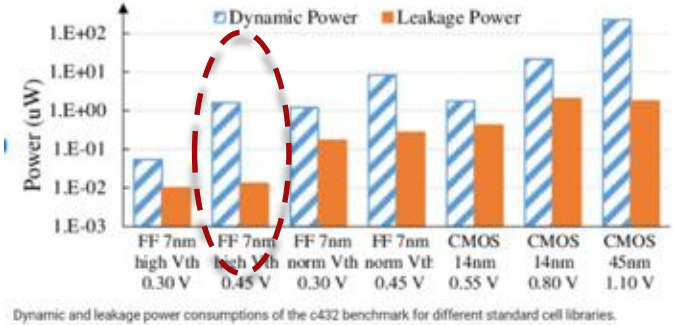


Figure 6. Energy consumption of a 20-stage inverter chain versus supply voltage at different activities factors (af) for FinFET 7nm high V_{th} device.

For <10nm processes, SoC power increases by 3% for every 10mV increase in supply voltage!

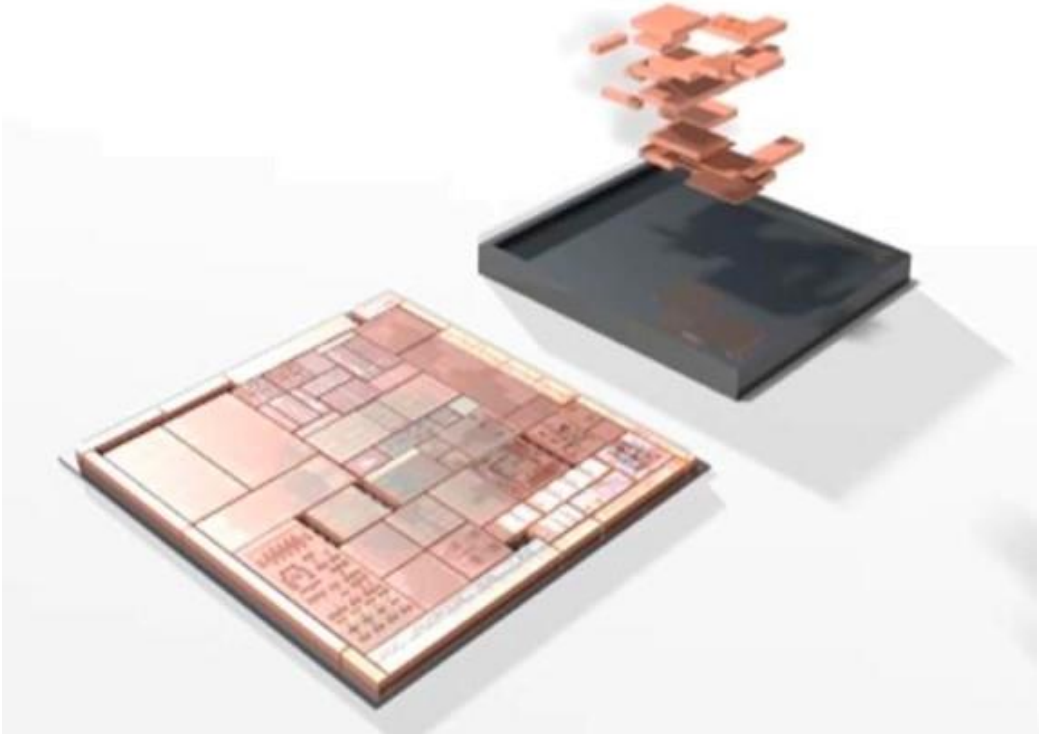


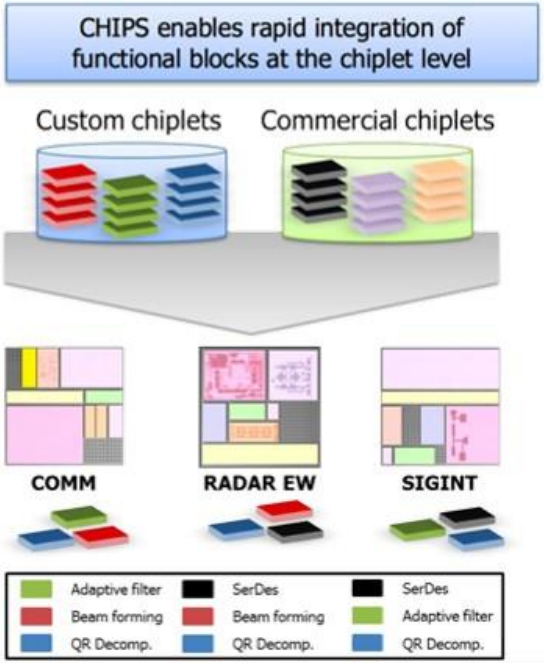
Dynamic and leakage power consumptions of the c432 benchmark for different standard cell libraries.

Qing Xie et al. "Performance Comparisons between 7nm FinFET and Conventional Bulk CMOS Standard Cell Libraries," IEEE Transaction on Magnetics, 2015

CHIPs

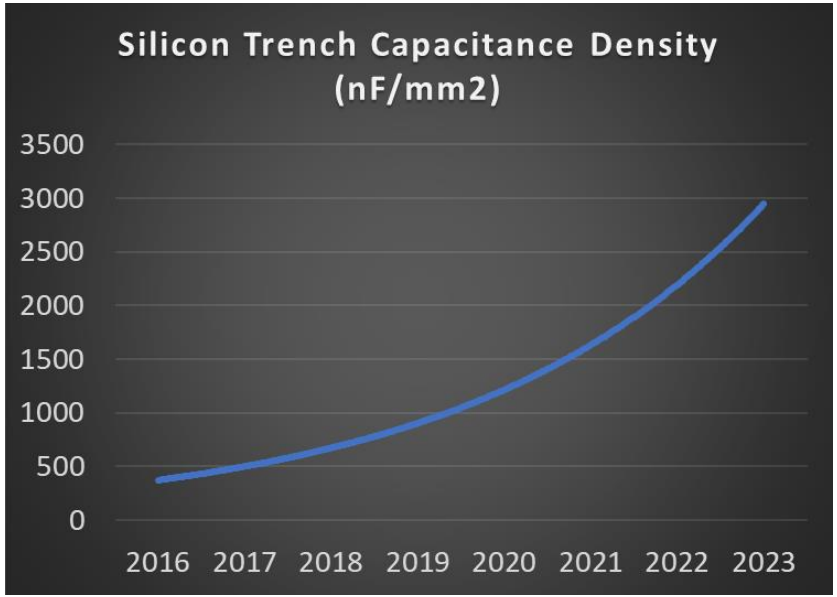
The evolution of high-performance systems to a "chiplet" approach and heterogeneous integration is facilitating the integration of the "PMIC chiplet," since a two-stage approach to regulation becomes mandatory

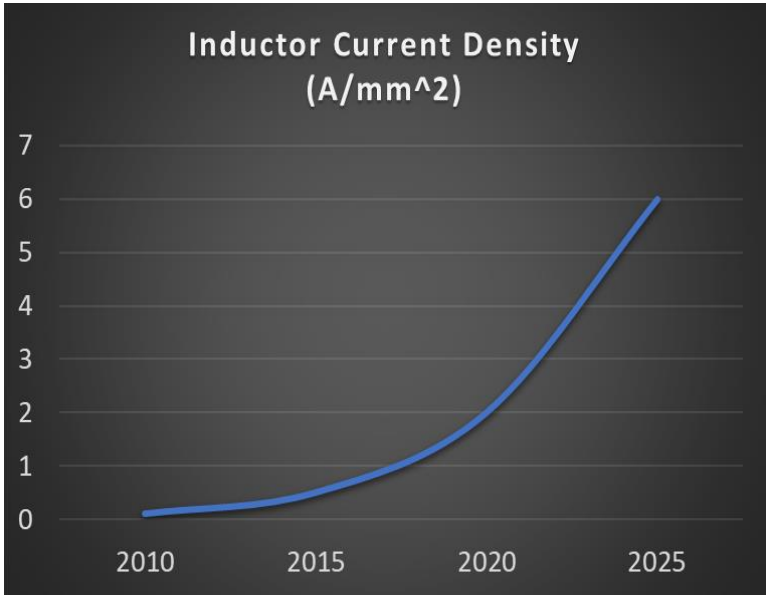




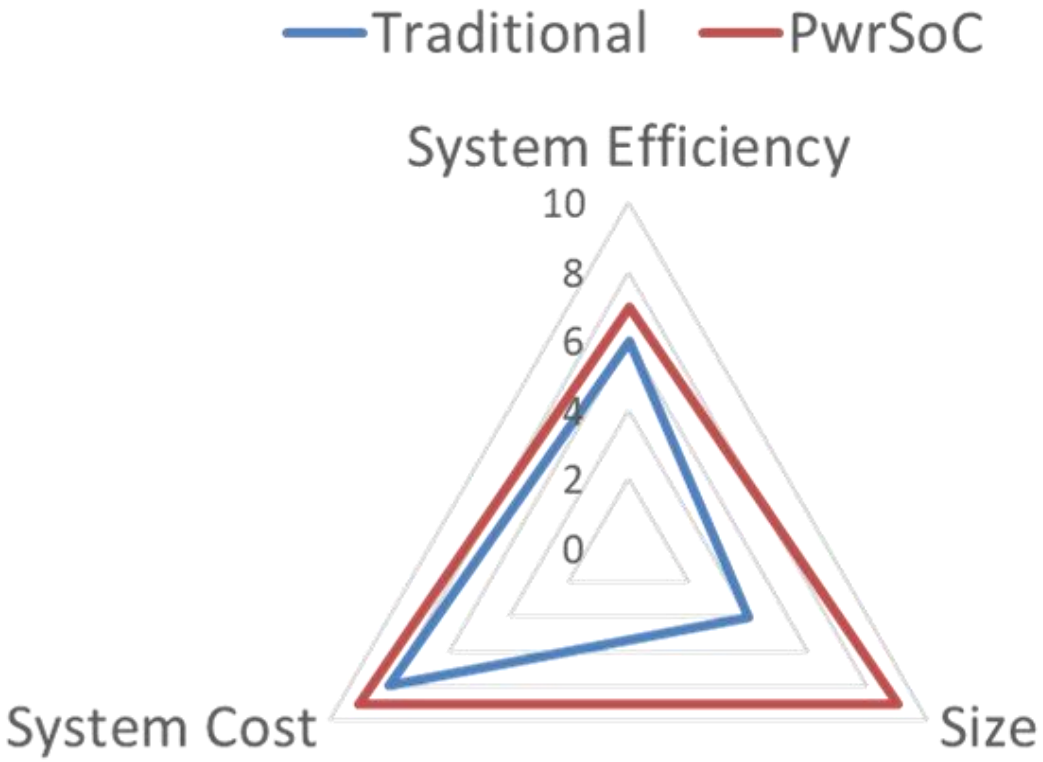
Enablers: Convergence of technologies

Deep Trench capacitors & Integrated Inductors

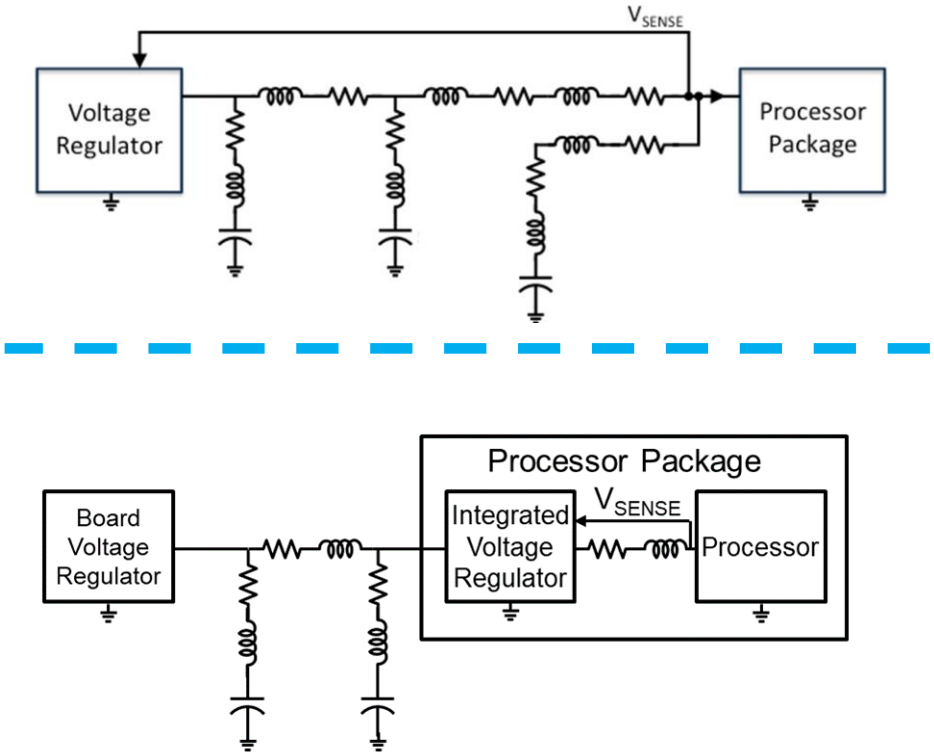




Value proposition: PwrSoC vs Traditional PMIC



Efficiency

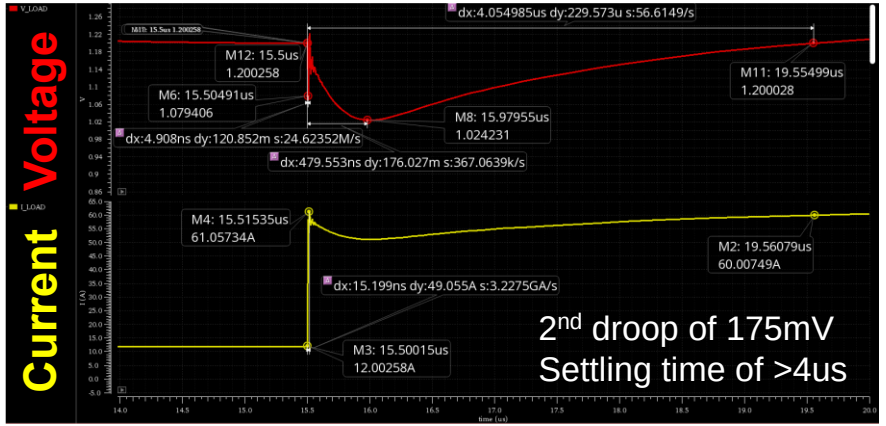


Benefits of PwrSoC:

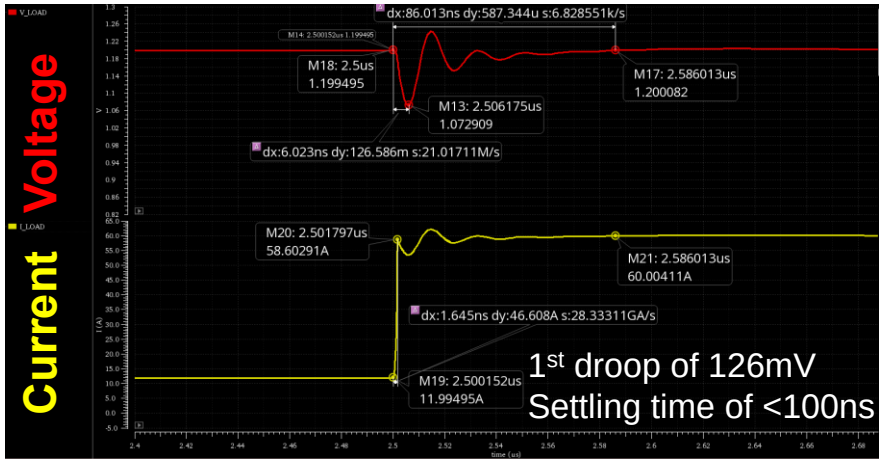
- High bandwidth (> 50MHz) feedback can be placed directly on the processor load
- Broadband supply impedance reduced to <1mΩ
- Drastic reduction of processor supply voltage margins → improved efficiency
- Regulation of resonant impedance peaks from upstream PDN →
- No 3rd droop and reduced 2nd droop

Power Integrity Comparison

60A Processor Load Step with Mother Board VR



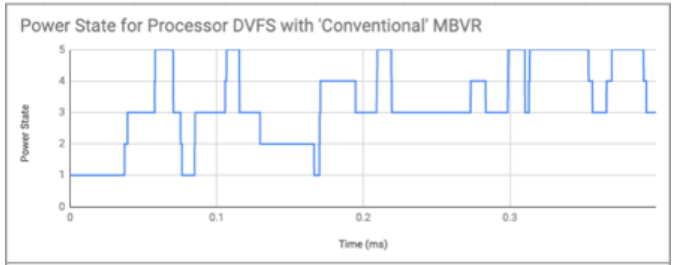
60A Processor Load Step with in-Package VR

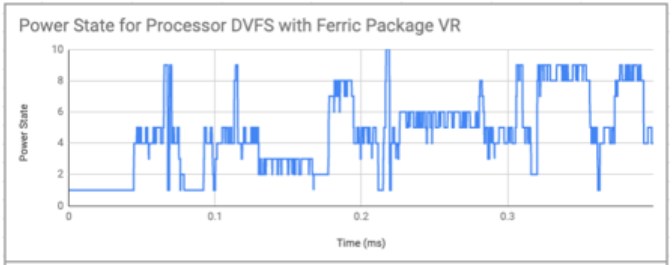


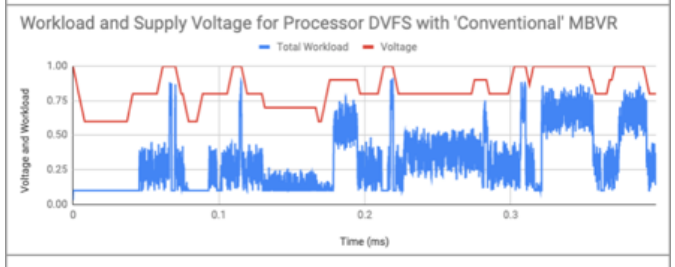
Courtesy of Ferric Inc.

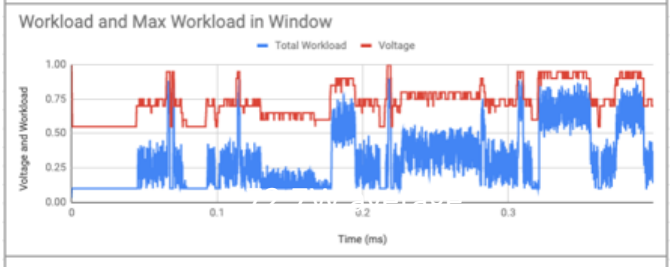
Fine Grain DVFS

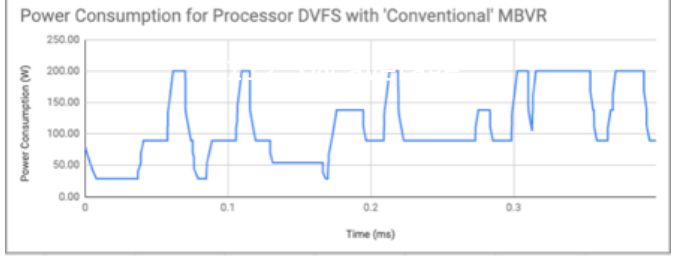
Identical Workload and Performance with 35% less power consumption!

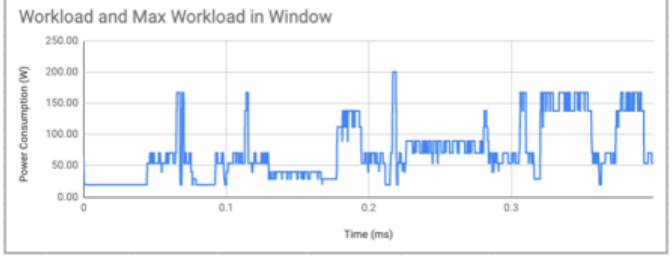






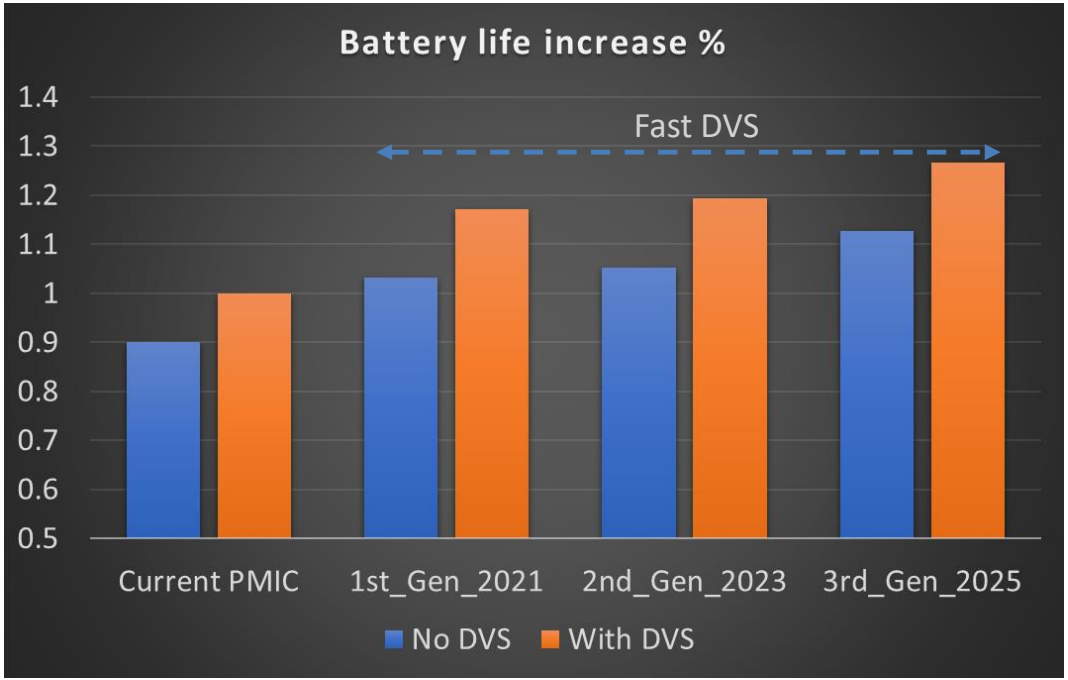






Courtesy of Ferric Inc.

BATTERY LIFE increase by 3-26% depending on implementation

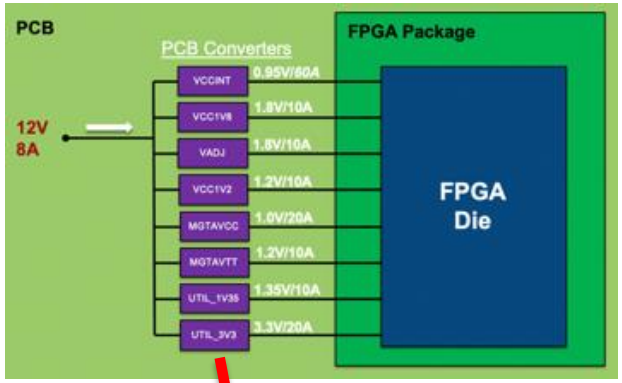


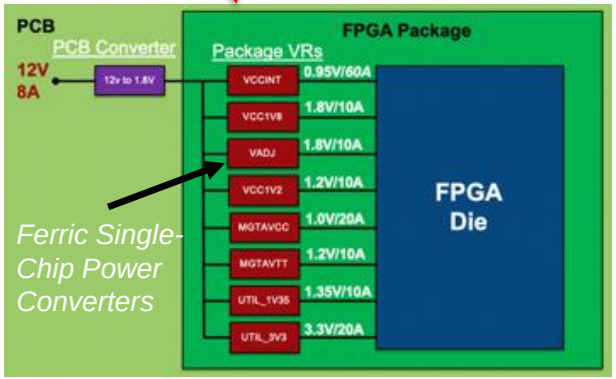
Note: Above numbers are based on the Google Pixel

Size Matters

- Shrink power converters to be co-packaged with processors
- Reduce losses associated with high currents through board → socket → package → processor
- Enable delivery of many independently scalable supplies

Courtesy of Ferric Inc.

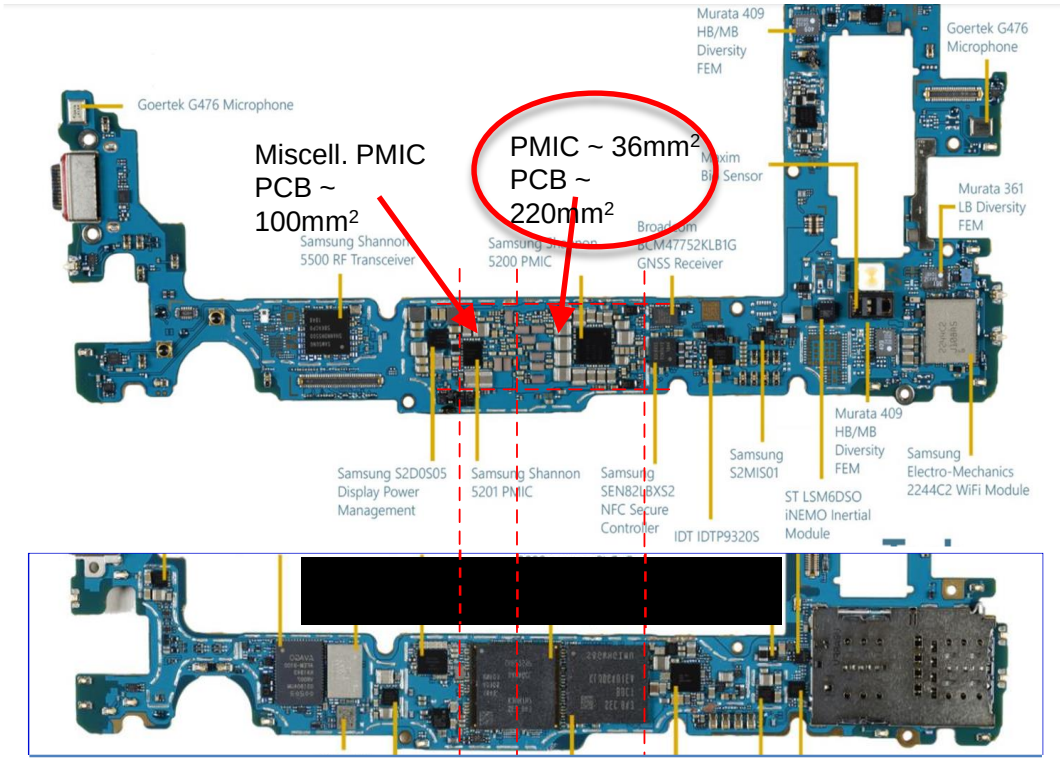




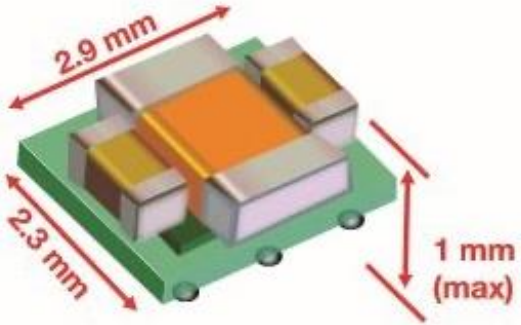
Mobile products: typical PMIC area dedicated to SoC's is greater than 200 mm^2

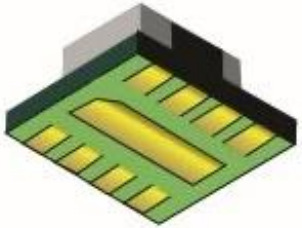
PC Boards are often skinny and long, making it difficult to optimize routing

Samsung Galaxy 10e

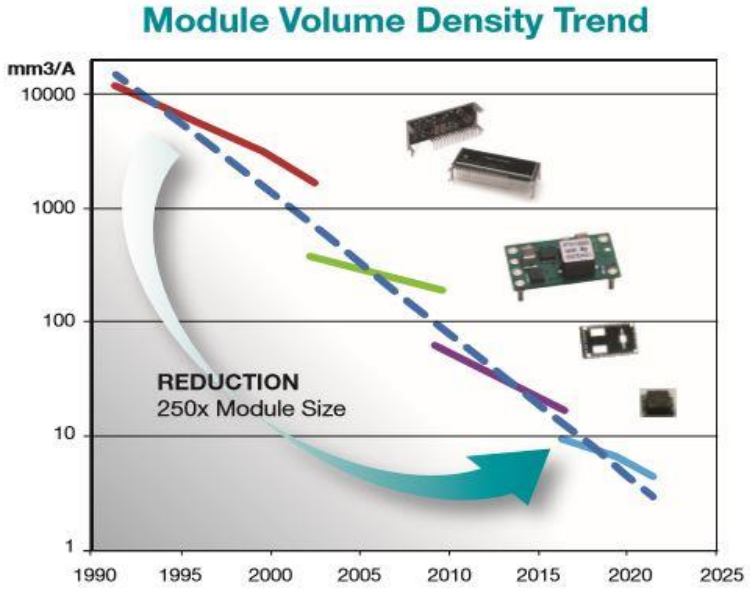


Current Roadmap for PMIC - State of the Art: MicroSIP (25% Volume Reduction per Year)



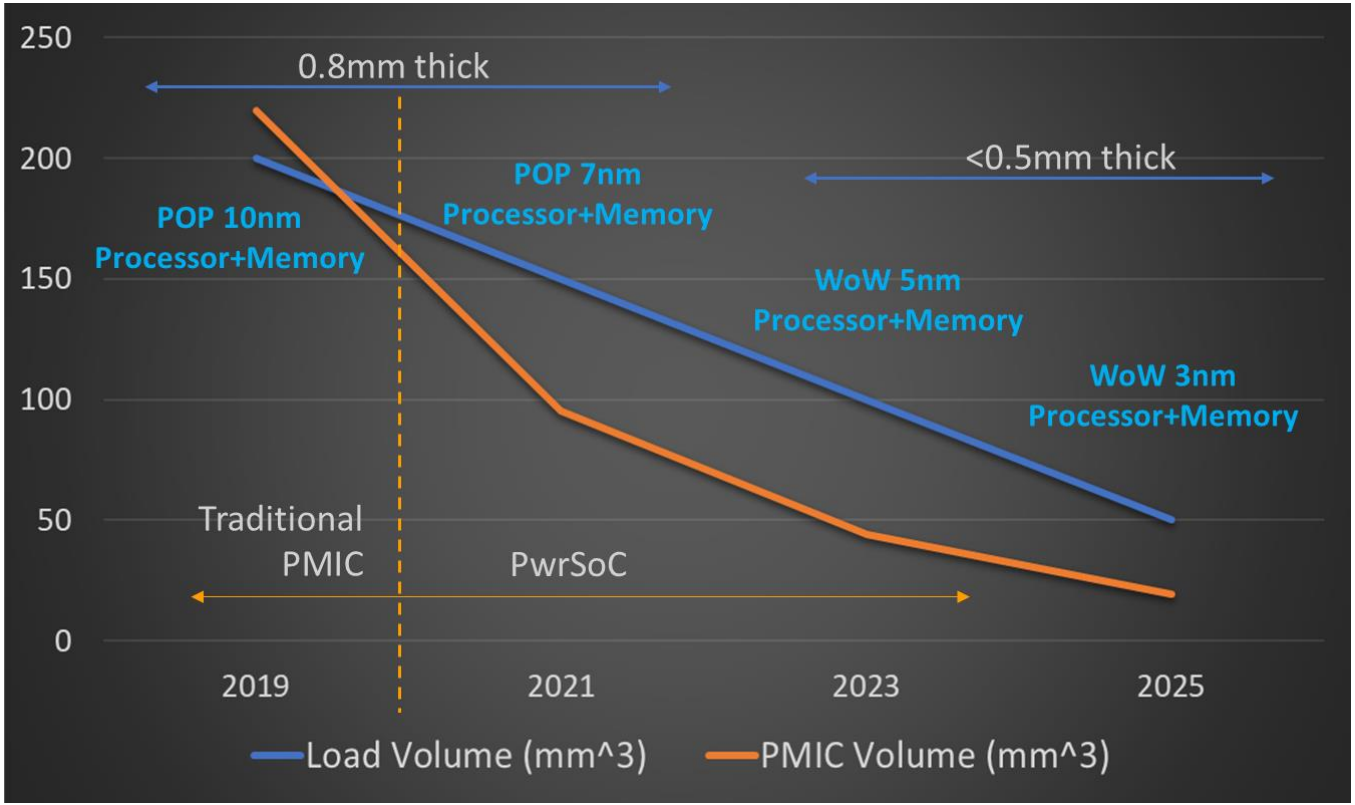


From Texas Instruments: "Powerful solutions come in small packages - Innovative SiP power modules simplify and accelerate system development"

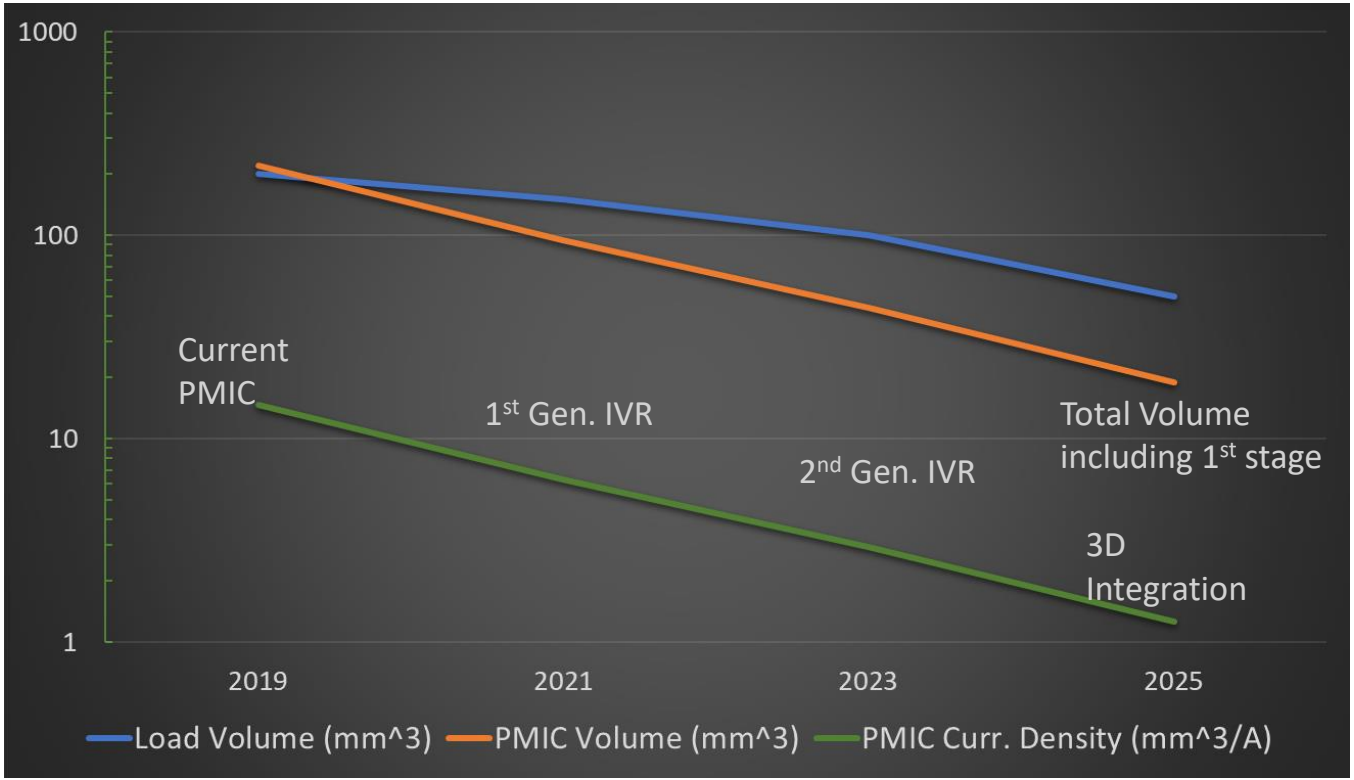


Power modules have paralleled the tremendous downscaling that has taken place in circuitry. In the past 25 years, TI has brought an average module size reduction of 25 percent annually – and aims to continue this trend.

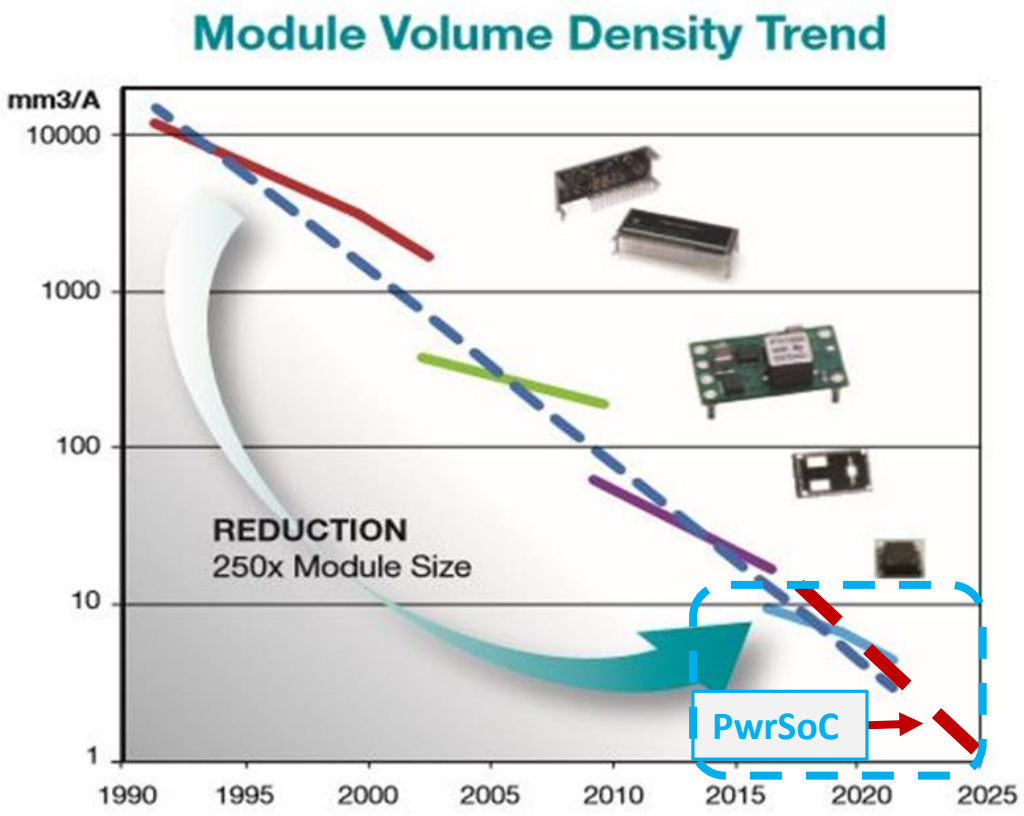
Volume occupied by Processor and PMIC



Density evolution

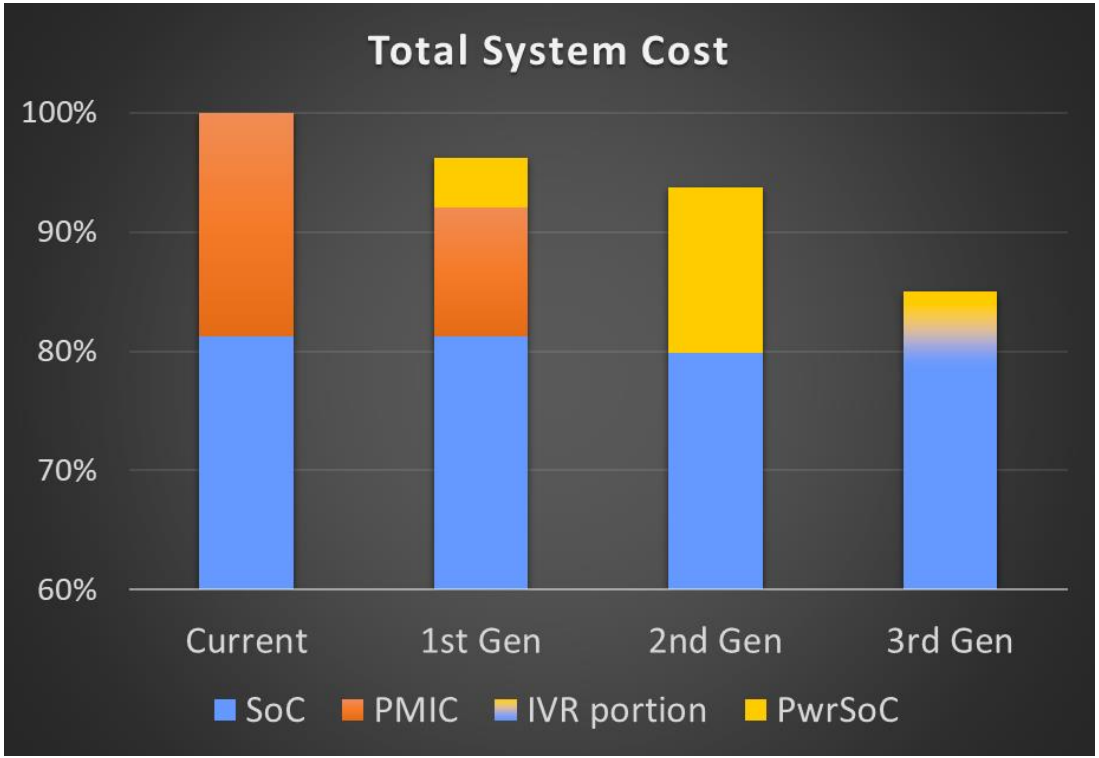


PwrSoC extends the Density trend another decade!



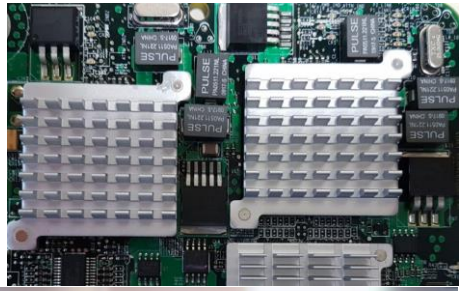
Power modules have paralleled the tremendous downscaling that has taken place in circuitry. In the past 25 years, TI has brought an average module size reduction of 25 percent annually – and aims to continue this trend.

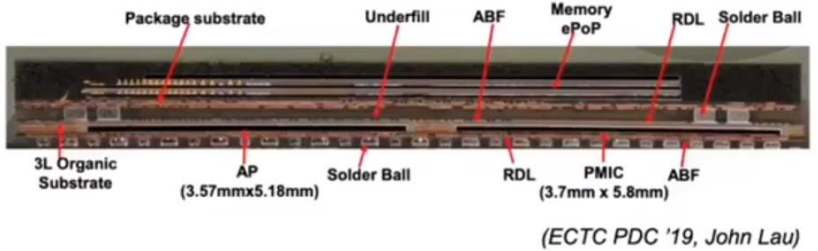
COST: PMIC Integration reduces system cost by ~15%



What are the drivers?

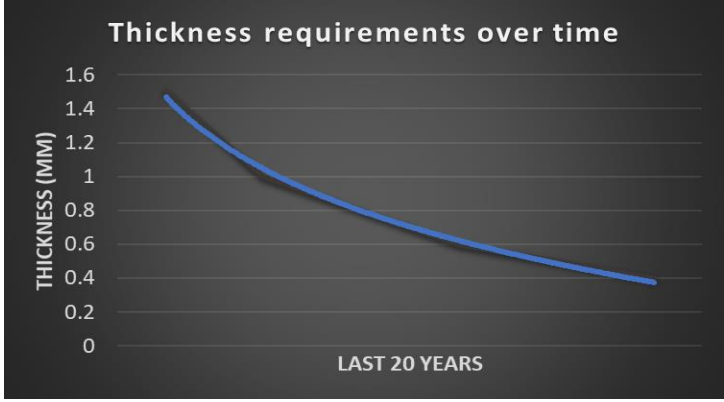
- Server platforms (performance!)
  - HPC
  - Accelerators
- Wearables (there is no room!)
  - Smartwatches
  - AR/XR glasses
- Mobile (size and efficiency!)
  - Smartphone
  - Tablets





(ECTC PDC '19, John Lau)

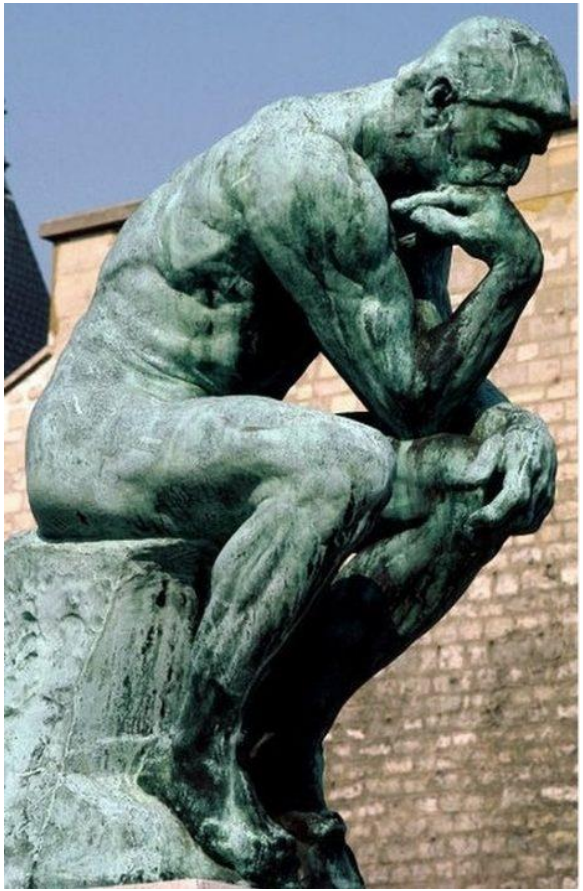
CONCLUSIONS



- Passives need to shrink to enable integration, both for performance and to keep up with packaging requirements

→ Only Silicon passives can deliver ***size-performance-reliability***

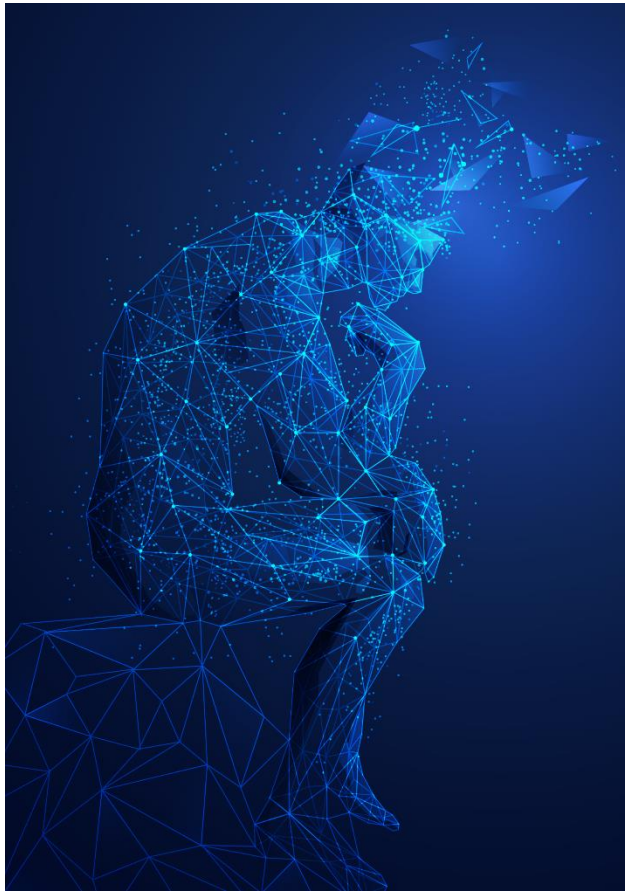
- We expect to see multiple product lines shipping by the end of 2021
- Evolution of integrated passives, together with advanced packaging technology, will keep the density trend going for many years.
- New Architectures leverage the integration, leading to high-frequency with performance superior to discrete approaches
- A byproduct of such integration is improved reliability (especially in small form factors)



QUESTIONS?

Thank you for Listening

francesco@iotissimo.com



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