more than you expect

WÜRTH ELEKTRONIK

PSMA APEC

Silicon Based Supercapacitors – Evolution to Integrated Passives

A scientific approach on the way to a record braking new technology?

Short Introduction

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Background:

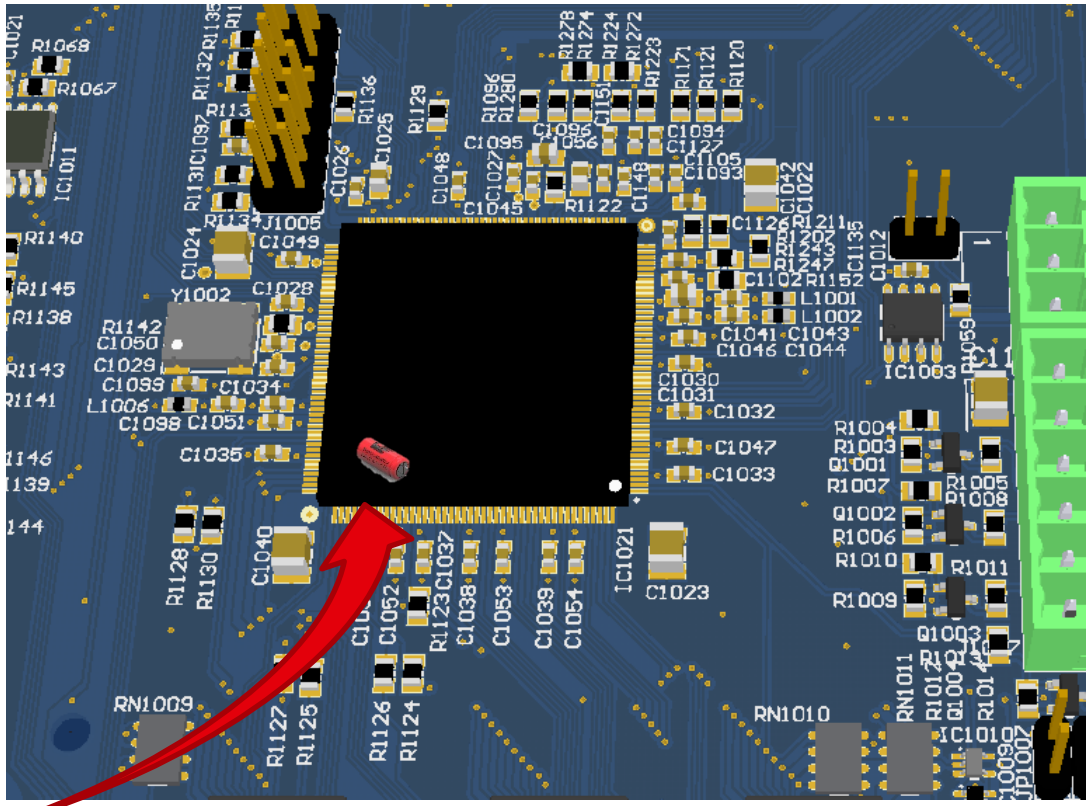
- Experience in
  - application-oriented research
  - development of organic electronics,
  - polymer analysis
- Responsible for Supercapacitors

Motivation

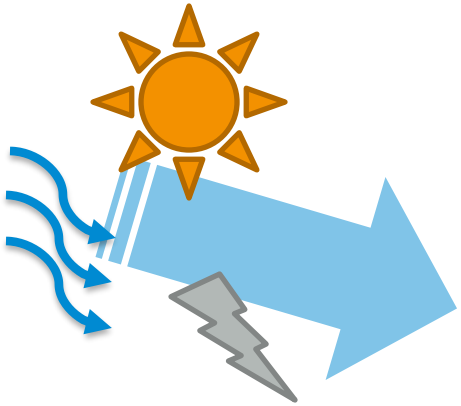
- **Power supply for processors and IC require**
  - Many discrete passive components
  - Space on the PCB
  - Design-in time

- **Supercapacitors are passive short term power supplies**

?



Motivation, Example



(light, wind, vibration, …)

Energy Harvester

Fluctuating Power Source

Power Management IC

Regulator

Charger

Transmitter

UHF Transmitter

Buffer Storage

Supercap

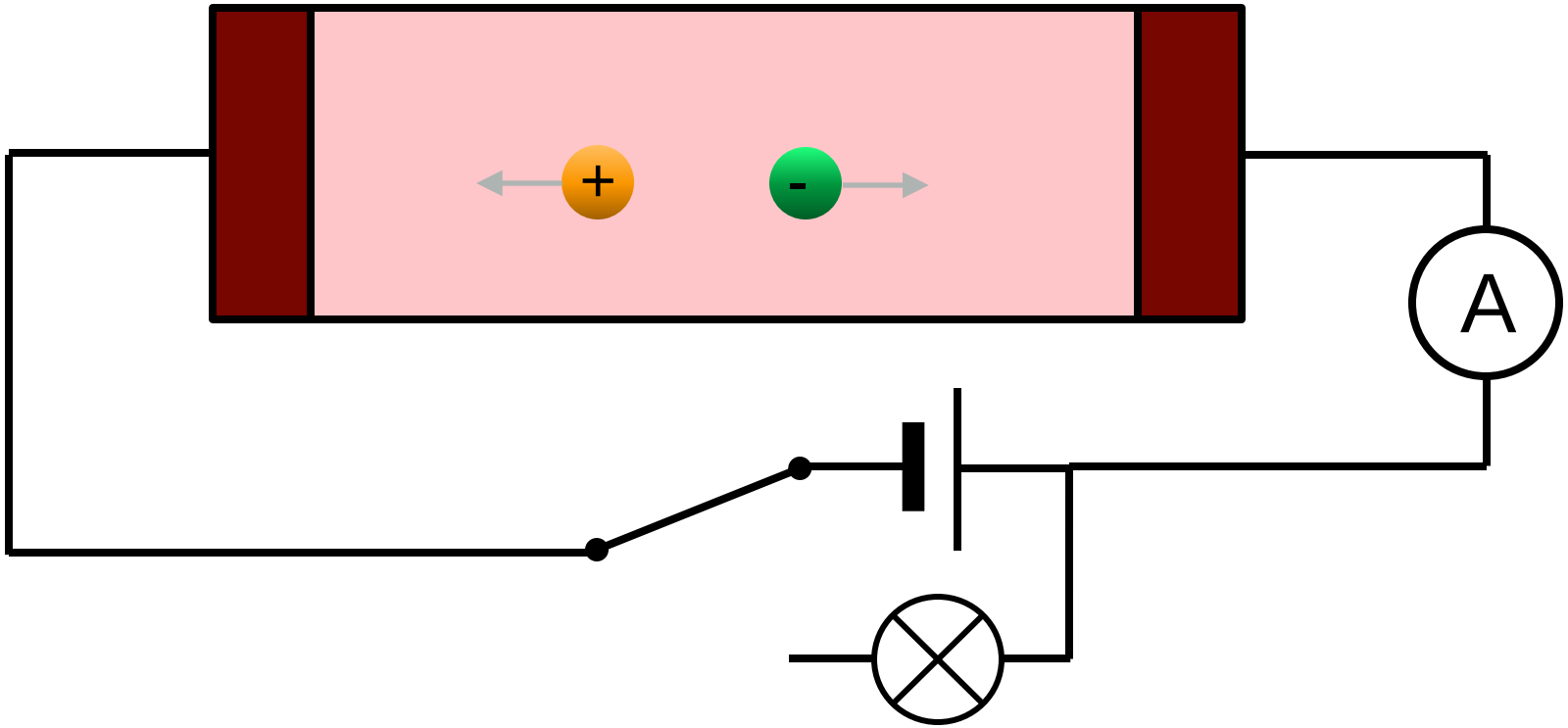
- **Supercapacitors:**
  - buffer volatile power supply
  - deliver high power output

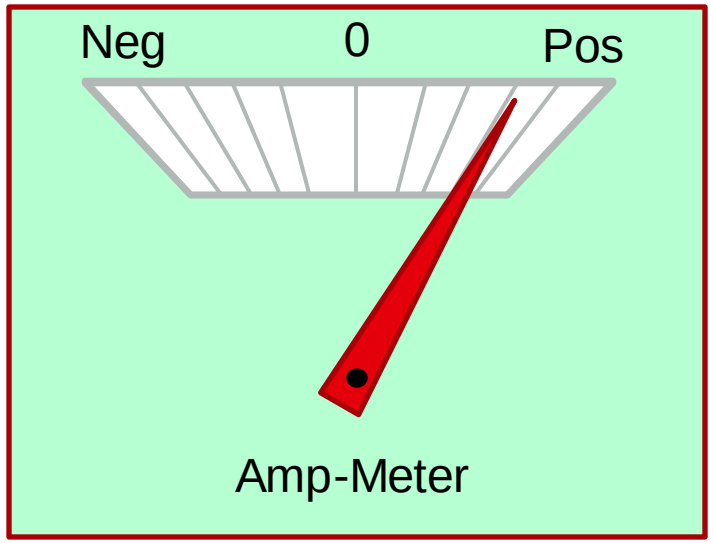
- **Why not integrate a supercap onto a SI-Chip?**
  - ➢Is the technology ready for it?

Agenda

- **Short Roundup about Supercapacitor**
  - Working Principle
  - Structure
- **Si-Based Supercapacitor:**
  - General Design Concepts
  - Design Parameters
  - Fabrication of Pores
  - Overlook Processing Steps
  - Performance Parameters
- **Conclusion**
- **References**

Supercaps: Working Principle



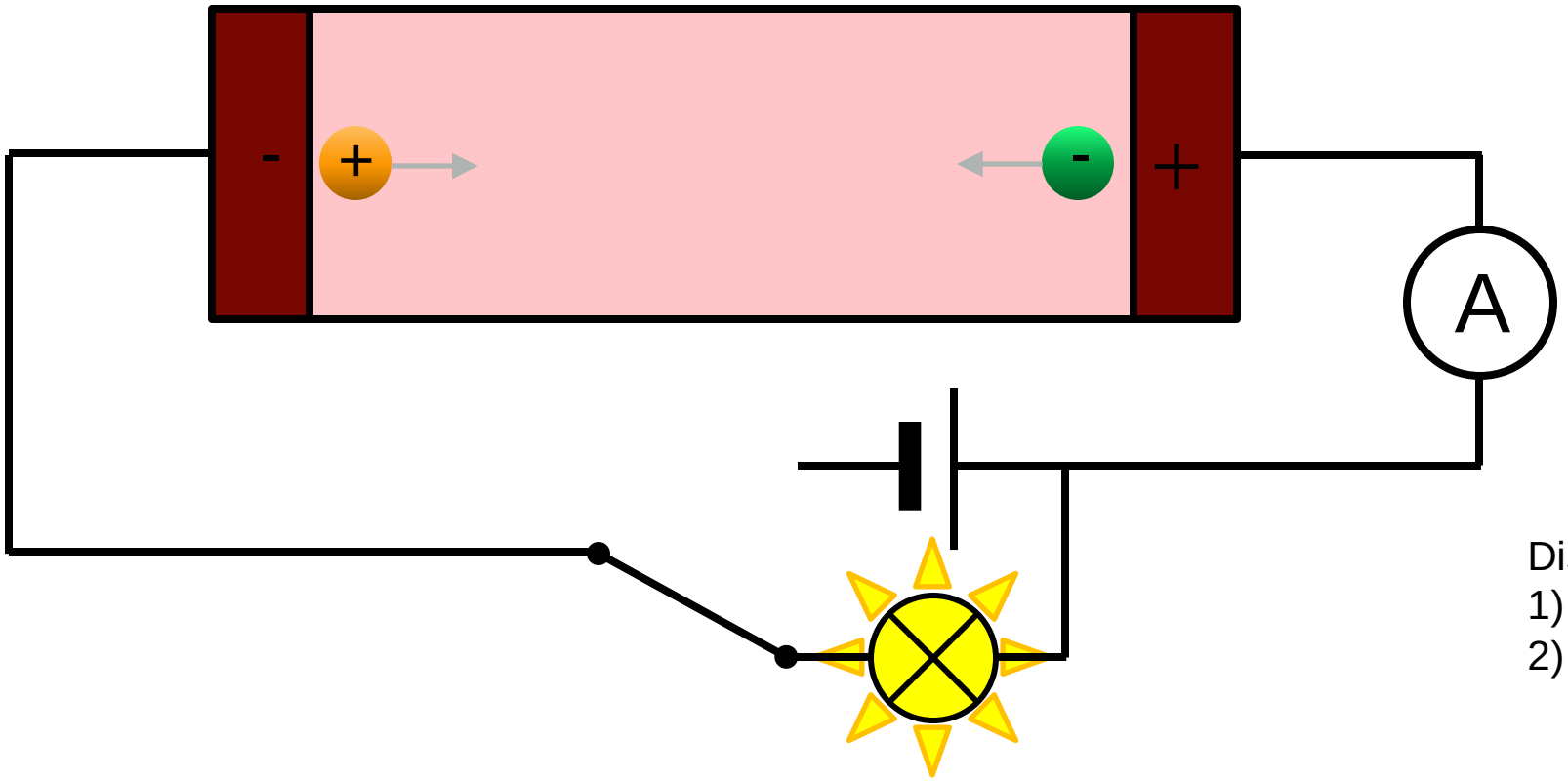


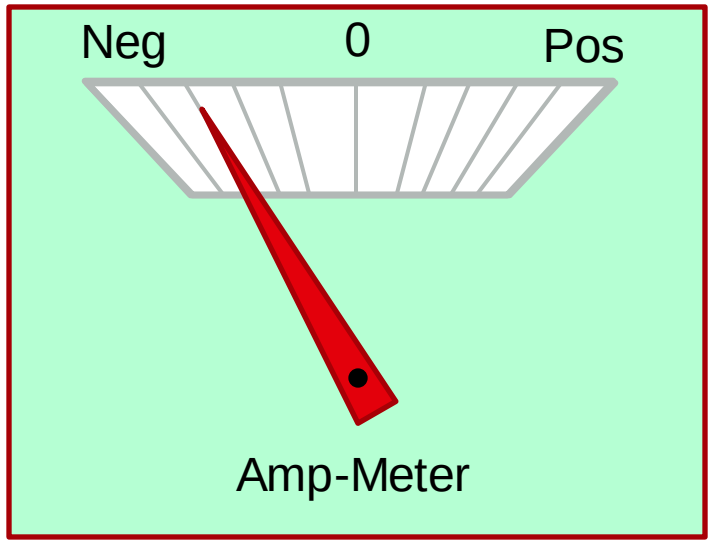
Charging:

1) voltage between plates (i.e. electric field) is applied
2) electric field “tears” charges apart
3) movement of the charges causes a current, provided by the voltage source

Energy storage with short time

Supercaps: Working Principle



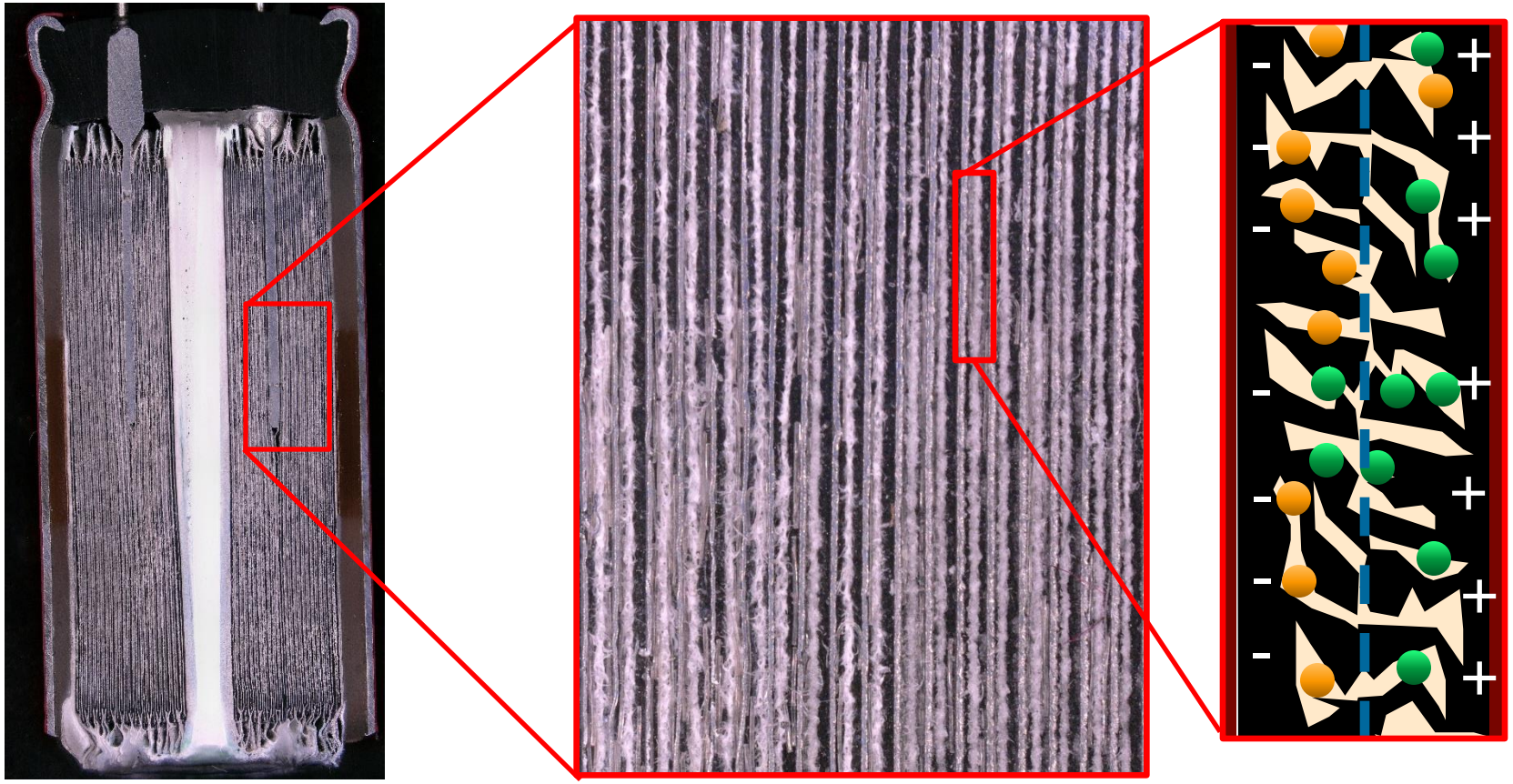


Discharge process:

1) circuit is closed
2) potential difference between the plates, causes electrical current at a certain voltage
3) anion/cations “loose” their mirror charge, leading to charge movement
4) the quicker the anions/cations can be released, the larger the current

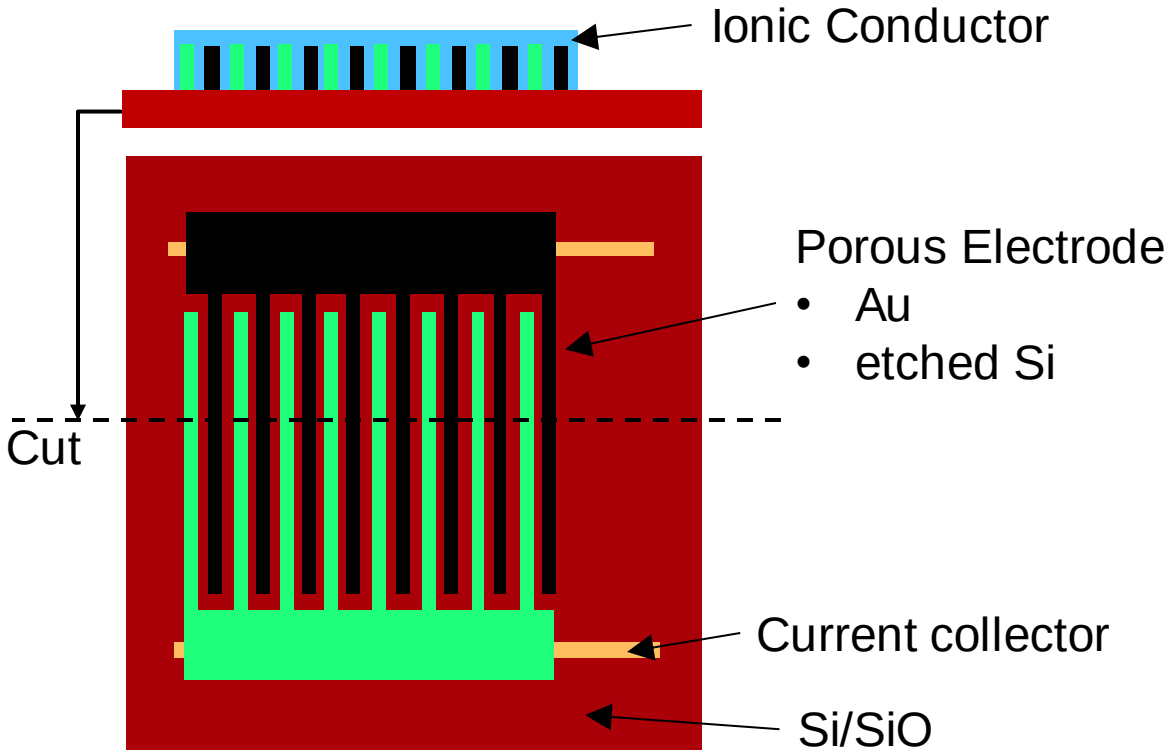
Provides short term electrical power

Commercial Supercaps: Structure

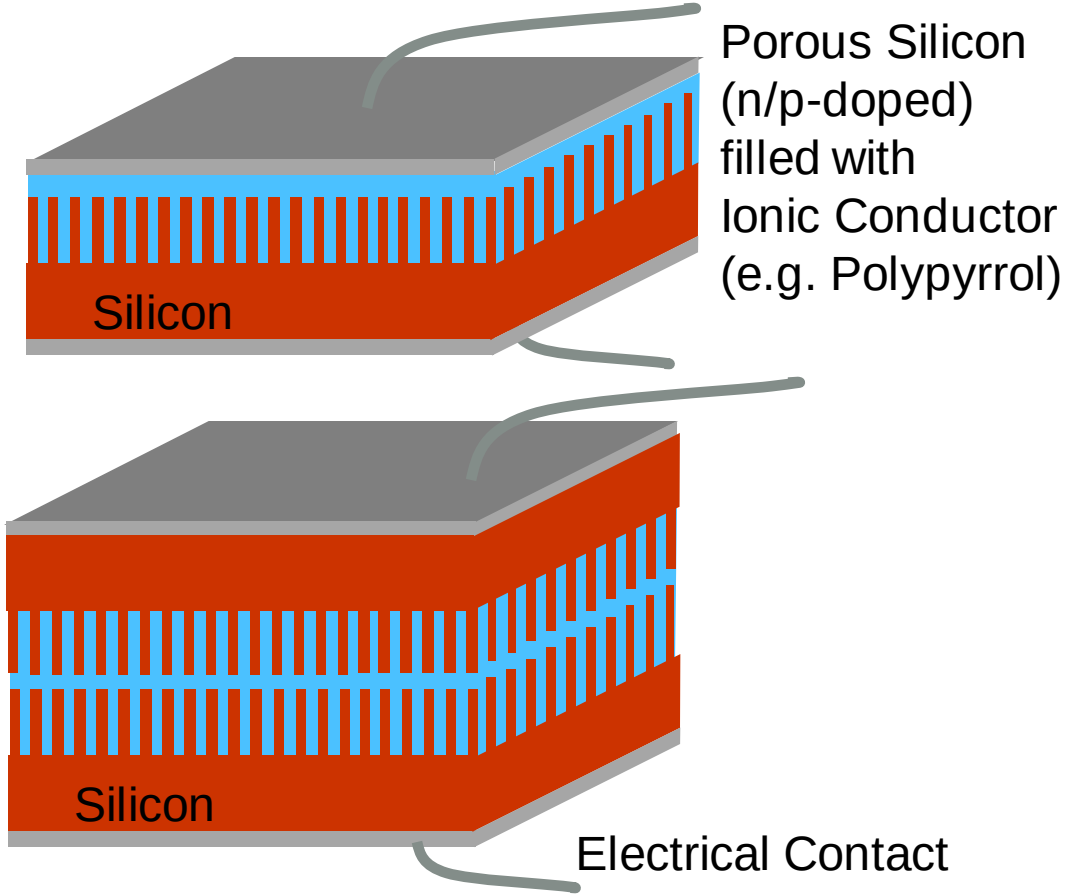


Si-Based SC: General Design

- Lateral Design



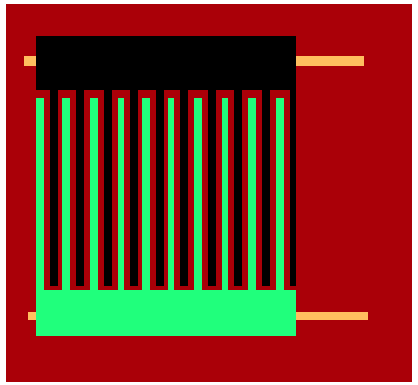
- Vertical Design

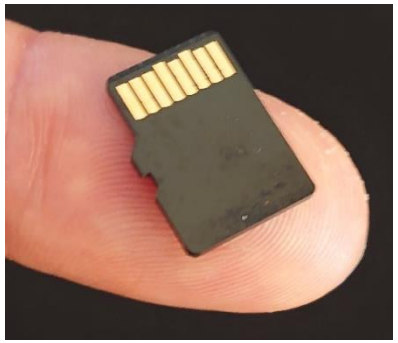


Ref.: *Ferris, A., Bourrier, D., Garbarino, S., Guay, D., Pech, D., Small, 15, 1901224. https://doi.org/10.1002/smll.201901224 (2019)*
Desplobain, S., Gautier, G., Semai, J., Ventura, L. and Roy, M., Phys. Status Solidi (c), 4: 2180-2184. https://doi.org/10.1002/pssc.200674418 (2007)
T. Studemund, Kapazitive Speicherung von elektrischer Energie in der Oxid-stabilisierten inneren Oberfläche mesoporösen Siliziums, Masterarbeit, Beuth Hochschule für Technik (2020)

Si-Based SC: Design Parameters

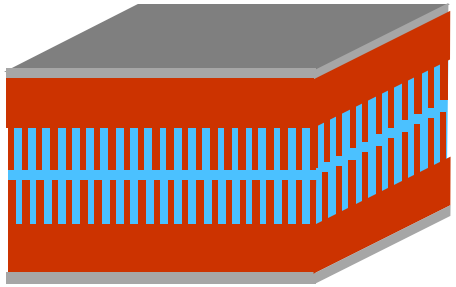
- Lateral Design





- Electrolyte: aqueous, organic, conductive polymers
- Footprint area: 25 mm² - 50 mm²
- Electrode width: 30 µm - 500 µm
- Electrode height: up to 500 µm
- Trench width: 50 µm - 500 µm
- Electrode material: Au, Cu, Silicon
- Electrode modification: ruthenium oxide, …

- Vertical Design

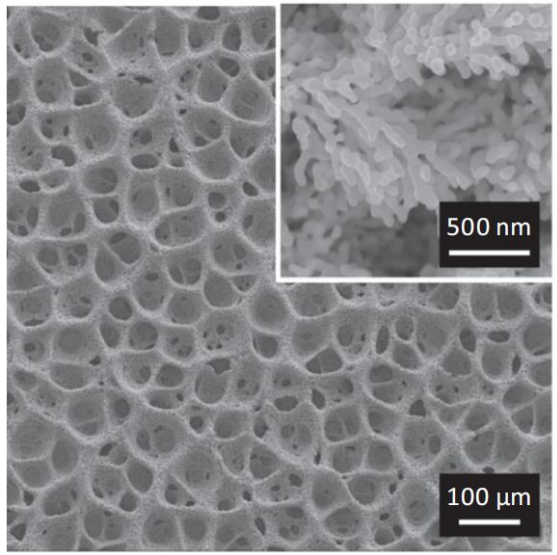


- Electrolyte: aqueous, organic, conductive polymers
- Footprint: up to 100 mm²
- Depth of pores: 7 µm -10 µm
- Separator Membrane: Celgard, Nafion
- Si-base wafer: 400 µm - 500µm
- Electrode material: n,p- doped Silicon
  - Modified with transition metals, carbon and graphite
  - Introduction of blocking layer possible

Si-Based SC: Pore Fabrication

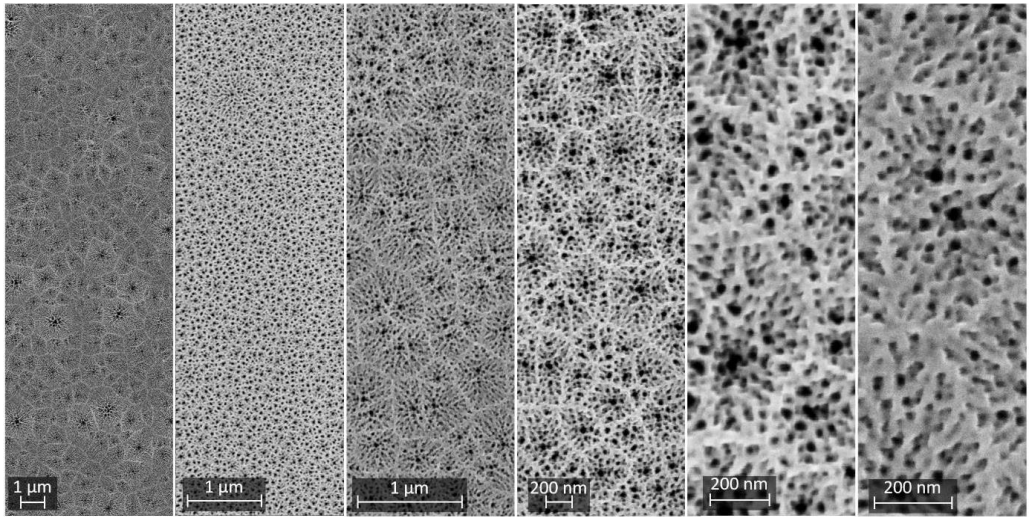
Electrochemical Methods, Examples:

- Dynamic hydrogen bubble template (DHBT)



- Pore Diameters: 100 nm – 100 µm (ca. 100 m²/g)

- Electrocemical etching



- Pore Diameters: 10 nm … 200 nm (porosity 80% about 300 m²/g)

Ref.: *Ferris, A., Bourrier, D., Garbarino, S., Guay, D., Pech, D., Small, 15, 1901224 (2019)*
T. Studemund, Masterarbeit, Beuth Hochschule für Technik Berlin, (2020)

Si-Based SC: Processing

- **Fabrication of pores/electrodes**
  - Dynamic hydrogen bubble template (DHBT)
  - Electrocemical etching
    - Hydrofluoric Acid etching (HF)
    - …

  Scalable

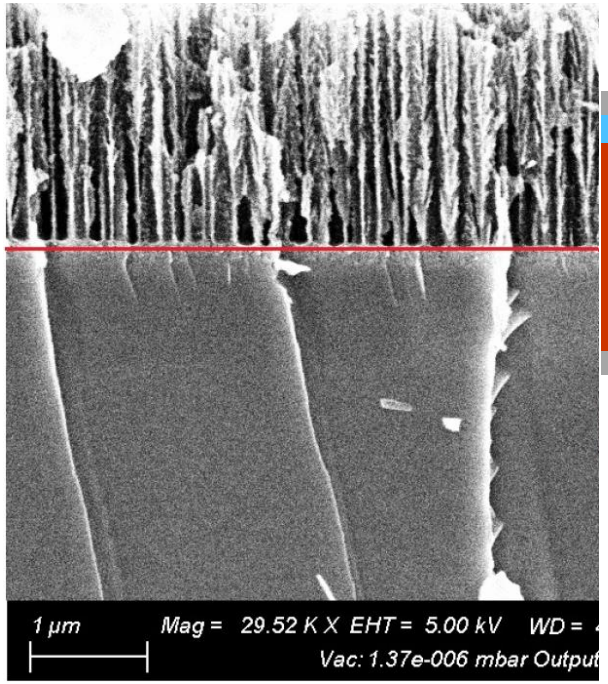
- **Surface treatment/modification**
  - Increase conductivity and pseudo-capacitance, pasivate suface
    - n/p-doping of porous silicon
    - Atomic layer deposition of titanium nitride or other transition metals (metalization)
    - electrochemical deposition of ruthenium oxide ($Ru0_2$)
    - …

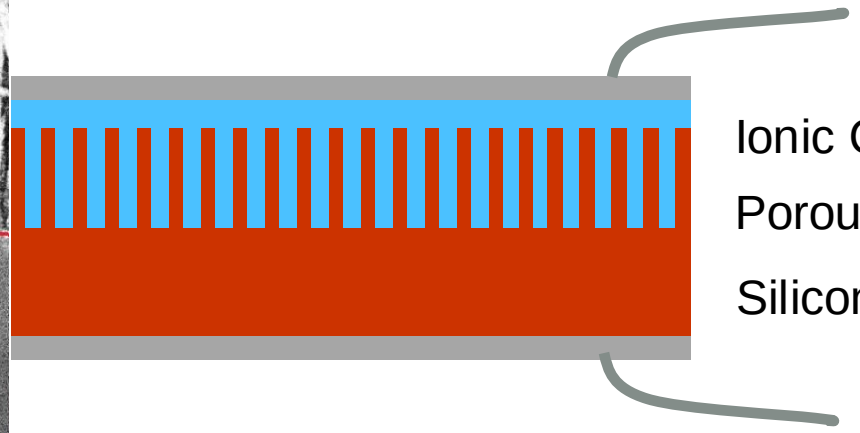
- **Electrolyte**
  - Aqueous and organic solvents with Ions, e.g.:
    - sulfuric acid (H_2SO_4) in H_2O
    - …
  - Ionic liquid, e.g.:
    - 1-ethyl-3-methylimidazolium tetrafluoroborate ($EMIBF_4$)
    - …
  - Conductive Polymers, e.g.:
    - Polypyrrol (PPy)
    - …

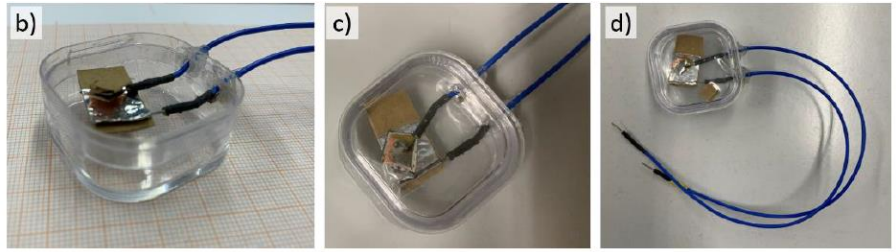
Ref.: *Desplobain, S., Gautier, G., Semai, J., Ventura, L., and Roy, M., Phys Stat Sol 4, 2180-2184 (2007)*
Oakes, L., Westover, A., Mares, J.W., Chatterjee, S., Ervin, W..R,, Bardhan R., Weiss,. SM., and Pint, C.L.,Sci Rep 3, 3020 (2013)
Kestutis Grigoras, Leif Grönberg, Jouni Ahopelto, and Mika Prunnila, Proc. SPIE 10246, Smart Sensors, Actuators, and MEMS VIII, 102460Z (2017)
Wei Sun, Ruilin Zheng, & Xuyuan Chen. Three Dimensional MEMS Supercapacitor Fabricated by DRIE on Silicon Substrate (Version 12040) (2009)

Si-Based SC: Electrochemical Etching

Scanning Electron Microscopy







Cooperation:

BEUTH HOCHSCHULE FÜR TECHNIK BERLIN University of Applied Sciences

WÜRTH ELEKTRONIK

htw. Hochschule für Technik und Wirtschaft Berlin University of Applied Sciences

RHEFOR

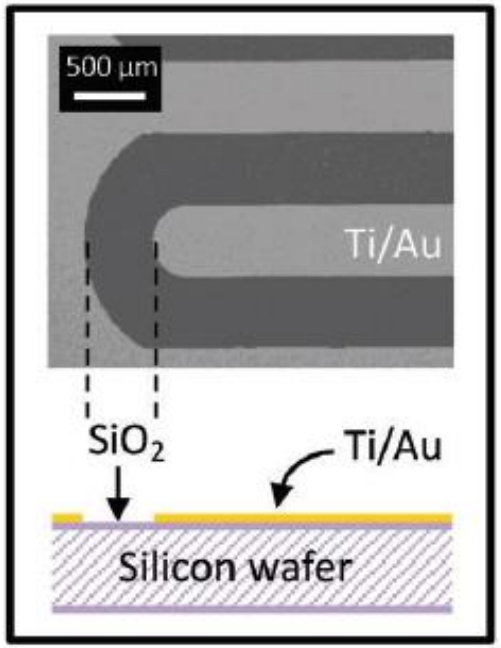
Ref.: *T. Studemund, Kapazitive Speicherung von elektrischer Energie in der Oxid-stabilisierten inneren Oberfläche mesoporösen Siliziums, Masterarbeit, Beuth Hochschule für Technik (2020)*

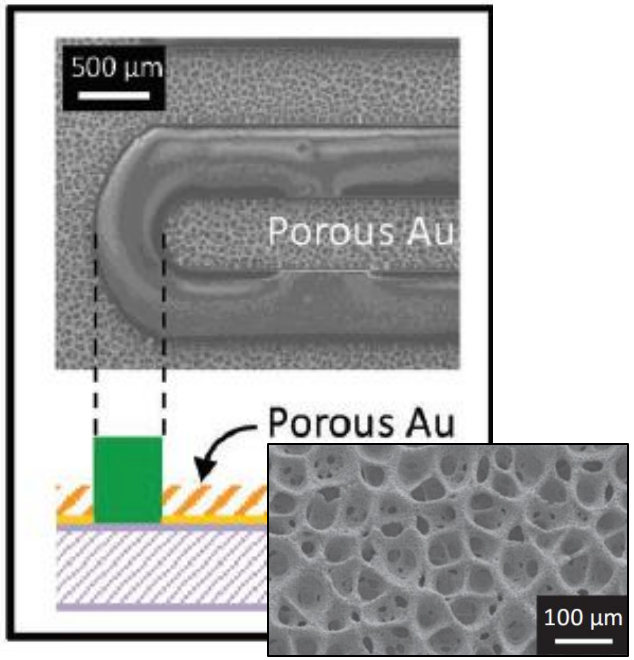
N. A. Kotitschke, Untersuchung der elektrischen Eigenschaften großflächiger Sperrschichten in mesoporösen Silizium, Masterarbeit, Beuth Hochschule für Technik Berlin (2019)

Si-Based SC: DHBT

Dynamic Hydrogen Bubble Template (DHBT) & etching

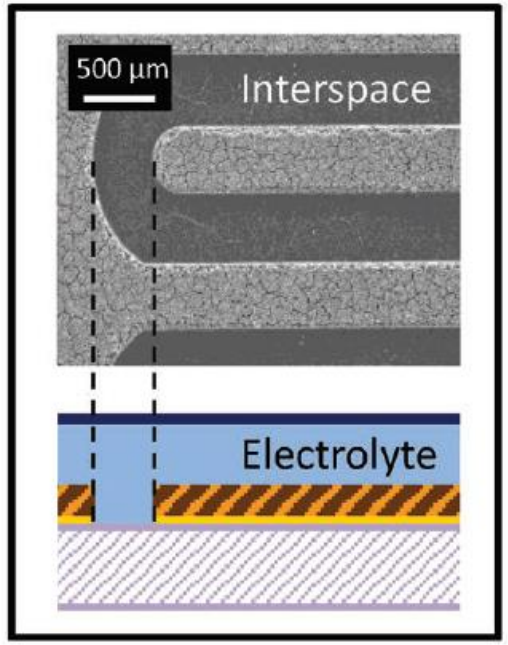
photolithographic deposition sublayer on oxidized Si-wafer

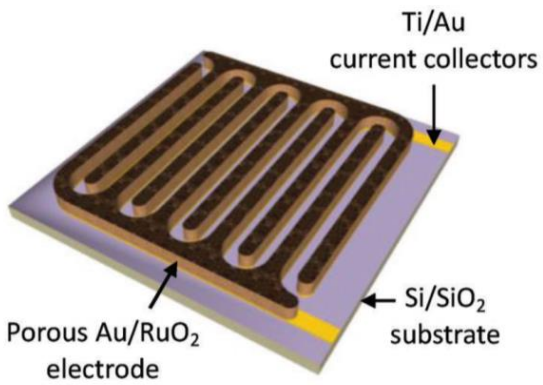




Forming µ-porous Au-Cu metal film (macro-porous gold film with large surface area)

deposition of ruthenium oxide (RuO_2)





Application of electrolyte: 0.5 M H_2SO_4 or doped polyvinyl alcohol (PVA)

Ref.: *Ferris, A., Bourrier, D., Garbarino, S., Guay, D., Pech, D., Small 2019, 15, 1901224.* *https://doi.org/10.1002/smll.201901224*

Electrical Parameter

Parameters based on footprint area of the electrical device

	Porous Gold, RuO_2 [1]	Porous Silicon, TiN [2]	n-doped - Silicon based [3]	p-doped - Silicon based [4]	Activated Carbon, comm.
	Lateral Design		Vertical Design		Avg.
Footprint Area [mm²]	45	25	9.42	100	400
C [mF/cm²]	812	3	318	0.14	6250
ESR, AC [Ohm/cm²]	1.3	20	106	3.9	0.0025

TRL 4, next: validation in relevant environment

- Similar performance also reached by other researcher

- Demonstrators have been build and results have been published
- Short term power supply for ICs ($\approx 100\ mW$) possible
- Next steps:
  - Optimization geometry/electrolyte
  - Adaptation of scalable processes
  - Developing of suitable encapsulation
  - …

[1] Ferris, A., Bourrier, D., Garbarino, S., Guay, D., Pech, D., Small, 15, 1901224. (2019)
[2] Kestutis Grigoras, Leif Grönberg, Jouni Ahopelto, and Mika Prunnila, Proc. SPIE 10246, Smart Sensors, Actuators, and MEMS VIII, 102460Z (2017);
[3] T. Studemund, Kapazitive Speicherung von elektrischer Energie in der Oxid-stabilisierten inneren Oberfläche mesoporösen Siliziums, Masterarbeit, Beuth Hochschule für Technik, (2020)
[4] Desplobain, S., Gautier, G., Semai, J., Ventura, L., and Roy, M., Phys Stat Sol 4, 2180-2184 (2007).

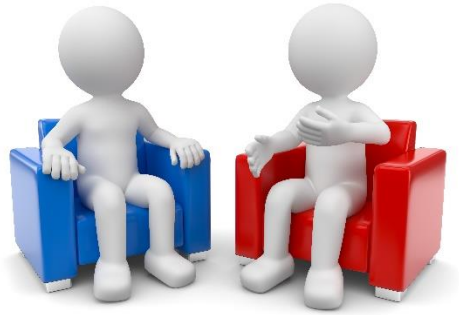
Conclusion

- **Proof of concept and demonstrators are available**
  - Easy to miniaturize
  - Depending on electrolyte higher operation temperature possible

- **Energy storage capabilities are low compared to standard Supercapacitor**
  - HOWEVER, sufficient for some ICs!

- **Could this replace conventional supercapacitors?**
  - We think it has potential,

    …however, what do you think?
  - Have I missed something?



OPINIONS?

QUESTIONS?

THANK YOU

FOR YOUR ATTENTION!

IDEAS?

REMARKS?

Further References

Your Home Work.

- Ferris, A., Bourrier, D., Garbarino, S., Guay, D., Pech, D., 3D Interdigitated Microsupercapacitors with Record Areal Cell Capacitance. Small, 15, 1901224. https://doi.org/10.1002/smll.201901224 (2019)
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- *Plowman, Blake J. and Jones, Lathe A. and Bhargava, Suresh K., Building with bubbles: the formation of high surface area honeycomb-like films via hydrogen bubble templated electrodeposition, Chem. Commun.*, 51, 4331-4346 (2015)
- Wen Zheng, "Fabrication of Capacitors Based on Silicon Nanowire Arrays Generated by Metal-Assisted Wet Chemical Etching", Thesis, B.S. Department of Chemistry, Tsinghua University (2010)

Further References

Your Home Work.

- *T. Studemund, "Kapazitive Speicherung von elektrischer Energie in der Oxid-stabilisierten inneren Oberfläche mesoporösen Siliziums", Masterarbeit, Beuth Hochschule für Technik Berlin, (2020)*
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- Kui-Qing Peng, Xin Wang, Li Li, Ya Hu, Shuit-Tong Lee, Silicon nanowires for advanced energy conversion and storage, Nano Today, 8, Issue 1, 75-97, https://doi.org/10.1016/j.nantod.2012.12.009, (2013)

Repository

Deep reactive-ion etching

The Bosch process, named after the German company Robert Bosch GmbH which patented the process,[1][2][3] also known as pulsed or time-multiplexed etching, alternates repeatedly between two modes to achieve nearly vertical structures:

1. A standard, nearly isotropic plasma etch. The plasma contains some ions, which attack the wafer from a nearly vertical direction. Sulfur hexafluoride [SF_6] is often used for silicon.
2. Deposition of a chemically inert passivation layer. (For instance, Octafluorocyclobutane [C_4F_8] source gas yields a substance similar to Teflon.)

Applications

RIE "deepness" depends on application:

- in DRAM memory circuits, capacitor trenches may be 10–20 µm deep,
- in MEMS, DRIE is used for anything from a few micrometers to 0.5 mm.

https://en.wikipedia.org/wiki/Deep_reactive-ion_etching

Metal-assisted chemical Etching (MACE, MacEtch)

Metal-assisted Chemical Etching (MacEtch) is a novel nanofabrication method (Appl. Phys. Lett. 77, 2572 (2000) and Patent US#6,790,785.) to produce extremely high aspect ratio semiconductor nanostructures including Si, Ge, GaAs, InGaAs, InP, SiC, GaN, Ga2O3 homo- and hetero-junctions.

It uses noble metal (such as Au, Pt and Ag) deposited on the surface of a semiconductor (e.g. Si) as a catalyst to catalyze the hole (h+) generation from an oxidant (such as H2O2) in an acidic (or basic) solution (such as HF) to induce local oxidation (Si + 4h+ --- Si4+) and reduction (2H+ + 2e- --- H2) reactions.
This results in the removal of semiconductor materials without net consumption of the metal.
Under controlled conditions, the reactions occur only at the interface between metal and the semiconductor.
As a result, metal descends into the semiconductor as the semiconductor is being etched right underneath, acting as a negative resist etch mask.
MacEtch is essentially a wet etching method yet produces anisotropic high aspect ratio semiconductor micro and nanostructures without incurring lattice damage.

http://mocvd.ece.illinois.edu/research/MacEtch.html

Si-Based SC: Processing

- **Fabrication of pores/electrodes**
  - Dynamic hydrogen bubble template (DHBT)
  - Electrocemical etching
    - Hydrofluoric Acid etching (HF)
    - deep reactive ion etching (DRIE)
    - Metal assisted chemical etching (MACE)

- **Surface treatment/modification**
  - Increase conductivity and pseudo-capacitance, pasivate suface
    - n/p-doping of porous silicon
    - Atomic layer deposition of titanium nitride or other transition metals (metalization)
    - electrochemical deposition of ruthenium oxide ($Ru0_2$)
    - Formation of carbone/graphite on Si-pores using high temperatures >600°C
    - chemical vapor deposition synthesis of vertically oriented graphenenanosheets

- **Electrolyte**
  - Aqueous and organic solvents with Ions, e.g.:
    - sulfuric acid (H_2SO_4) in H_2O
    - Lithium perchlorate $LiClO_4$ in Dimethyl carbonate (DMC)
  - Ionic liquid, e.g.:
    - 1-ethyl-3-methylimidazolium tetrafluoroborate ($EMIBF_4$)
    - 1-ethyl-3-methylimidazolium dicyanamide (EMI-DCA)
  - Conductive Polymers, e.g.:
    - Polypyrrol (PPy)
    - Poly(3,4-ethylenedioxythiophene) (PEDOT)

Ref.: *Desplobain, S., Gautier, G., Semai, J., Ventura, L., and Roy, M., Phys Stat Sol 4, 2180-2184 (2007)*
Oakes, L., Westover, A., Mares, J.W., Chatterjee, S., Ervin, W..R,, Bardhan R., Weiss,. SM., and Pint, C.L.,Sci Rep 3, 3020 (2013)
Kestutis Grigoras, Leif Grönberg, Jouni Ahopelto, and Mika Prunnila, Proc. SPIE 10246, Smart Sensors, Actuators, and MEMS VIII, 102460Z (2017)
Wei Sun, Ruilin Zheng, & Xuyuan Chen. Three Dimensional MEMS Supercapacitor Fabricated by DRIE on Silicon Substrate (Version 12040) (2009)

Si-Based SC: Electrochemical Etching

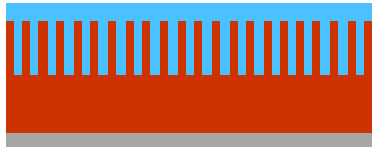
Electrochemical Method

- Electrochemical etching and doping:

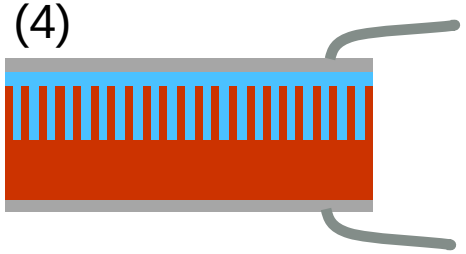
1) Electrochemical etching of silicon in hydrofluoric acid (HF) solution
2) n-Doping: plasma-enhanced chemical vapor deposition (PECVD) with Phosphorus
3) polymer infiltration, polymerization of pyrrol (or alternative conductive polymers, electrolyte)
4) Apply top electrode and Electrical contacting

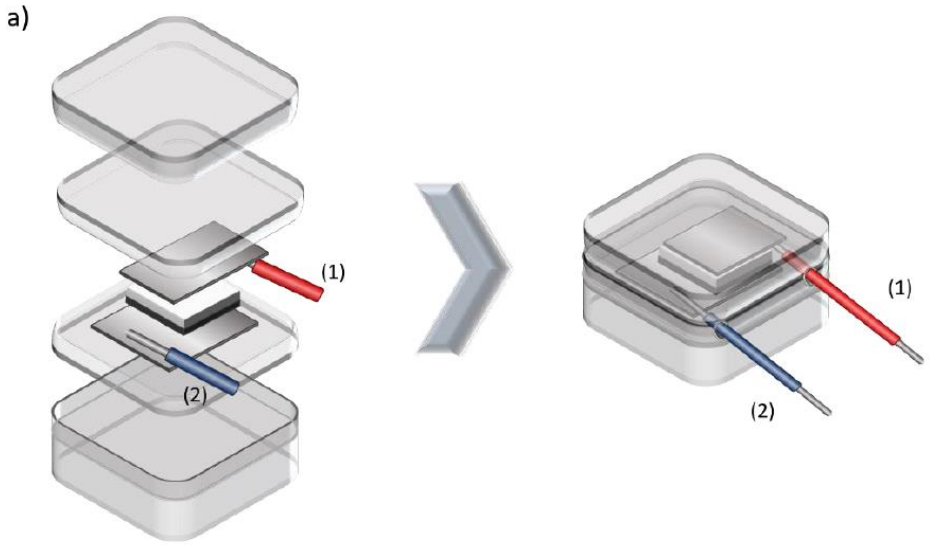
(1 - 2)

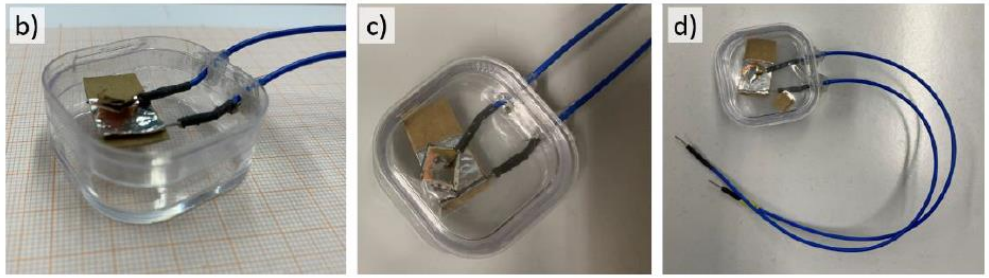
(3)



(4)







Cooperation:

BEUTH HOCHSCHULE FÜR TECHNIK BERLIN University of Applied Sciences

WÜRTH ELEKTRONIK

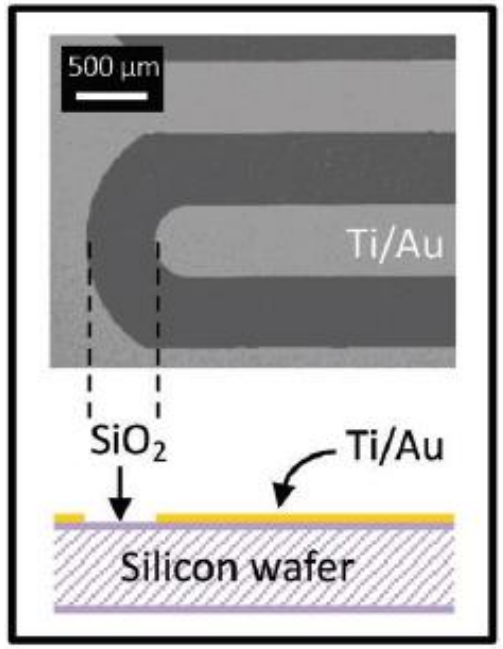
htw. Hochschule für Technik und Wirtschaft Berlin University of Applied Sciences

RHEFOR

Ref.: *T. Studemund, Kapazitive Speicherung von elektrischer Energie in der Oxid-stabilisierten inneren Oberfläche mesoporösen Siliziums, Masterarbeit, Beuth Hochschule für Technik (2020)*

Si-Based SC: DHBT

(1)



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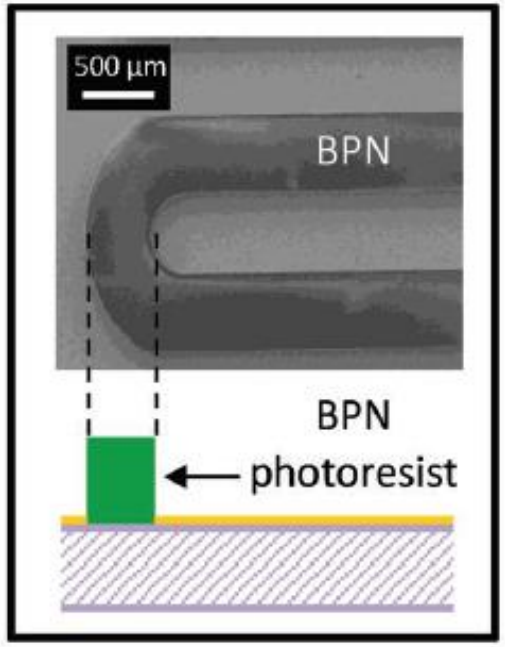
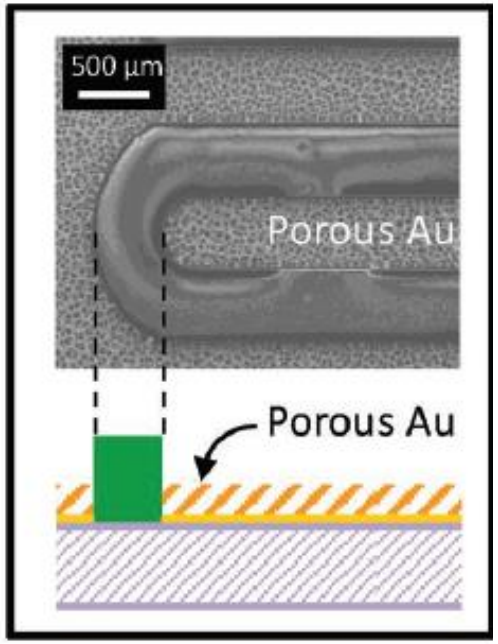


(3-5)



Electrochemical Method

- dynamic hydrogen bubble template (DHBT) & etching

(1) Pholithographical deposition of Ti/Au sublayer on oxidized Si-wafer

(2) Deposition of protective photoresist

(3) Deposition form Au^{3+} Cu^{2+} acid aqueous solution at applied cathodic over potential to trigger hydrogen evolution

(4) Forming µ-porous Au-Cu metal film

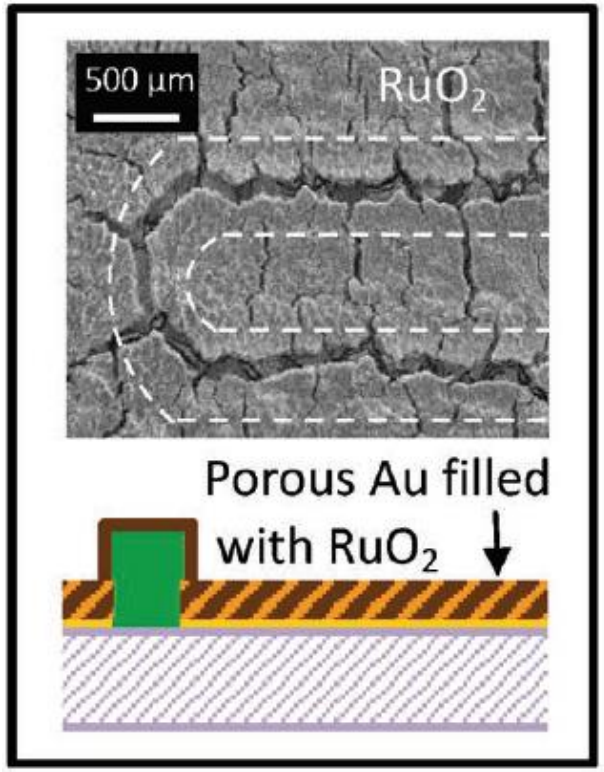
(5) Increasing pore size and surface area by electro chemical etching of Cu

<u>Result:</u> macro-porous gold film with large surface area

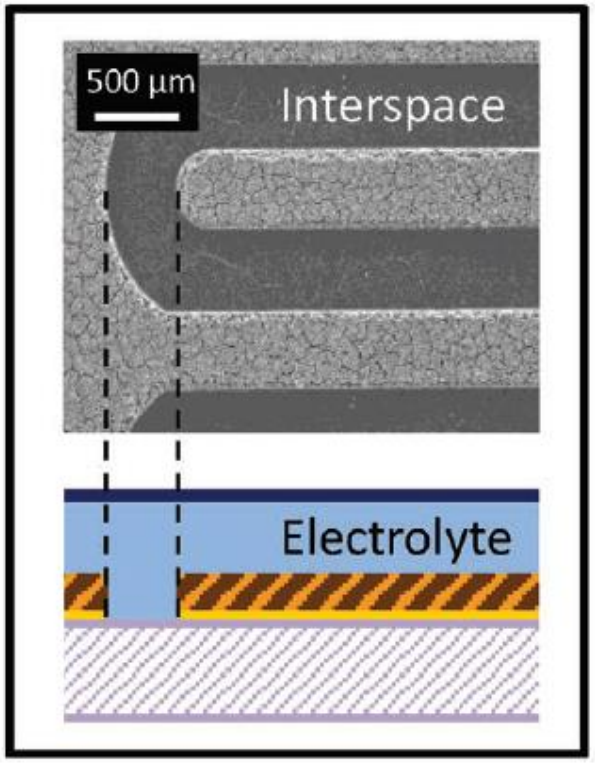
Ref.: *Ferris, A., Bourrier, D., Garbarino, S., Guay, D., Pech, D., Small 2019, 15, 1901224.* *https://doi.org/10.1002/smll.201901224*

Si-Based SC: DHBT

(6)



(7-8)



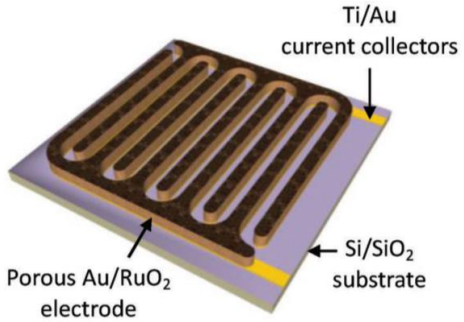
Electrochemical Method

- dynamic hydrogen bubble template (DHBT) & etching

(6) electrochemical deposition of ruthenium oxide ($Ru0_2$)

(7) Removal of photoresist spacer

(8) Application of electrolyte: 0.5 M H_2SO_4 or doped polyvinyl alcohol (PVA)



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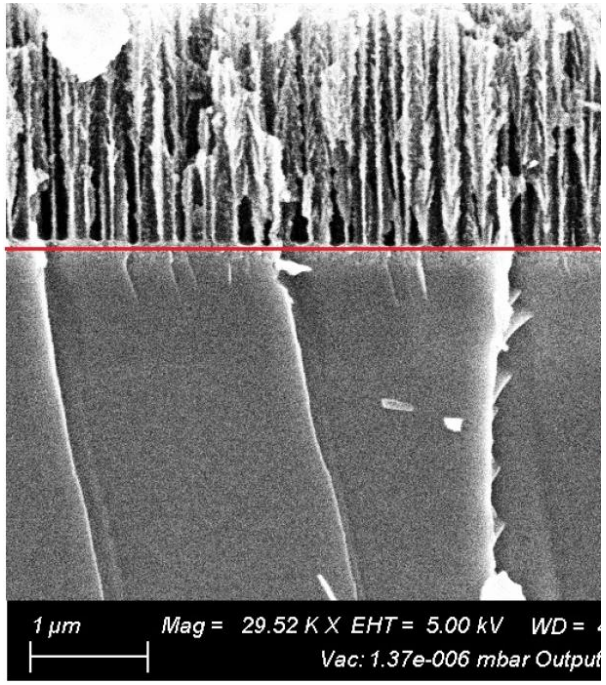
Si-Based SC: Forming of Pores

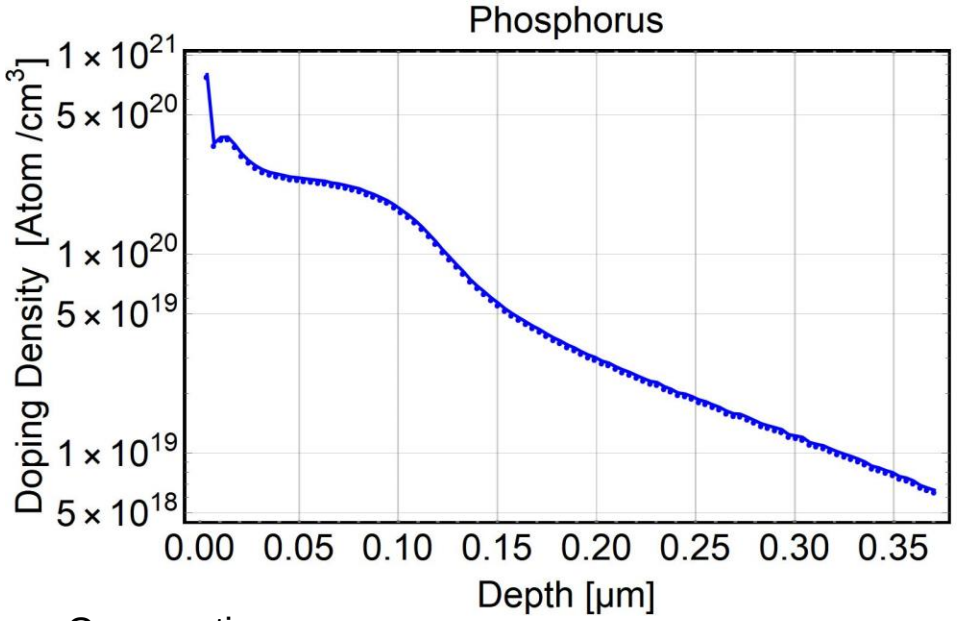
pores in silicon through the use anodization cell

Scanning Electron Microscopy



Increase conductivity with n-doping: plasma-enhanced chemical vapor deposition (PECVD) with Phosphorus

Secondary ion mass spectrometry



Cooperation:

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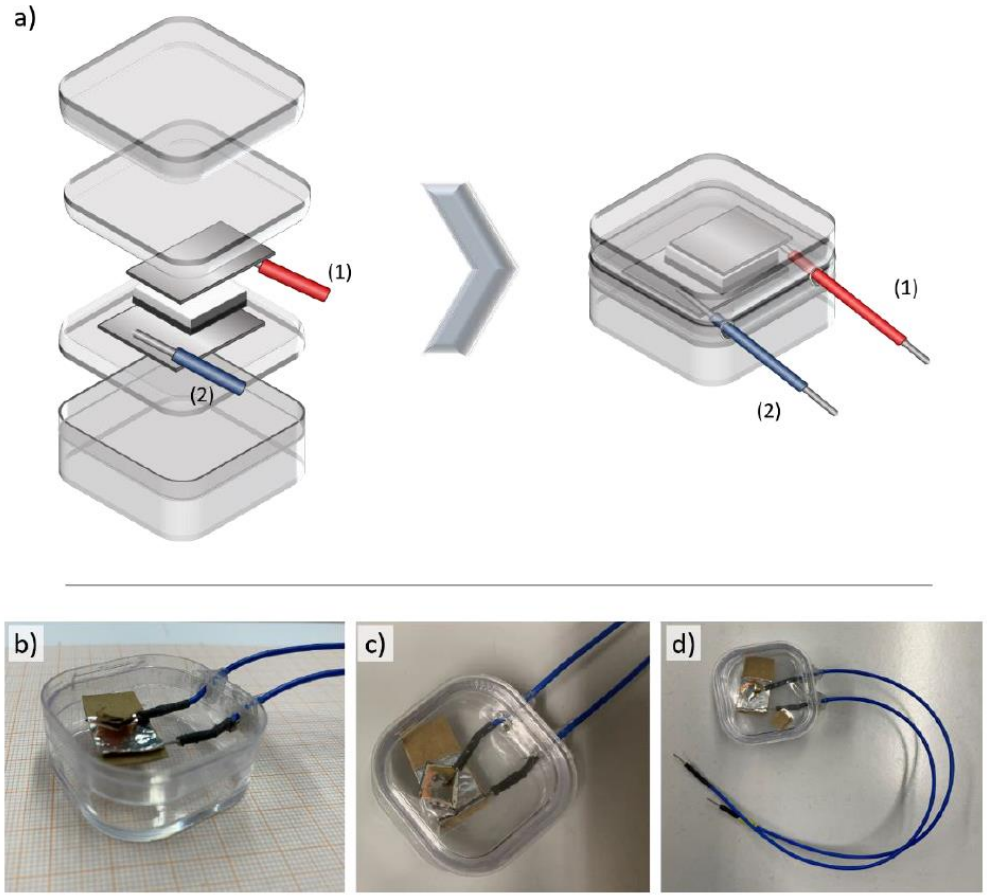
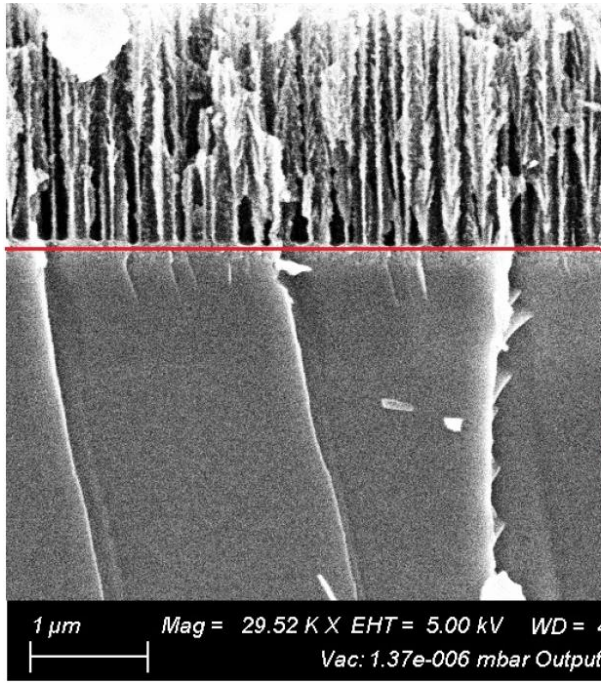
N. A. Kotitschke, Untersuchung der elektrischen Eigenschaften großflächiger Sperrschichten in mesoporösen Silizium, Masterarbeit, Beuth Hochschule für Technik Berlin, 2019

Si-Based SC: Forming of Pores





Electrochemical Method

- Electrochemical etching and Doping

1) Electrochemical etching of silicon in hydrofluoric acid (HF) solution
2) n-Doping: plasma-enhanced chemical vapor deposition (PECVD) with Phosphorus
3) polymer infiltration, polymerization of pyrrol (or alternative conductive polymers, electrolyte)
4) Electrical contacting

Cooperation:

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T. Studemund, Kapazitive Speicherung von elektrischer Energie in der Oxid-stabilisierten inneren Oberfläche mesoporösen Siliziums, Masterarbeit, Beuth Hochschule für Technik, 2020

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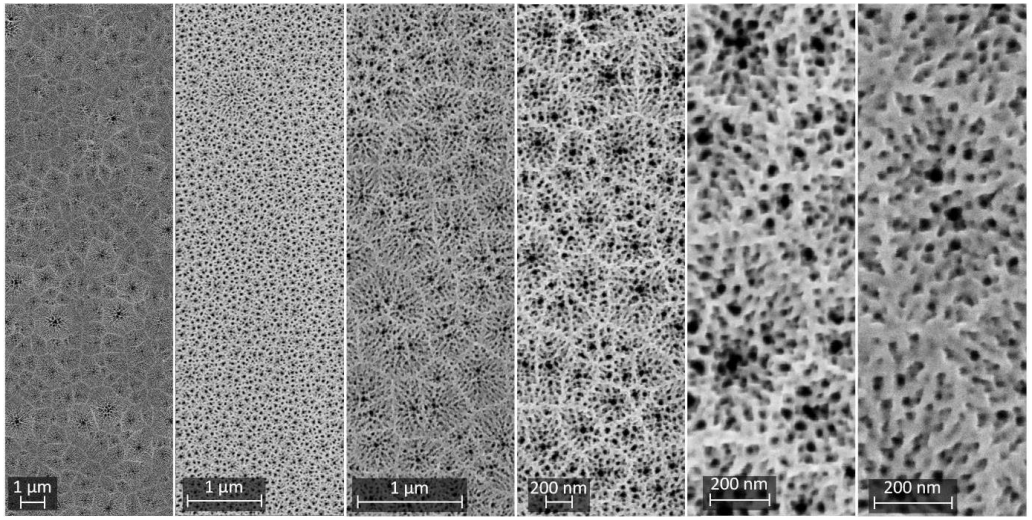

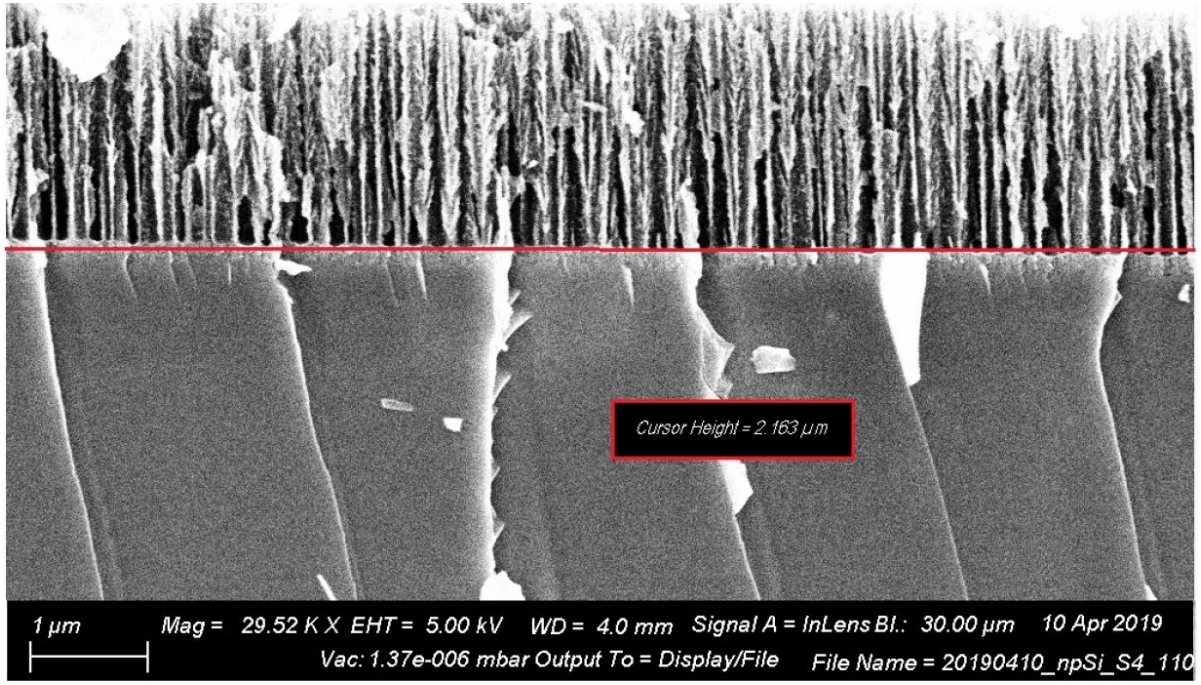

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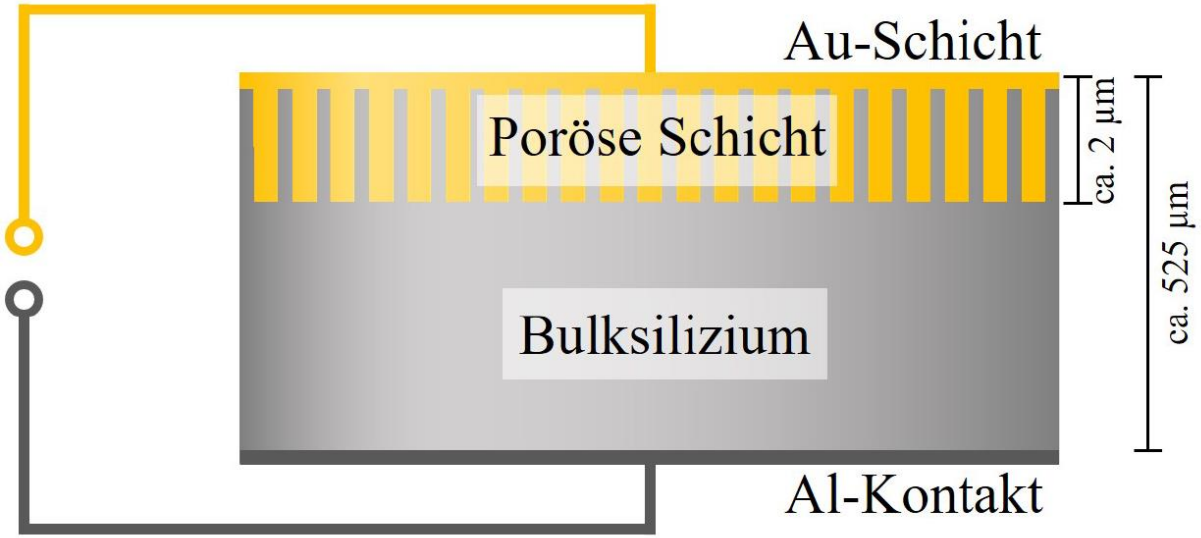

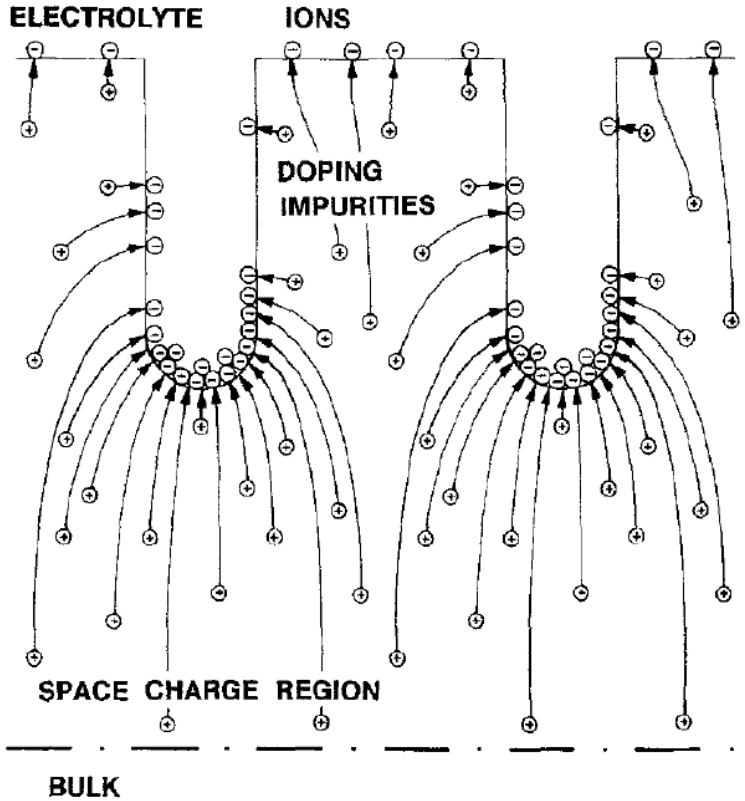

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A. Creuz, Design und Aufbau eines Ultrakondensators basierend auf porösen Festkörperstrukturen, Masterarbeit, Beuth Hochschule für Technik Berlin, 2017