Texas Instruments

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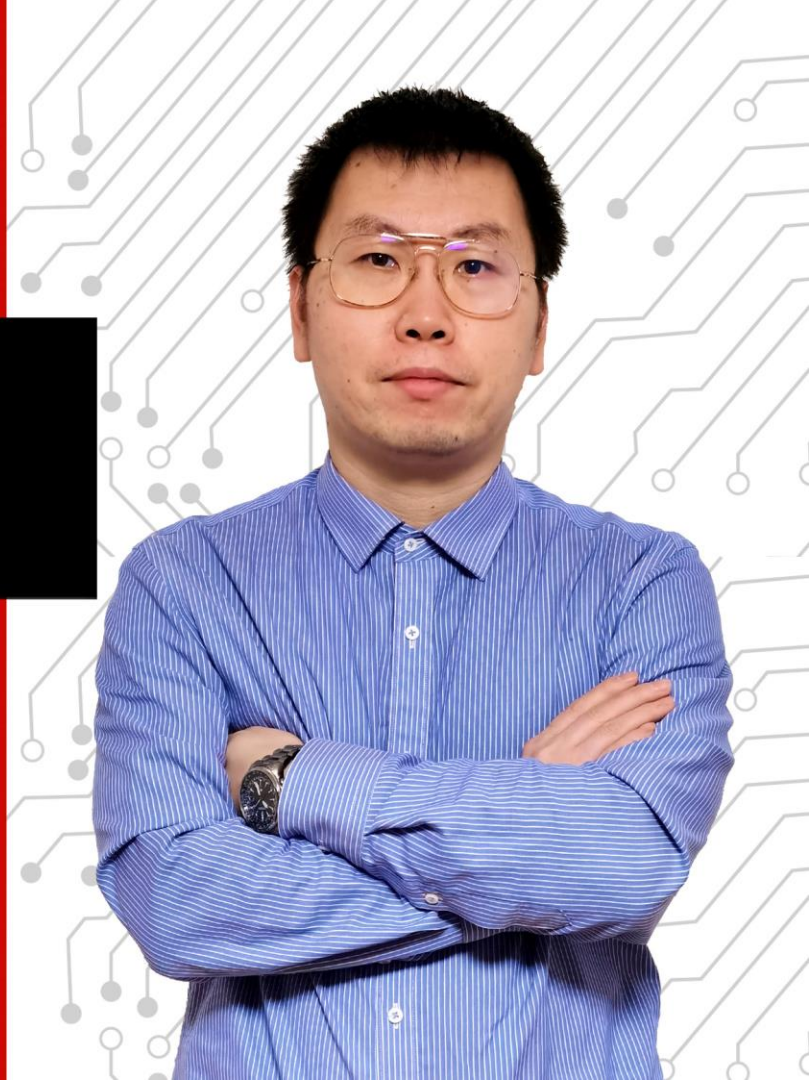
DESHENG GUO

HIGH-EFFICIENCY 4-kW SINGLE-PHASE CCM TOTEM-POLE PFC DESIGN



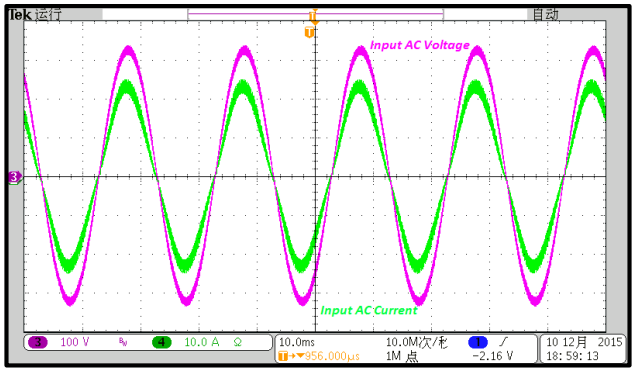
Agenda

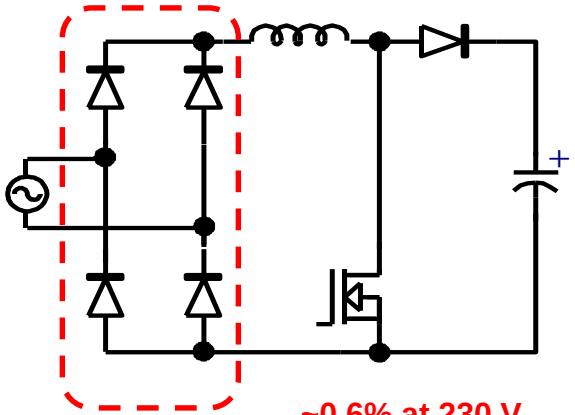
- **Background:** Why choose Totem-pole PFC and common concerns
- **4kW Totempole PFC design and test results**
  - Efficiency and deadtime influence
  - AC drop response
  - Surge test
  - EMI-CE & Thermal test
- **Conclusion**

Why choose totem-pole PFC?

Background

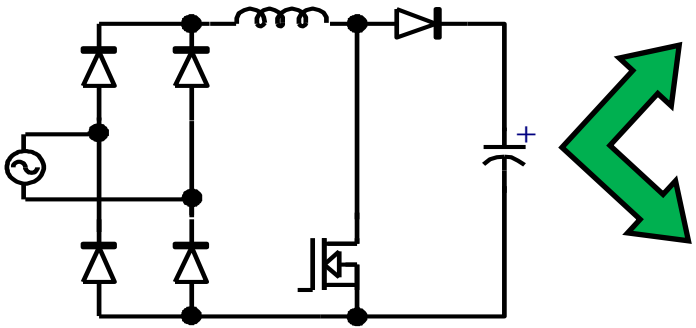
- PFC is widely used in AC/DC applications as a front stage to improve power factor and iTHD.
- Bridge diode loss is a key part in total losses.





~0.6% at 230 V
~1.5% at 90 V

Technologies to improve PFC efficiency



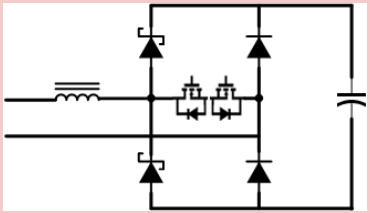
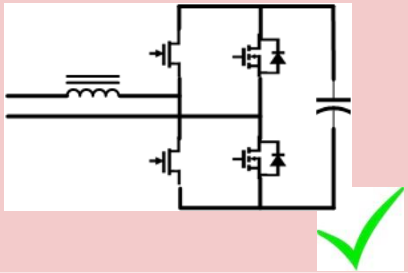
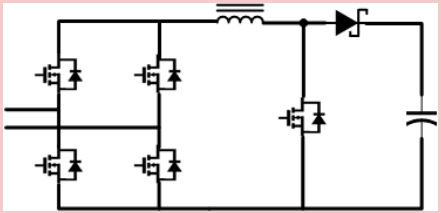
Active bridge rectifier

Bridgeless

- AC switch bridgeless
- Totem-pole bridgeless

Which one is the future?

PFC technology comparison

	AC switch PFC	Totem-pole PFC	Active bridge PFC
Block diagram			
Details	2 silicon diodes 2 MOSFETs 2 silicon diodes or SiC diodes 1 choke coil	2 **GaN FETs** or SiC MOSFETs 2 MOSFETs 1 choke coil	5 MOSFETs 1 silicon diodes or SiC diodes 1 choke coil
Cost	**Middle**	**Lowest in future**	**High**
Efficiency	On-time: 2 MOSFETs Off-time: 1 SiC diode + 1 silicon diode	On-time: 1 MOSFET + 1 FET Off-time: 1 MOSFET + 1 FET	On-time: 3 MOSFETs Off-time: 2 MOSFETs + 1 diode
	~98.7%	**~99.0%**	**~98.5%**

Common concerns about totem-pole PFC

- What is the **efficiency** performance of GaN FETs?
- How is the power stage and control in the **AC drop** test?
- What is the real risk in the **lighting surge** test?
- What is the **EMI/CE and thermal** performance of totem-pole PFC with GaN?

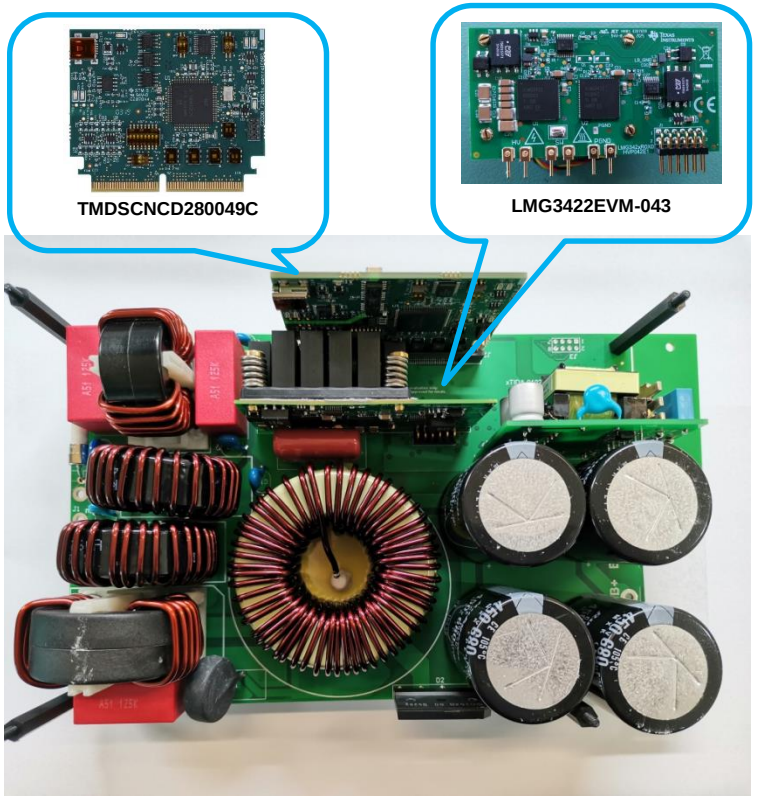
Let’s find out these answers in the following slides.

4kW totem-pole PFC design and test result

4-kW design of a CCM totem-pole PFC

Design parameters

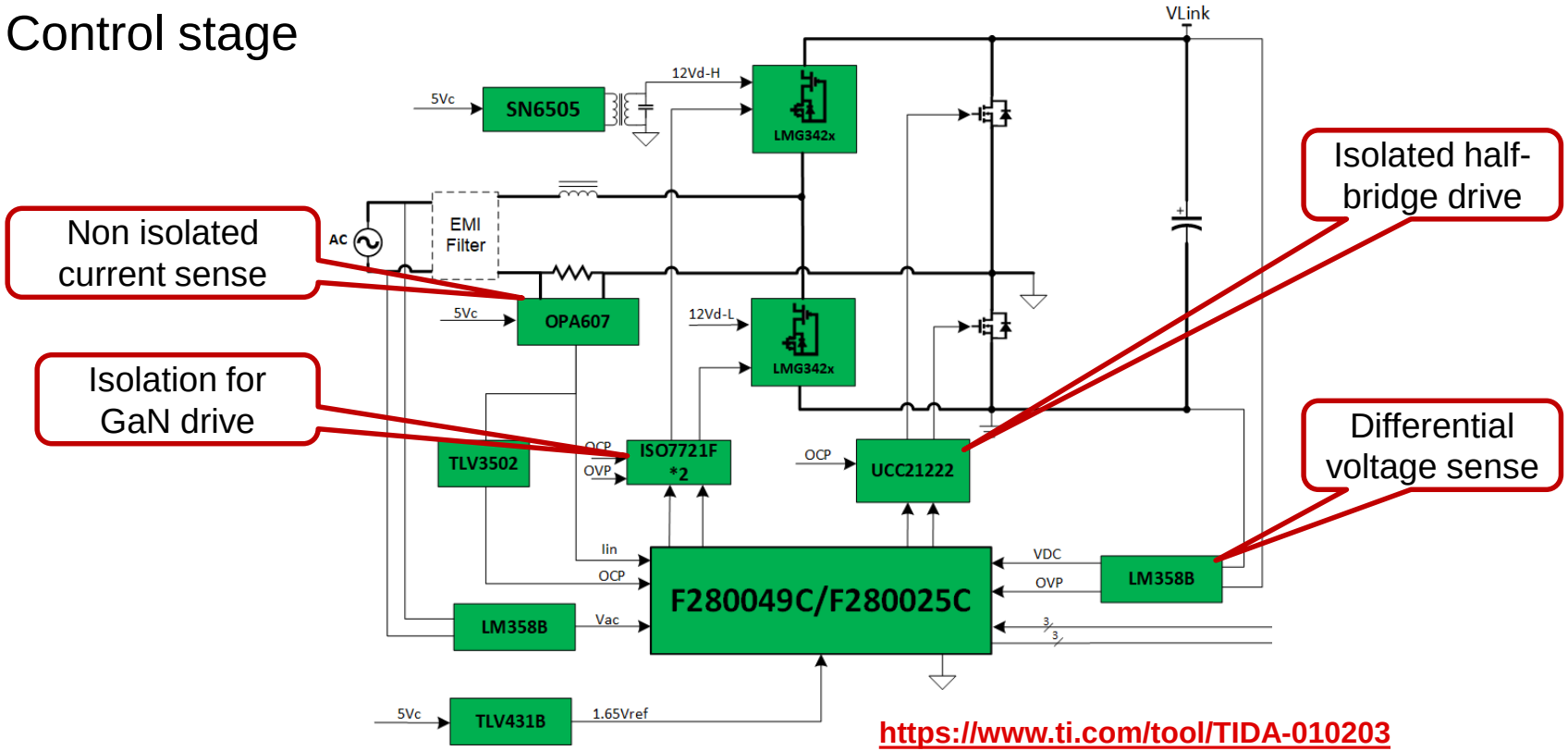
Key parameters	Key specification
Input range	200 V_{AC}-277 V_{AC}
Nominal input	230 V_{AC}
DC output voltage	400 V_{DC}
Maximum power	4,000 W
GaN HEMET (Q1/Q2)	LMG342xR030
Controller	F280049
Switching frequency	50 kHz



https://www.ti.com/tool/TIDA-010203

4-kW design of a CCM totem-pole PFC

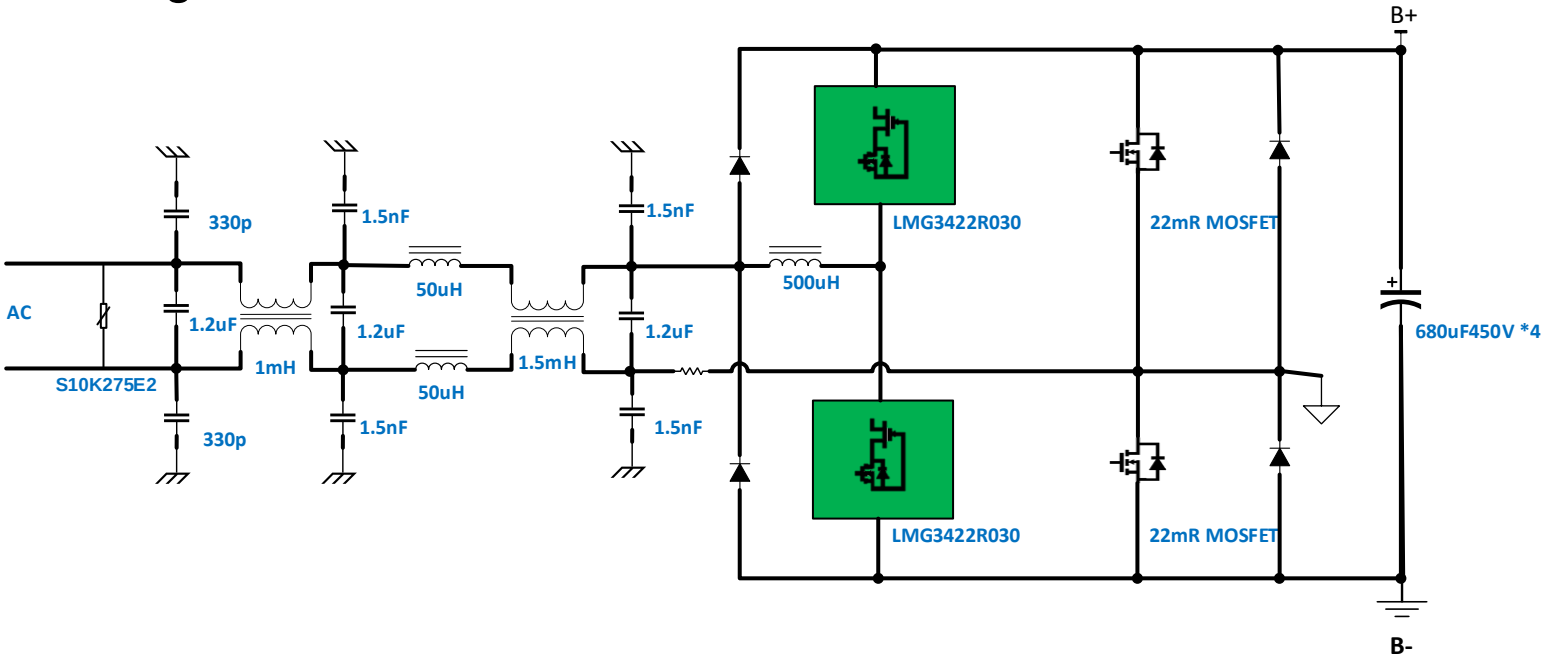
- Control stage



https://www.ti.com/tool/TIDA-010203

4-kW design of a CCM totem-pole PFC

- Power stage

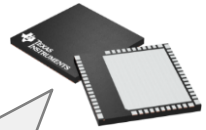


https://www.ti.com/tool/TIDA-010203

TI GaN: integrated driver and protection features

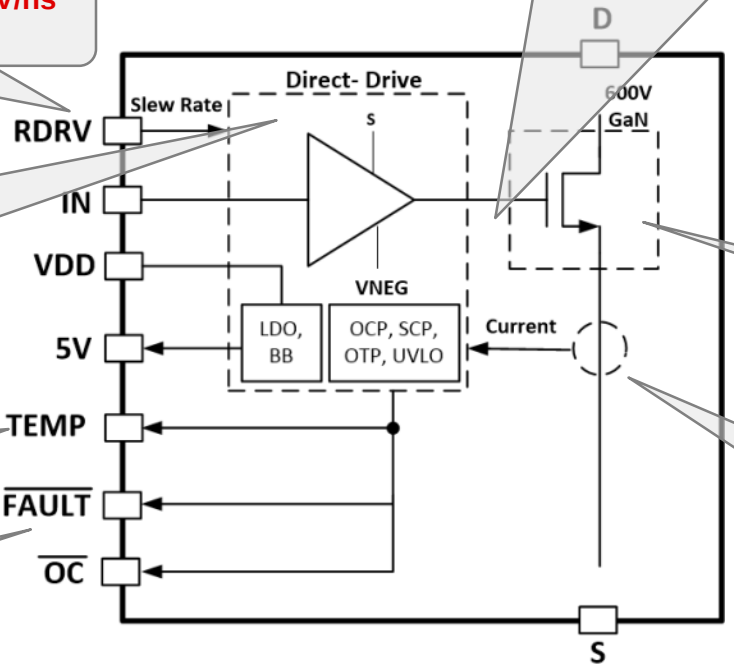
The industry's fastest switching speed:
2.2 MHz

Slew-rate capability **increased** to **150 V/ns**
Cuts losses by 50% vs. discrete GaN



New package: 12 mm by 12mm
Junction to heat-sink thermal impedance = **2.3 (°C/W)**

TI ideal diode mode cuts third-quadrant losses by as much as **66%**
https://www.ti.com/product/LMG3425R030



600-V GaN FET
50 mΩ and 30 mΩ

New GaN **temperature reporting**

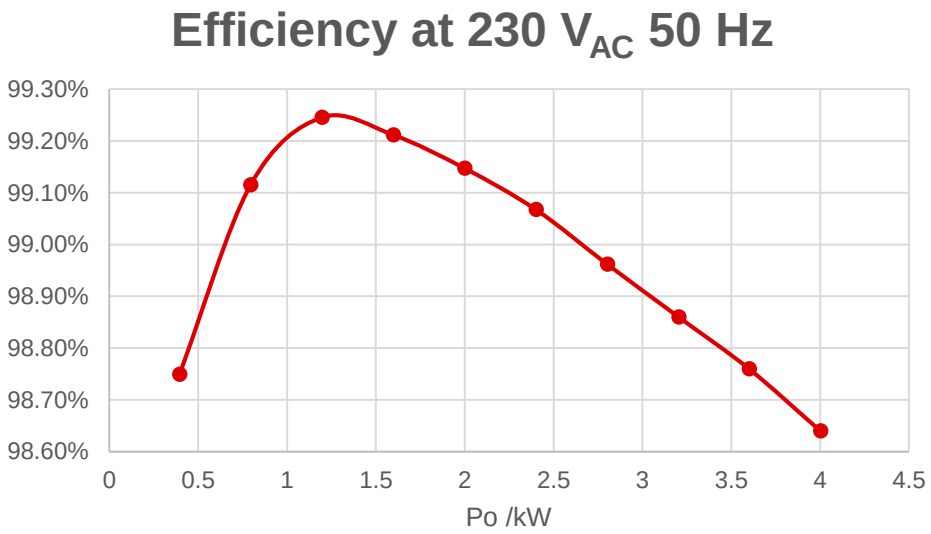
Digital fault reporting

- **Cycle-by-cycle** OCP (<100 ns)
- **Latched** short-circuit protection (<100 ns)

https://www.ti.com/product/LMG3422R030

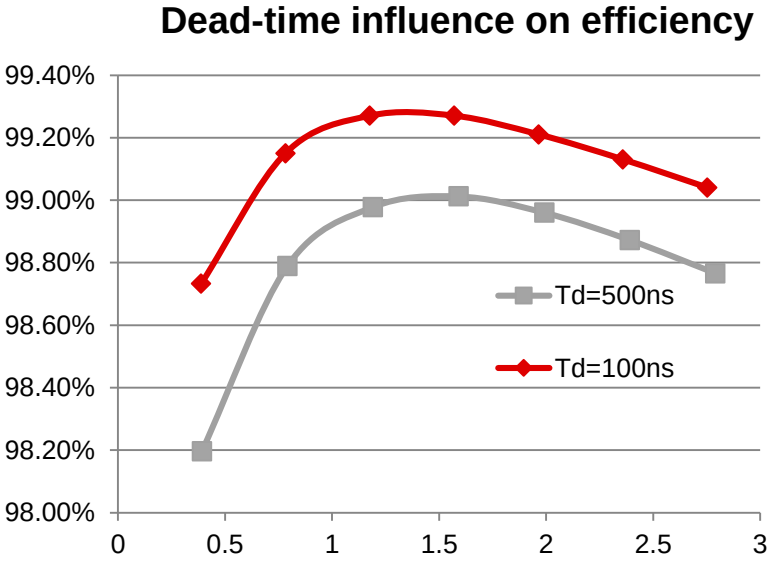
Efficiency

Efficiency test results at 230 V



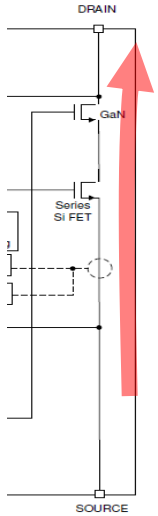
*Efficiency was measured by WT500 /YOKOGAWA

Dead-time consideration

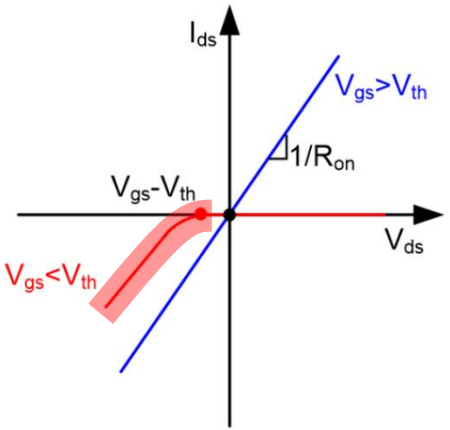


*Test condition: fs = 50 kHz

Simplified behavior of GaN in the first and third quadrants



TI GaN FET



$$V_{sd} \approx (V_{th} - V_{gs}) + I_{sd}R_{on\_reverse}$$

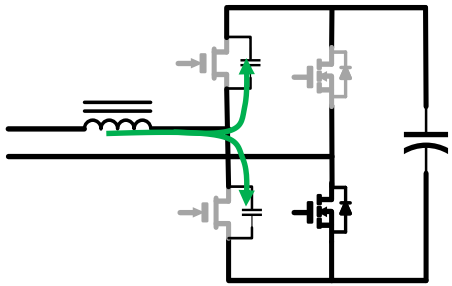
Does GaN have a body diode? - understanding the third quadrant operation of GaN

Dead-time consideration

Hard switching off

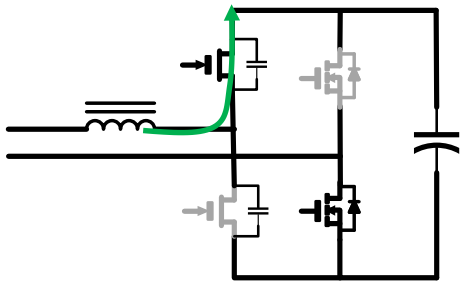
- ✓ Time related to switching current
- ✓ **Need adaptive control**

$$t_{deadtime\_optimal} = \frac{2C_{oss}V_{out}}{i_{L\_peak}}$$



Hard switching on

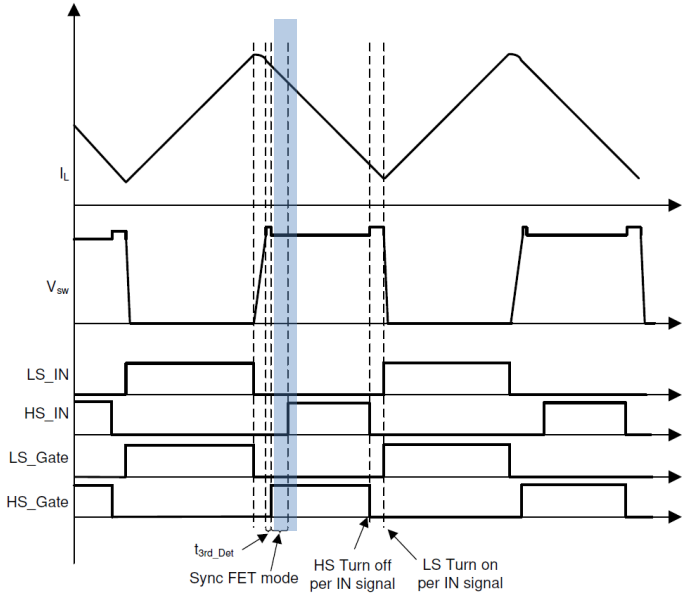
- ✓ Time related to driving strength
- ✓ Fix on the smallest

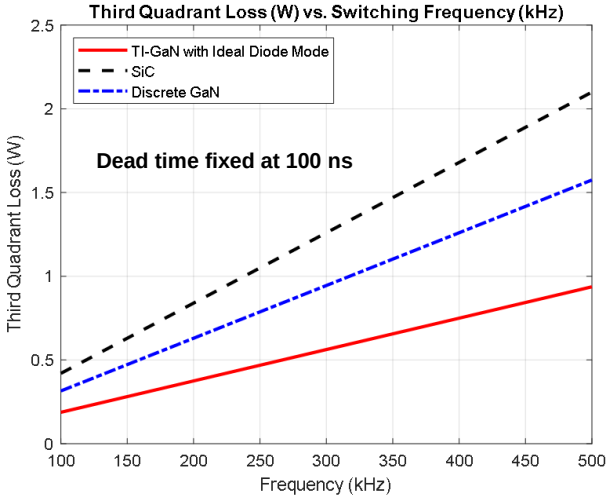


The Bidirectional High Density GaN CCM Totem Pole PFC Using C2000™ MCU reference design in the DigitalPower software development kit for C2000™ MCUs includes an “adaptive control” feature

Dead-time consideration

Ideal diode mode – LMG3425R030



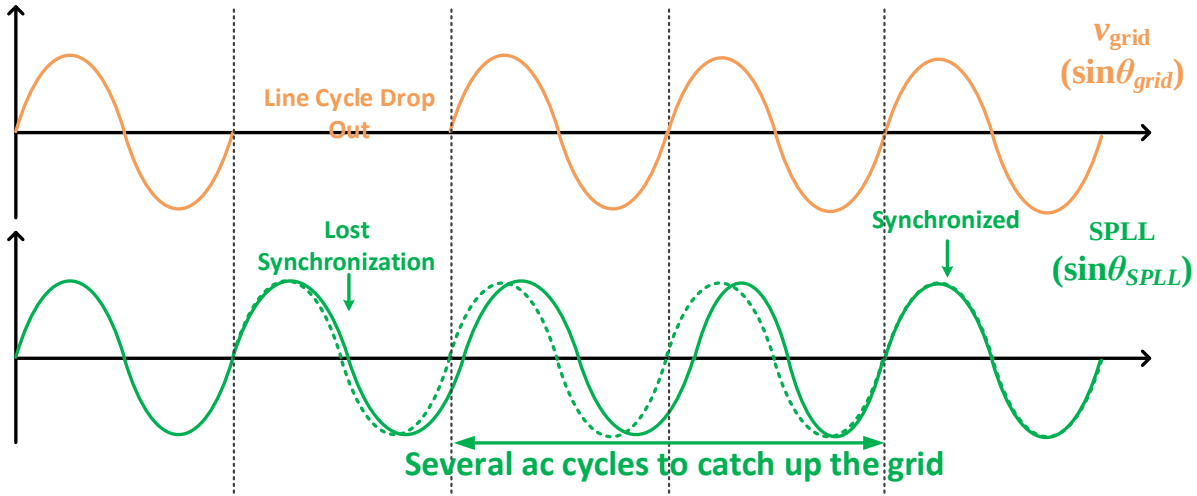


The LMG3425R030's ideal diode function could save the effort of adaptive control and improve system efficiency. This is helpful in high-frequency solutions.

AC drop

Key challenges for AC drop:

- SPLL is disturbed and requires several ac cycles to catch up with the grid.
- When ac gets back, SPLL is not synchronized with the grid phase.

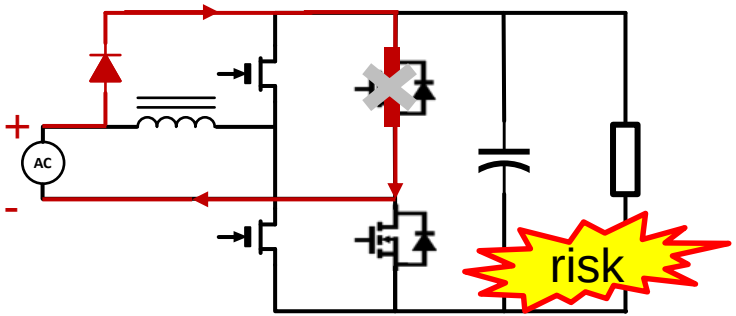


AC drop

TI’s method to solve AC drop:

- Shutdown the SR MOSFET immediate when SPLL loss control or AC voltage out of range.
- Generate an internal sine signal to keep up with grid phase.
- Well-organized state machine ensures the correct trigger of the GaN FET and grid phase.

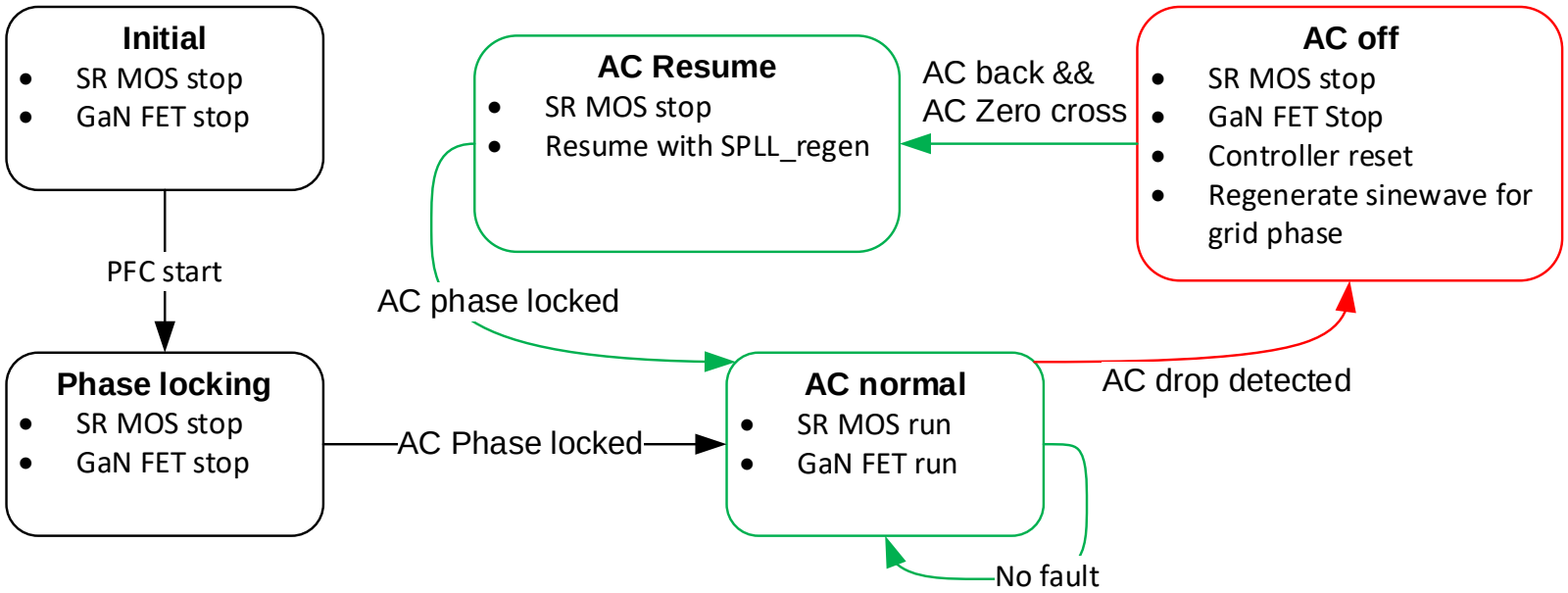
A mistrigger of the SR MOSFET leads to an input short and current spike



References:

- DigitalPower software development kit for C2000 MCUs
- Design guide of TIDM-2008, Bidirectional Interleaved CCM Totem Pole Bridgeless PFC Reference Design Using C2000 MCUs

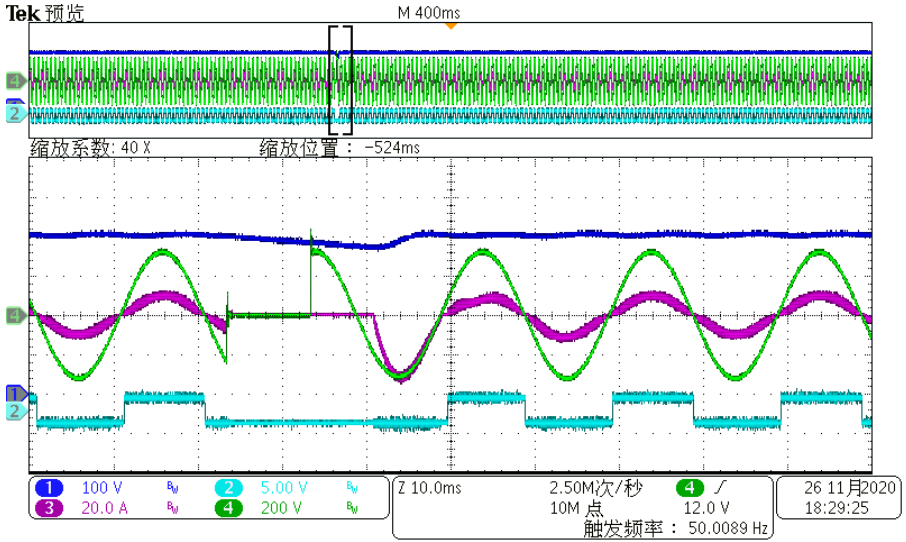
State machine for AC drop monitoring



AC drop

Waveform test result

AC drop (10ms @ 45 deg)



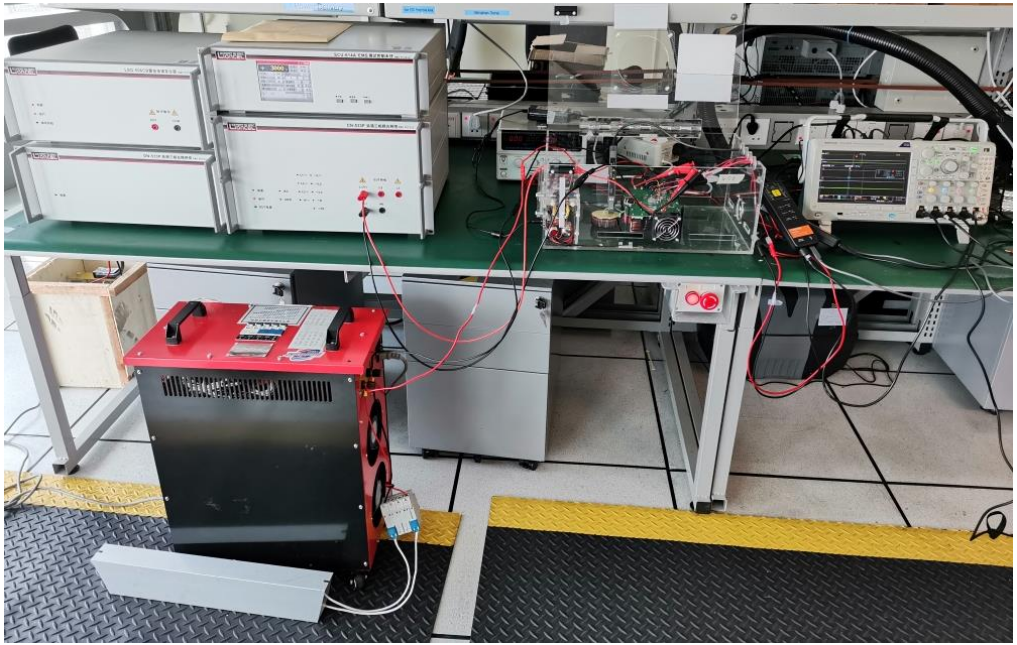
Surge test

Equipment setup:

- 5-kVA isolated transformer
- (Lioncel)
  SCU-614A
  + LSG-506CB
  + DN-533P
  + CN533P

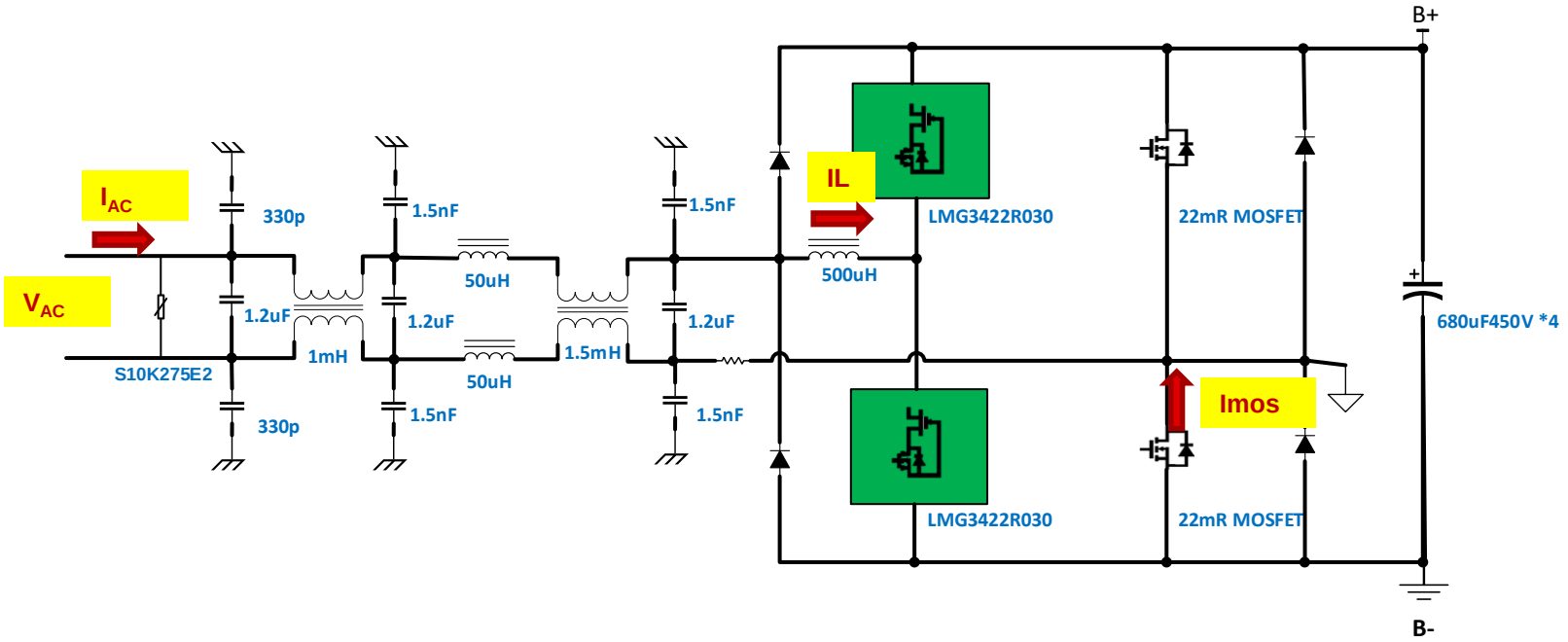
Standard:

- 1.2 μs/50 μs
- 2-Ω impedance



Surge test

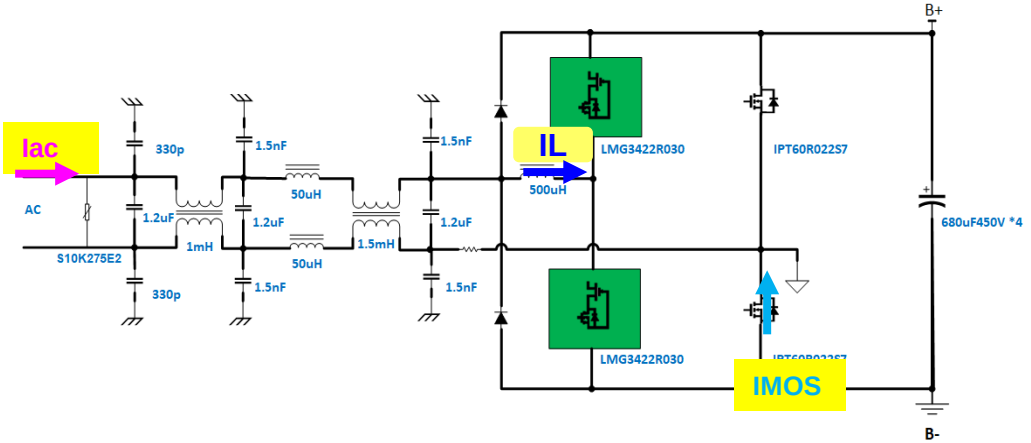
EUT parameters and probes



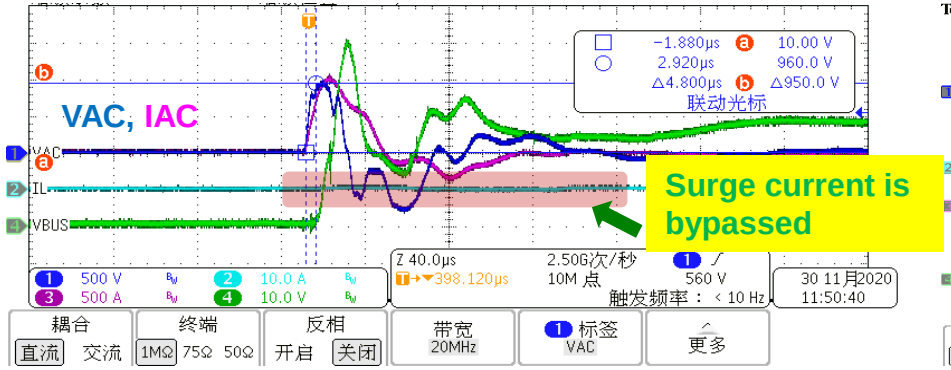
Surge test

Test without grid AC:

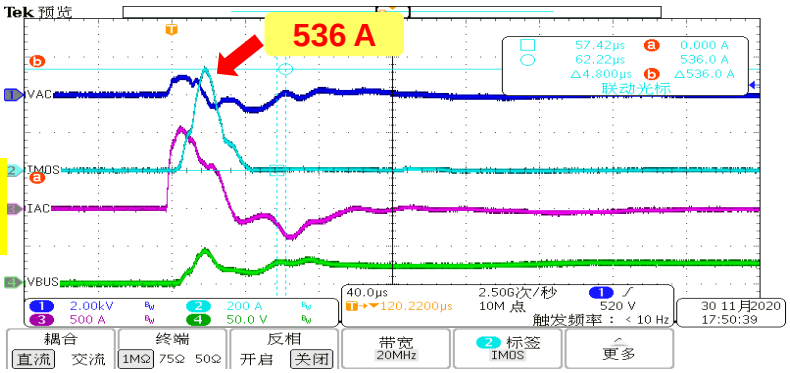
- **+3 kV**, L to N,



GaN FET is safe.



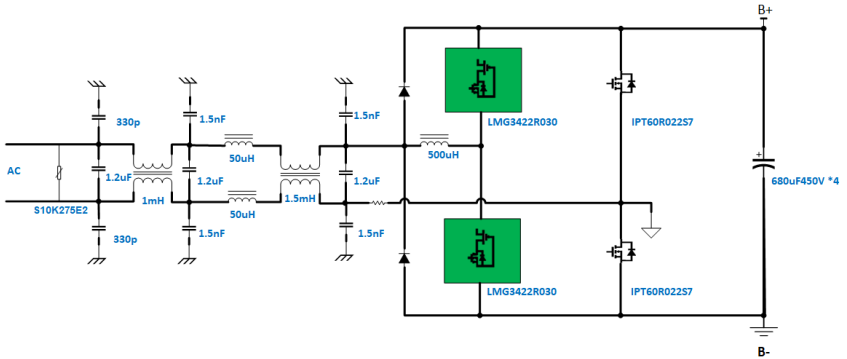
The SR MOSFET faces the risk of breaking.



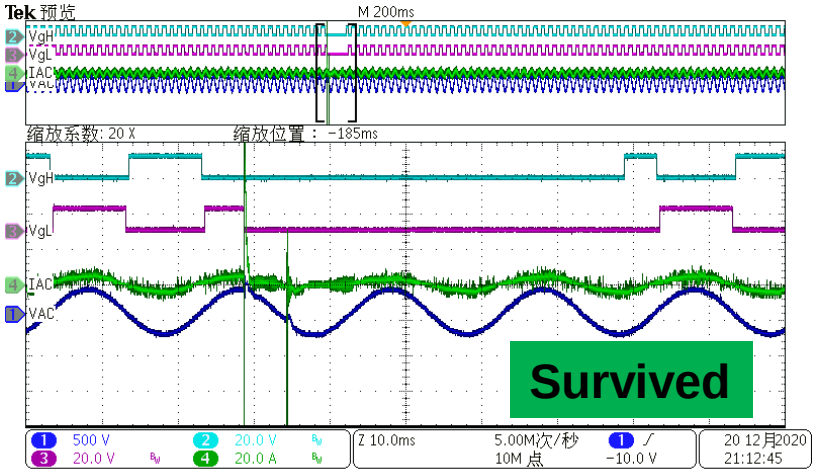
Surge test

Test with PFC operating:

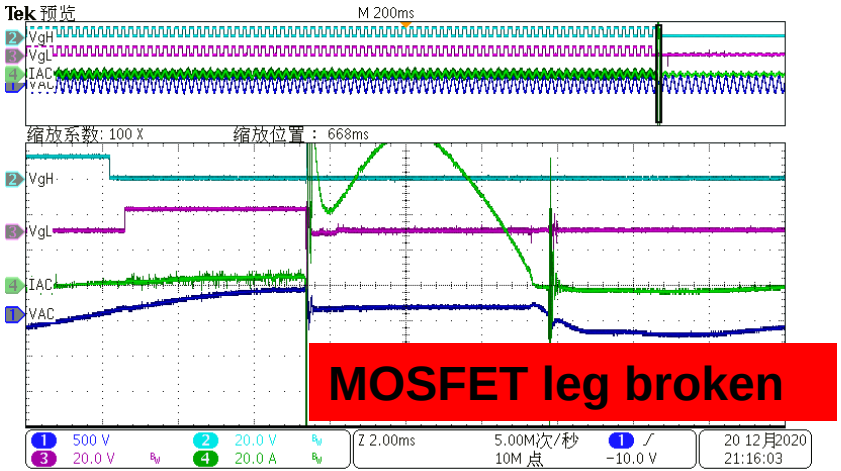
- The SR MOSFETs survived at +/-3 kV 90º.
- But SR MOSFETs broke at -4 kV 90º.



Surge test at -3 kV 90º

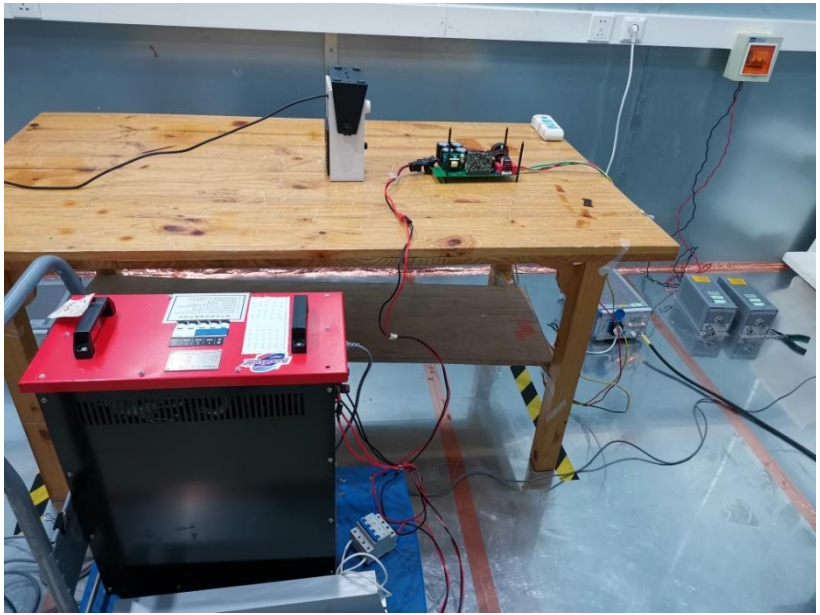


Surge test at -4 kV 90º

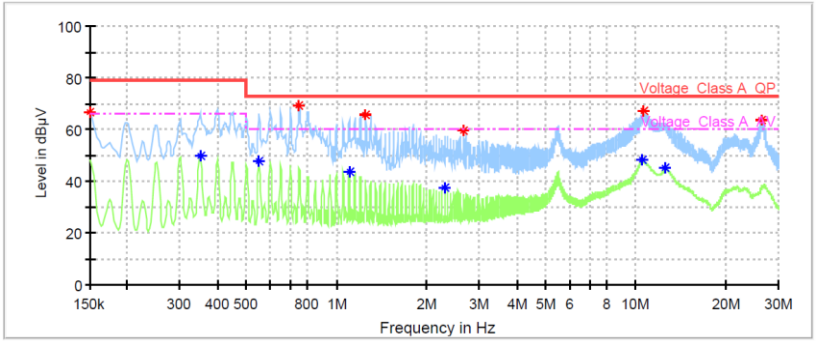


EMI CE performance

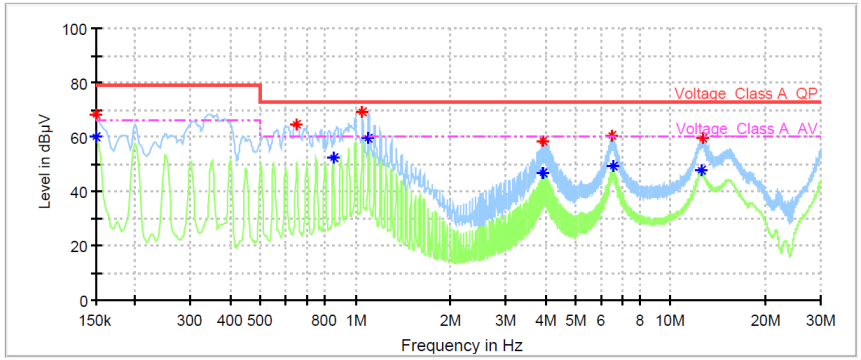
CE test setup



230 V_{AC}, load open



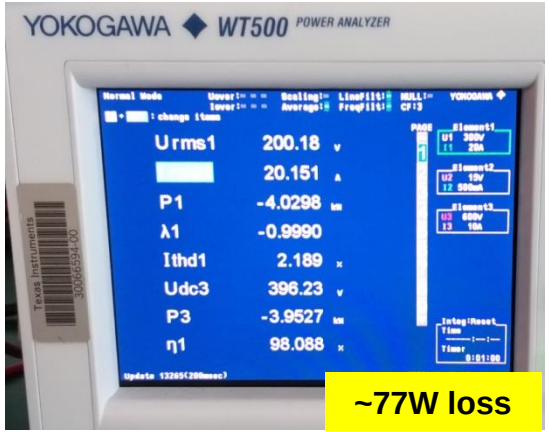
230 V_{AC}, load 40 Ω

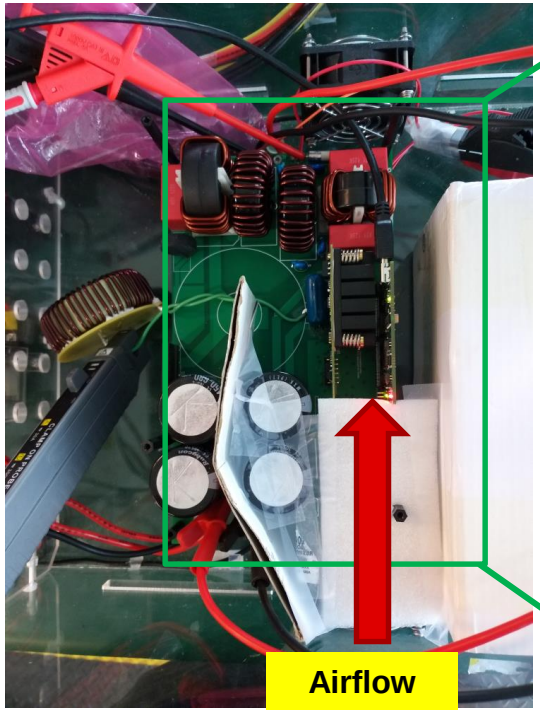


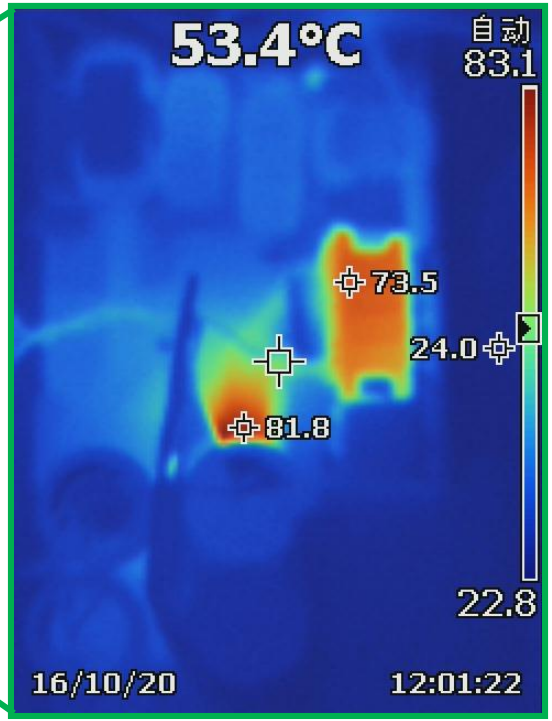
Thermal performance

Test conditions

- 200 V_{AC}, 4-kW load
- FAN: 27CFM, 24 V 2.64 W; MB60252VX-00C-A99 /SUNON
- Test after 10 minutes

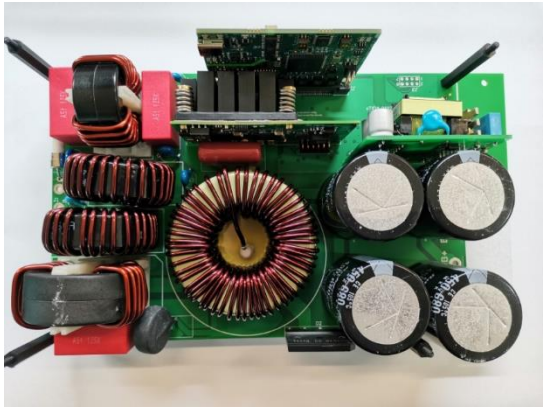






Summary

- 4-kW CCM totem-pole PFC with the LMG342xR030 could achieve 99.2% efficiency.
- AC drop and surge test are validated.
- Lighting surge is not a threat to GaN FETs, but more a risk to the SR MOSFET.
- EMI CEs can be solved in a totem-pole PFC with GaN FET.
- Thermal rise is shown, with common-air force-cooling conditions.



THANKS