Reliability of Thermally Integrated 3D Power Packaging

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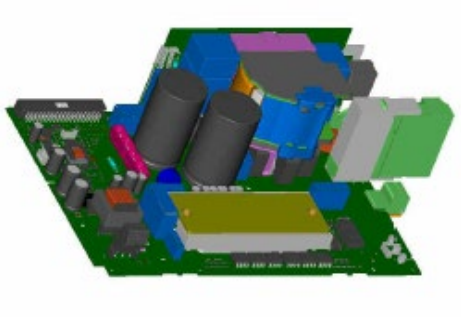
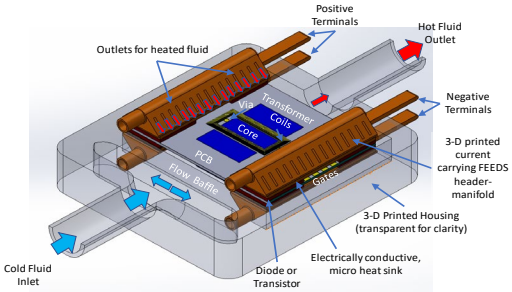
Trends in Power Electronic Packaging

- Increasingly the key product differentiator is size, weight, power efficiency and cost (SWaP-C).
- Power Electronics are being used at
  - Increased load levels
  - With denser packaging schemes
  - In harsher environments
- Drive towards a fully integrated 3D power electronics module.



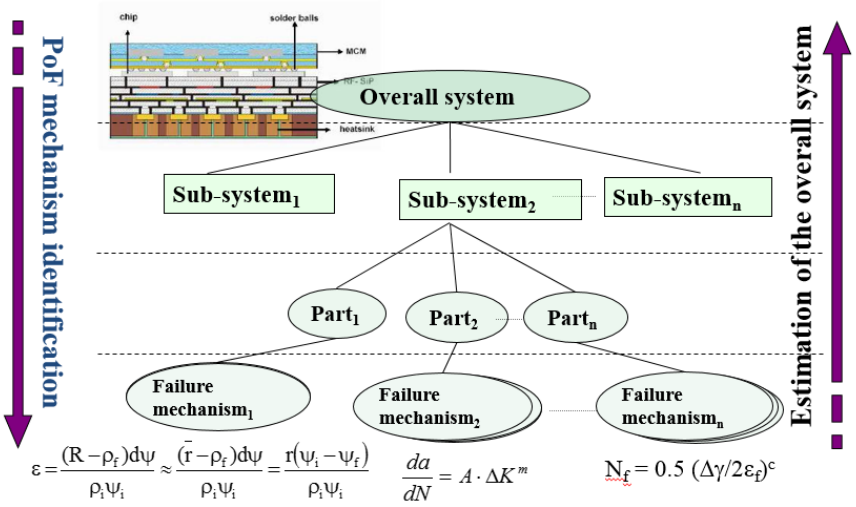


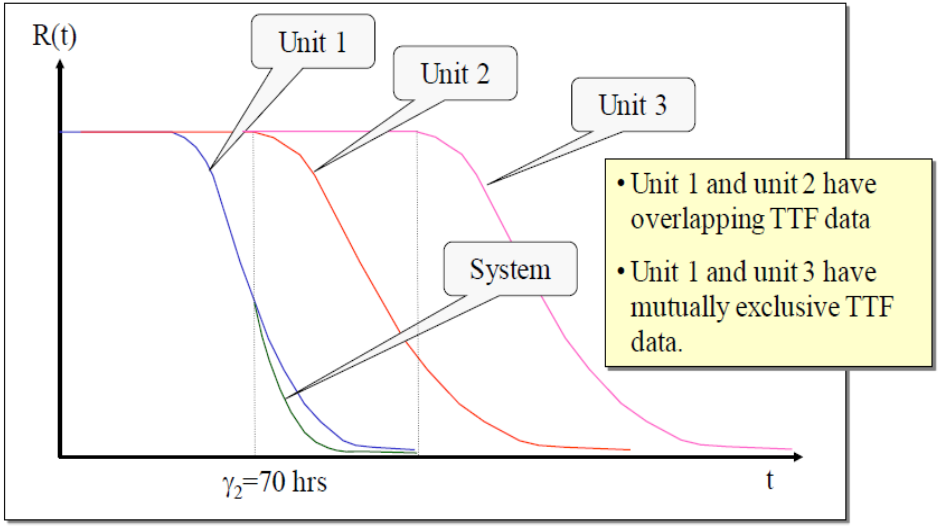
- Physics-of-failure concepts enable reliable design of future systems.

Probabilistic PoF Reliability Assessment

A PPoF approach can be used to determine reliability. This includes the following:

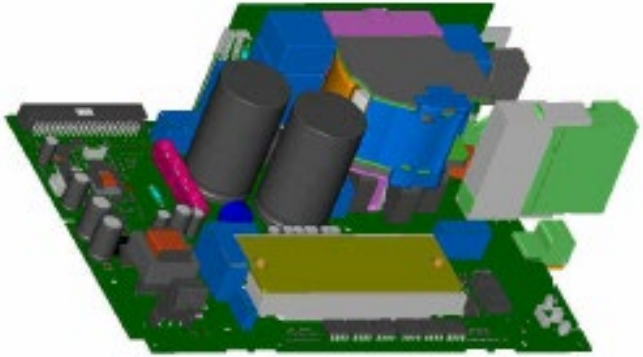
- Estimating MTTF and FFOP for each element failing by each failure mechanism
- Using a fault tree analysis to see which components are in series
- Using probabilistic mathematical approaches to combine the independent distributions for identical or non-identical parts failing due to identical or non-identical failure mechanisms

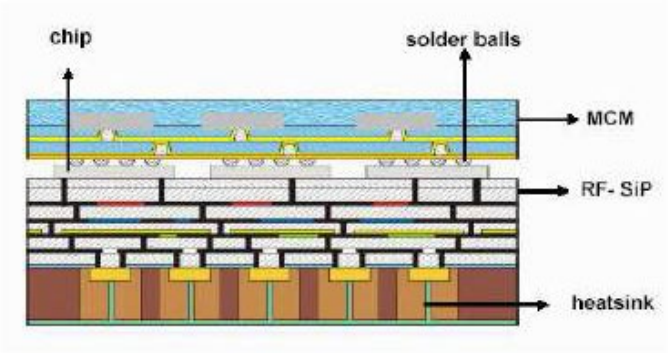




3D Integrated Packaging

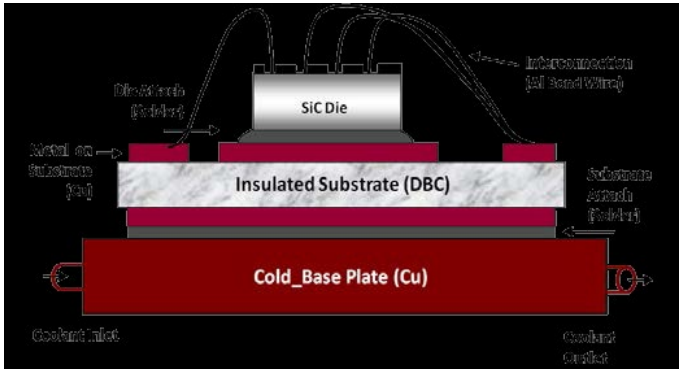
- Moving from 2D packaging of discrete components on a PWB to 2.5D – 3D stacked modules
- Examples are:
  - Power Supply on Chip (PSOC)
  - Power Supply in Package (PSIP)
- These packages contain embedded actives, embedded passives, embedded thermal management, and attachments.
- Additive manufacturing may be used for true 3D structures





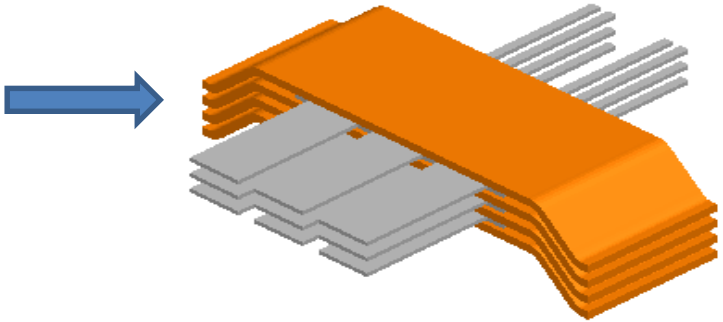
From Wirebond → Sintered Interconnect

"Traditional" Wirebond



- Chips interconnected with 125-375 mm diameter wire.
- Dice soldered to a thick metalized ceramic substrate (e.g. DBA, DBC) which is soldered to a heat spreader.
- Most heat (>85%) dissipated from the back of the die through the substrate to the heat spreader.

Sintered Interconnect

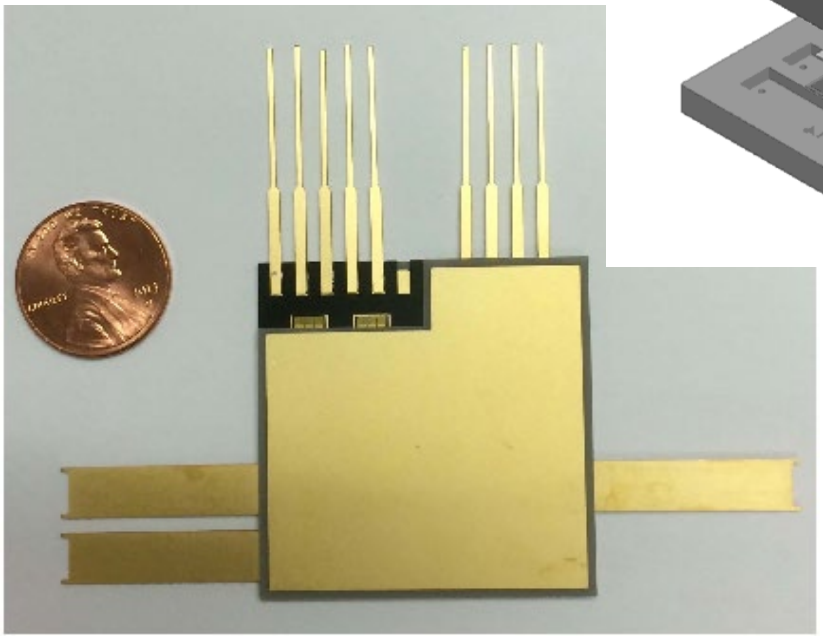


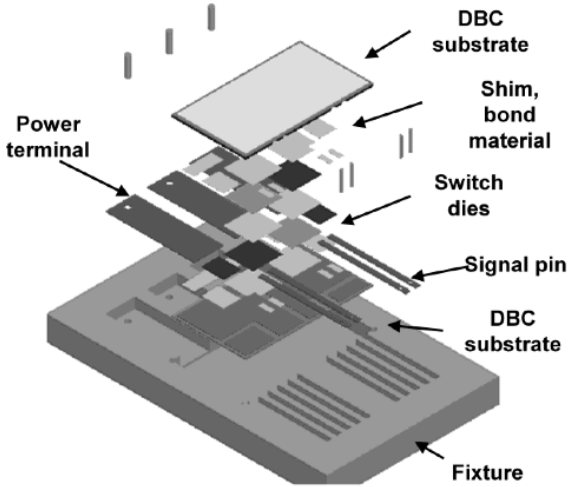
- Chip bonded top and bottom with a permanent attach.
- Eliminates wirebond failures
- Supports double sided cooling
- Need high temperature attach robust against delamination and cracking

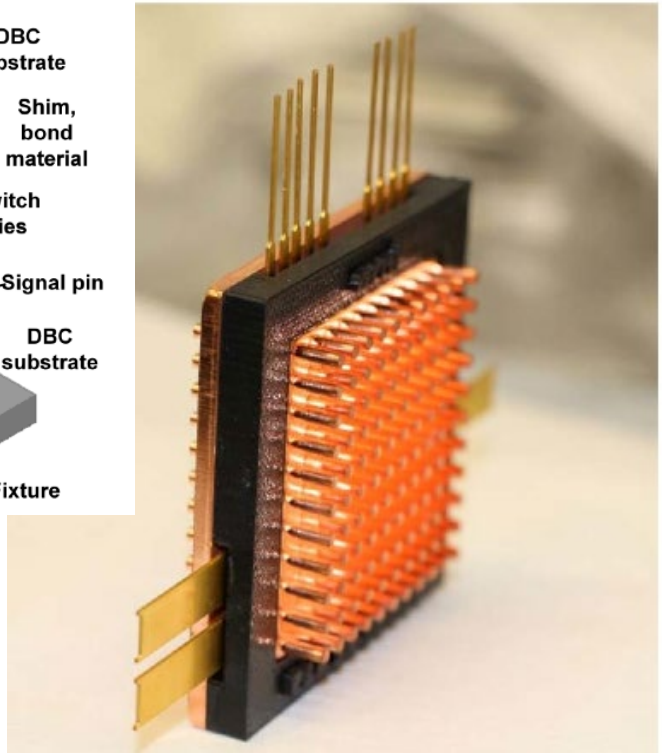
Z. Liang, "WBG Inverter Packaging," 2013 U.S. DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review

Sandwich Construction

Zhenxian Liang; Puqi Ning; Wang, F.; Marlino, L., "A Phase-Leg Power Module Packaged With Optimized Planar Interconnections and Integrated Double-Sided Cooling," *Emerging and Selected Topics in Power Electronics, IEEE Journal of* , vol.2, no.3, pp.443,450, Sept. 2014







Zhenxian Liang; Wang, F.; Tolbert, L., "Development of packaging technologies for advanced SiC power modules," *Wide Bandgap Power Devices and Applications (WiPDA), 2014 IEEE Workshop on* , vol., no., pp.42,47, 13-15 Oct. 2014

Die Attach

- High lead solder (e.g. Pb2Sn2.5Ag,PbSn5) has been a standard die attach.
- With the advent of RoHS, which required the removal of lead from most solder since 2006, the industry has moved to alternative attach materials that provide:
  - T_m > 250°C
  - Excellent wettability
  - Toughness and reliability
  - Cost competitiveness
- These alternatives are grouped in three main categories
  - Brazes
  - Sintered Metal Powders (Copper, Silver)
  - Transient Liquid Phase Attachments

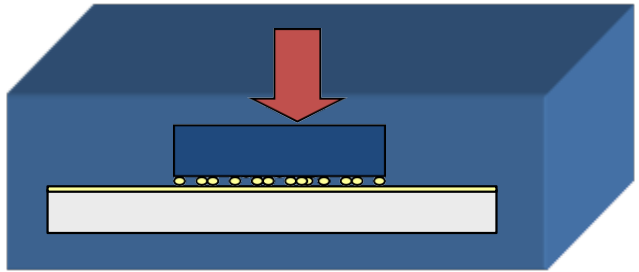
Sintered Interconnect

Reflow Attachments

Solder	T_m	Issues
Bi-Ag Alloys	262˚C	- Small elongation, brittle - Limited wetting - Low thermal conductivity
Au20Sn	280˚C	- High process temp - High cost
Au12Ge	361˚C	
Au3.2Si	363˚C	
Zn6Al	381˚C	- Complicated processing - Limited wetting - High process temp
Zn5.8Ge	390˚C	

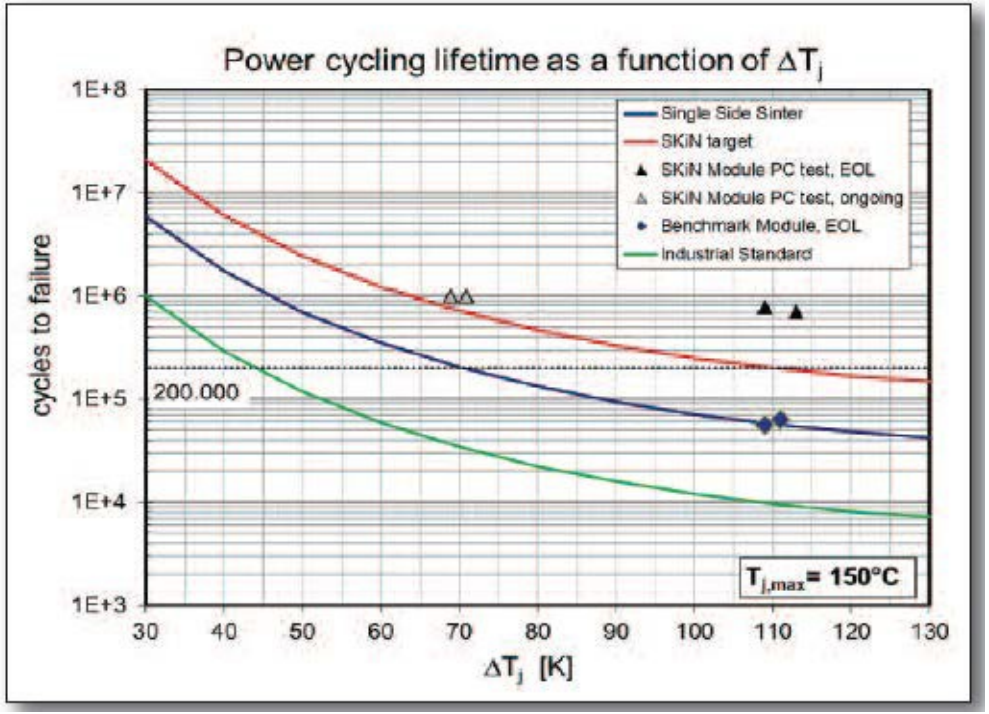
Sintered Silver

Combine moderate range processing temperatures (225°C - 275°C) with modest pressure to convert a silver powder paste into a porous solid joint. Order of magnitude better power cycling reliability than soldering.



Sintered Silver Attachment

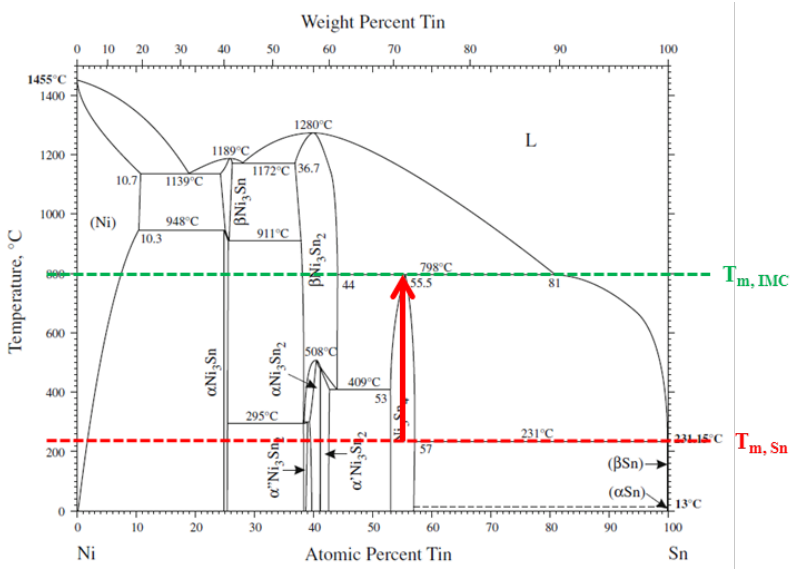
- Advantages
  - Better thermal/electrical performance than solder 2.5 – 12.5 μΩ-cm; 80-290 W/mK
  - Drop-in replacement for solder paste
  - Shear strength to 100 MPa; Modulus < 10 GPa
- Disadvantages – Cost
  - No self-alignment
  - Best on Ag plated surfaces, Au requires higher temperature and Cu oxidizes
  - Potential for silver migration
- Silver Microflake Paste
  - Requires high pressure levels (30-40 MPa)
  - Distributed micropores lower modulus and stress
  - Can hybridize with nanopowders
- Silver Nanopowder Paste
  - Can be done pressureless in reducing atmosphere
  - Potential for >15X improvement in heat transfer
  - Greater reliability than solder.
  - Prone to vertical cracking if not properly dried



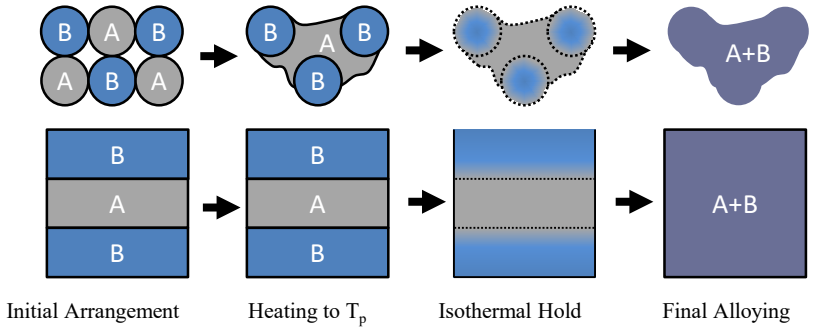
Beckedahl, P., "Power Electronics Packaging Revolution Without Bond Wires, Solder, and Thermal Paste," Power Electronics Europe, No. 5, July/August 2011

TLPS Attach Technology

- TLPS (Transient Liquid Phase Sintering) is a liquid-assisted sintering process during which a low melting temperature constituent, *A*, melts, surrounds, and diffuses in a high melting temperature constituent *B*.
- Intermetallics with high melting temperatures are formed by liquid-solid diffusion
- TLPS systems can be processed at low temperatures but are capable of operating at the high melting temperatures of the intermetallic compounds.

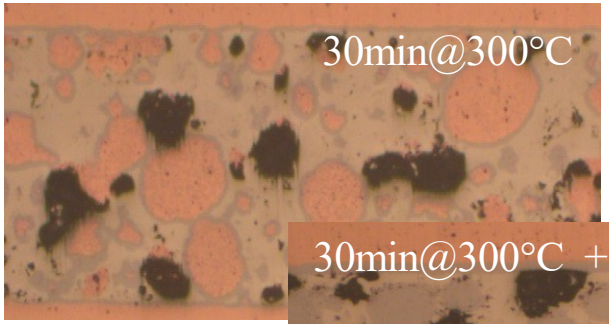


- TLPS joints with flux can be formed from low cost material systems (Cu-Sn, Ni-Sn) without pressure or vacuum. Common metallizations can be joined.

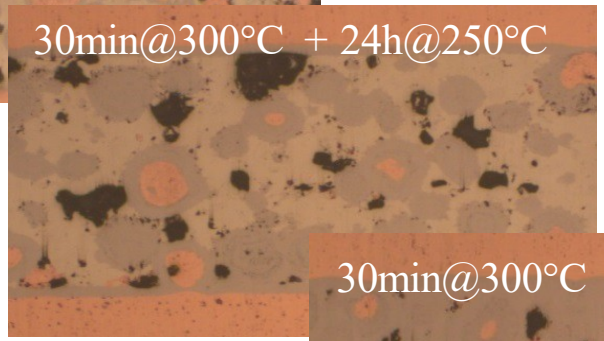


Recent Research on TLPS

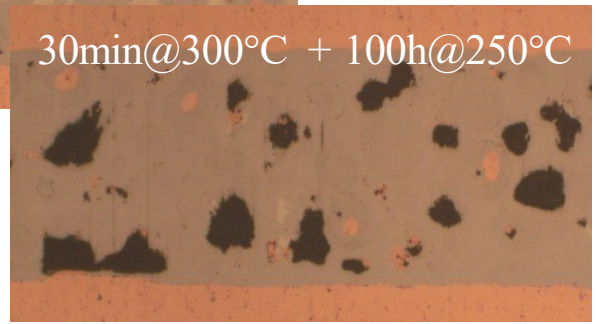
Characterized microstructural evolution in joints during use from Cu → Cu_6Sn_5 → Cu_3Sn



Cu_6Sn_5 matrix

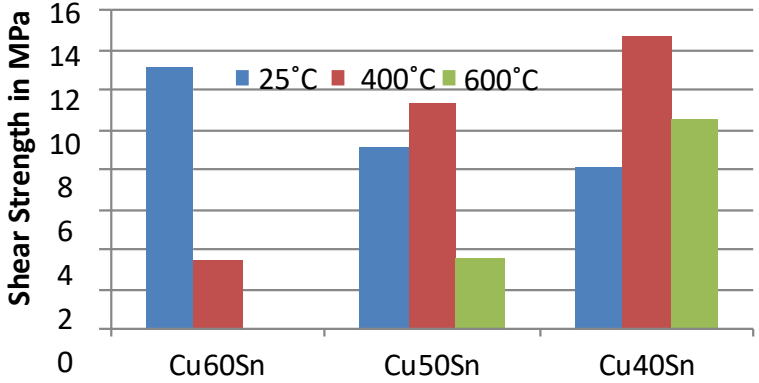


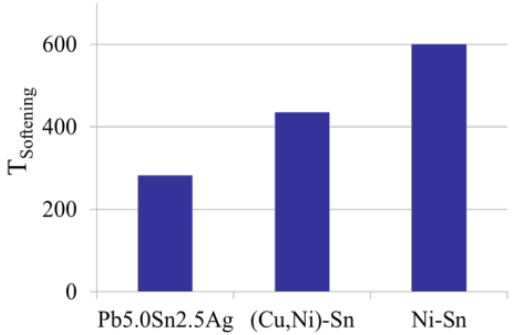
Cu_3Sn + Cu_6Sn_5 matrix



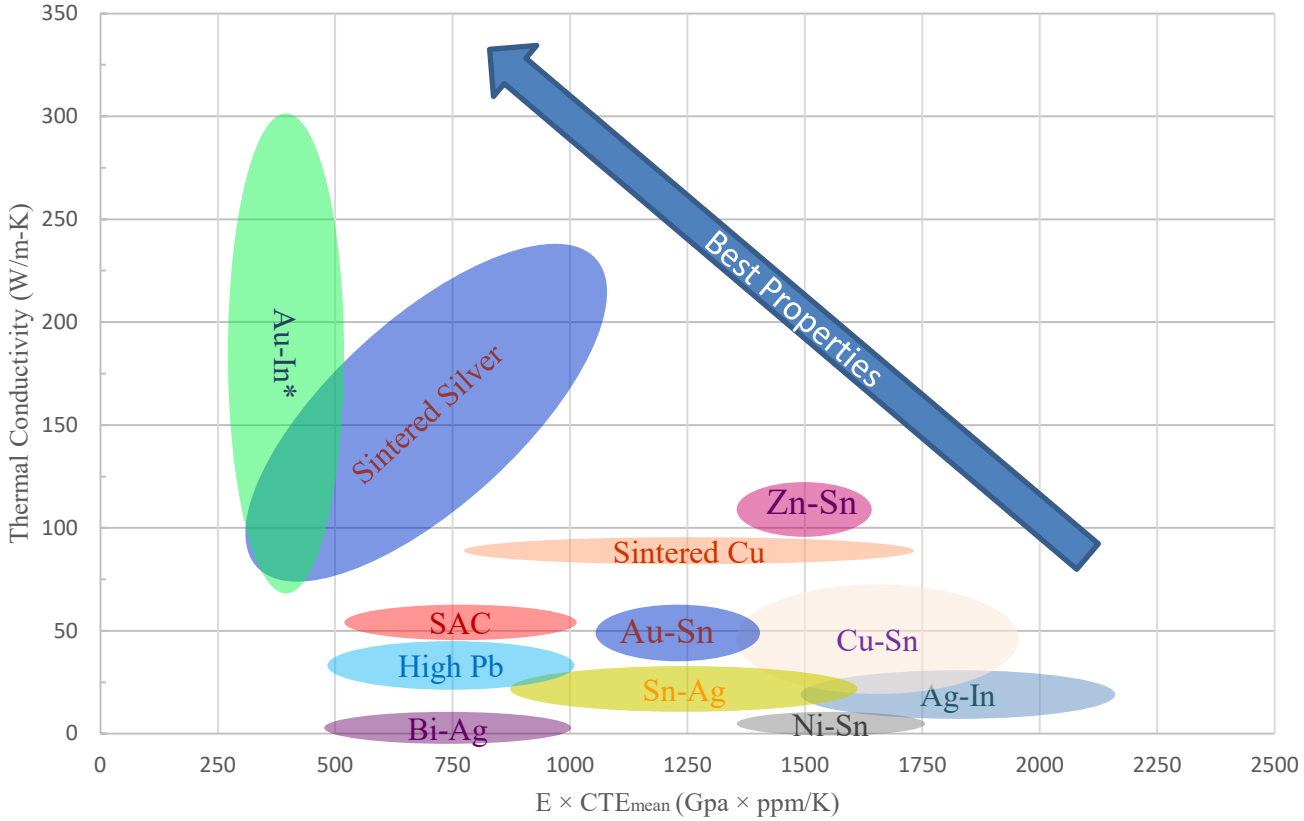
Cu_6Sn_5 matrix

Showed that TLPS joints retain strength > 10 MPa to temperatures> 600°C



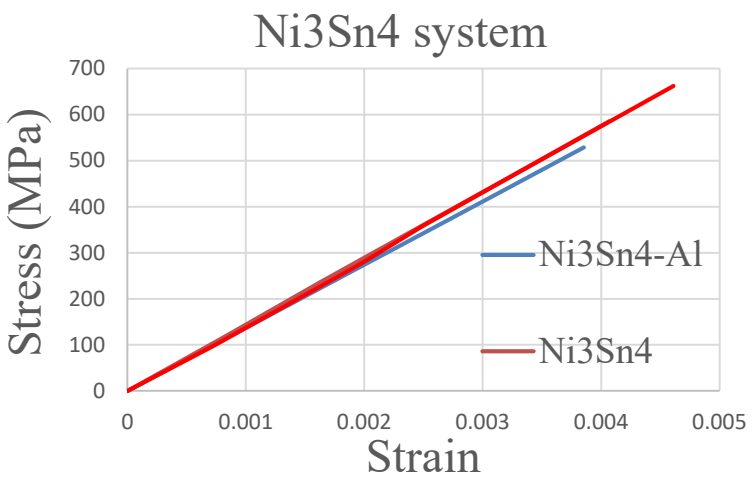


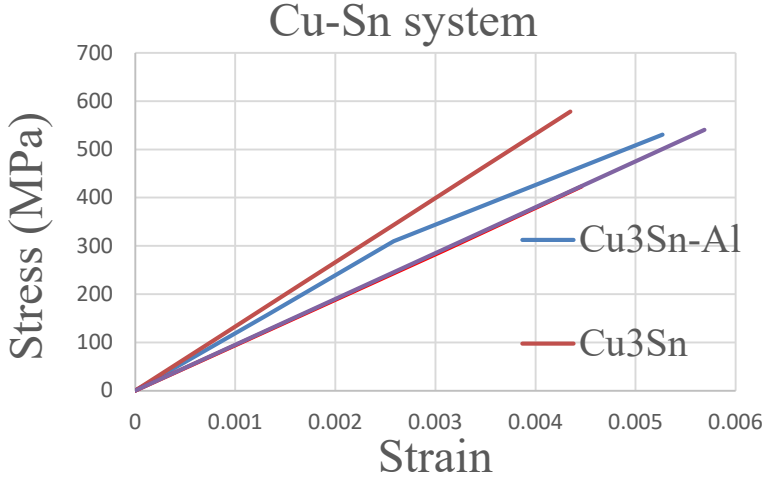
Thermal Conductivity vs Mechanical Properties



*Thermal conductivity of Au-In system was not found in the literature, conductivity of In and Au were considered as limits

Effect of Ternary Metal Additions

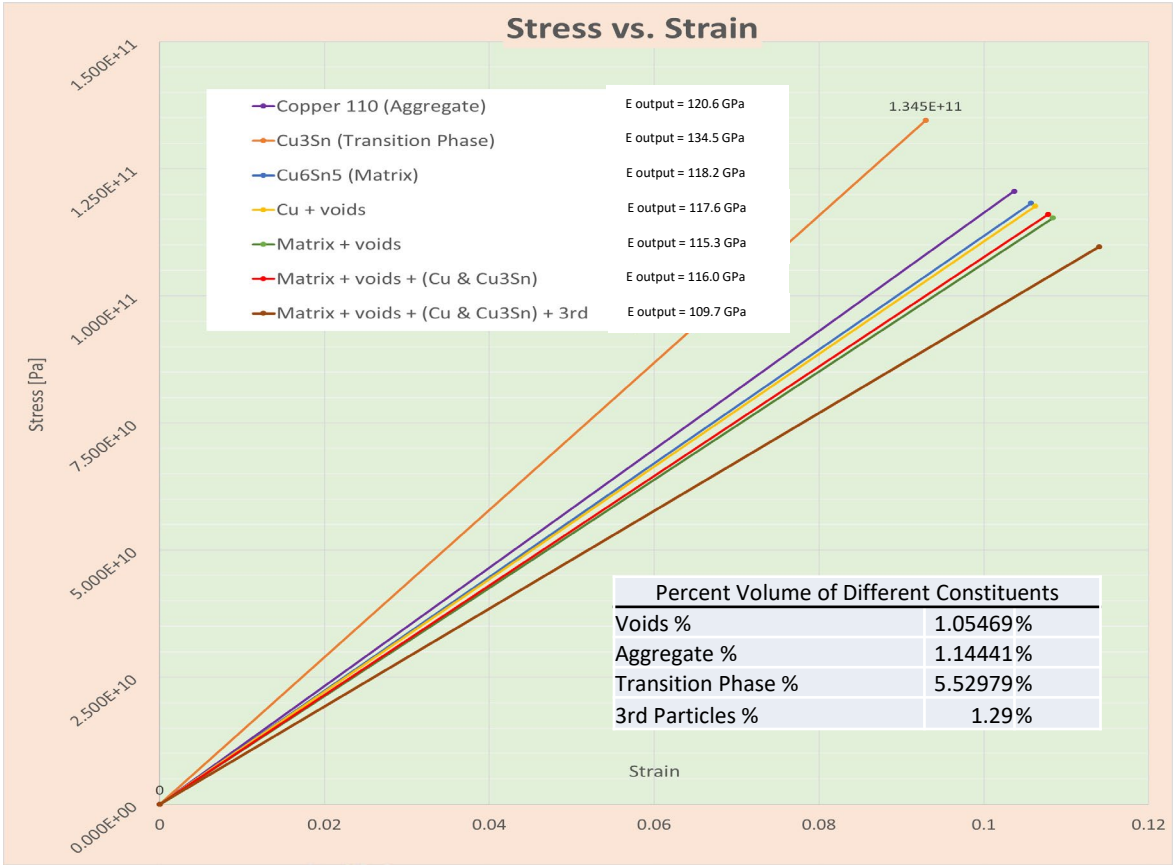




IMC Matrix	Tertiary Particle (rad.)	Percentage Vol%	Force (N)	Max Stress (MPa)	Homogeneous Sample Max Stress (MPa)
Ni_3Sn_4	Al (10μm)	14.5	40	528	586
Ni_3Sn_4	Al (20μm)	15.6	40	507	586
Cu_6Sn_5	Al (10μm)	14.5	40	422	540
Cu_3Sn	Al (10μm)	14.5	40	530	578

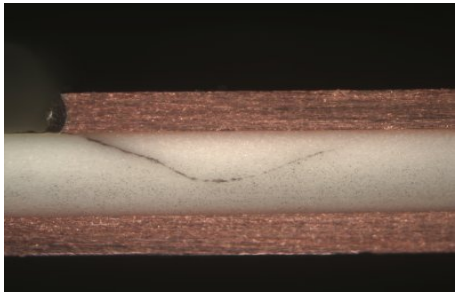
Effect of Soft Particles

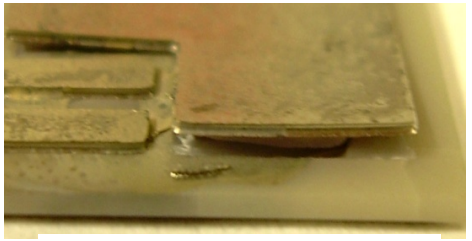
- The respective elastic modulus for each joint is shown in the graph.
- The graph depicts a trend rather than the true strain since the test was limited to the elastic region.
- It reveals that a small percentage of Si rubber particles (3rd Particles) can decrease the slope of the line.

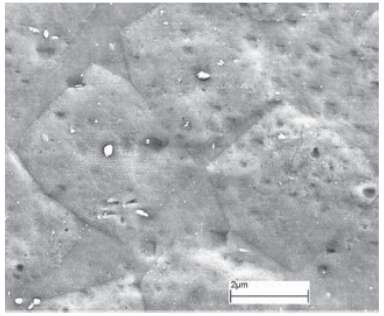


Ceramic Substrate Failure Mechanisms

- Direct Bond Copper on Al_2O_3, AlN
  - Failure mode: Debonding of metallization followed by cracking in the ceramic
  - Cause: Local CTE mismatch between metallization and ceramic in temp cycling
  - DBC cracking can be mitigated by:
    - Dimpling or Copper Metallization Thinning
    - Increased Fracture Toughness (Additions)
    - Bonding of Substrate to Copper Heat Sink
- Direct Bond Aluminum
  - Cu: $\sigma_y \approx 70$ MPa → High stresses in ceramic and Cu-ceramic interface → short time-to-failure under system temperature excursions
  - Al: $\sigma_y \approx 20$ MPa → Reduced susceptibility for ceramic fracture, but: extensive deformation of metallization → Hillock formation

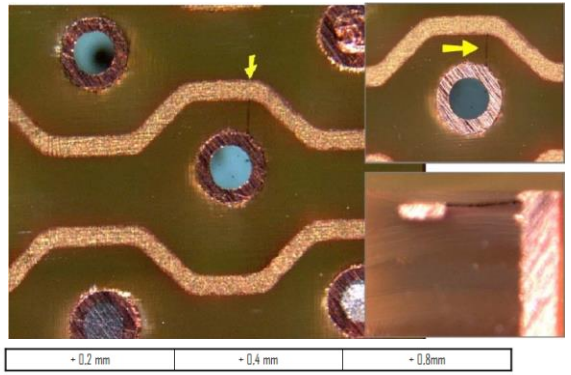


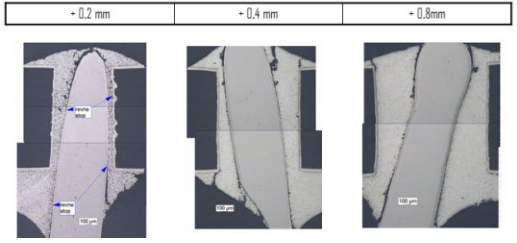


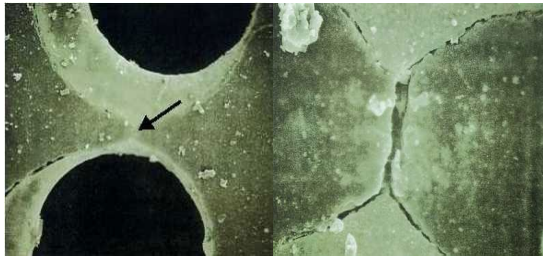


Polymer Substrate Failure Mechanisms

- Conductive Filament Formation
  - Creation of thin metal conducting filaments between traces and vias on the board at voltages > 300V when subjected to thermal cycling and humidity
- Solder Fatigue
  - PTH and SMT components
- PTH/Via Fatigue
  - Fatigue cracking of the walls of a plated through hole or via as a result of thermal cycling. Crack can propagate around the circumference of the plated through hole (PTH) or Via when cyclic stresses exceed the fatigue strength of the copper wall
- Corrosion
- Creep Corrosion/Dendrite Growth
  - Electrochemical metal degradation

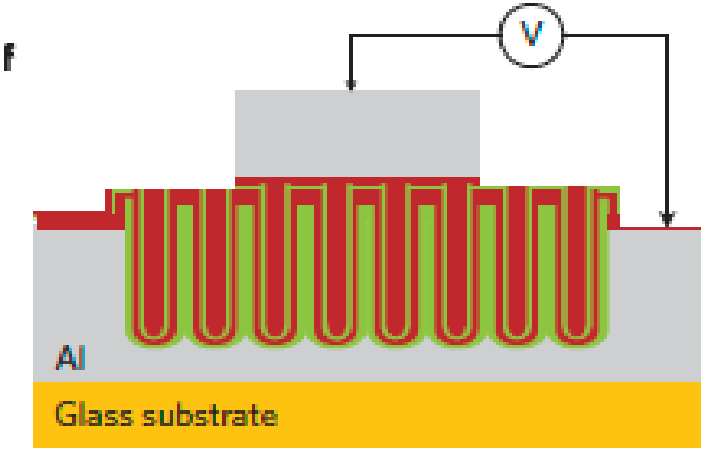






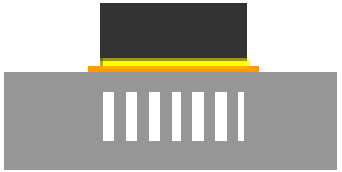
Reliability of Embedded Capacitors

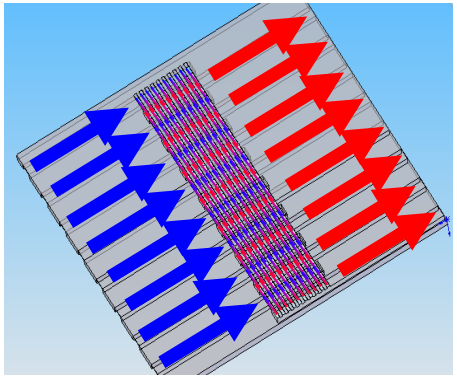
- Methods for integrating capacitors into 3D structures
  - Embedded capacitor films
    - Pin holes/partial discharge
    - Metal migration
    - Dielectric breakdown
  - Embedded capacitor devices
    - Cracking and delamination – thermomechanical stress
    - Swelling and delamination – hygrothermal stress

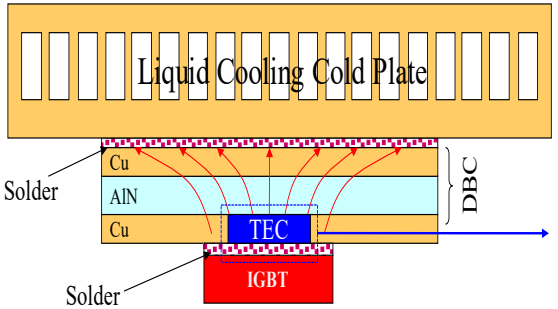


Increasing Power Density → Integrated Cooling

- Increasing power densities in electronics require more effective cooling solutions, particularly for power electronics modules.
  - Dissipation levels on the order of several hundred watts/cm^2 are not unusual.
- Controlling temperature is critical to device performance and reliability.
  - Performance
    - Slower switching, Higher leakage current, Higher forward voltage
    - More Losses (Thermal run-away)
  - Reliability
    - Many failure mechanisms occur more quickly at higher temperatures.
    - Others occur more quickly with wide temperature swings.

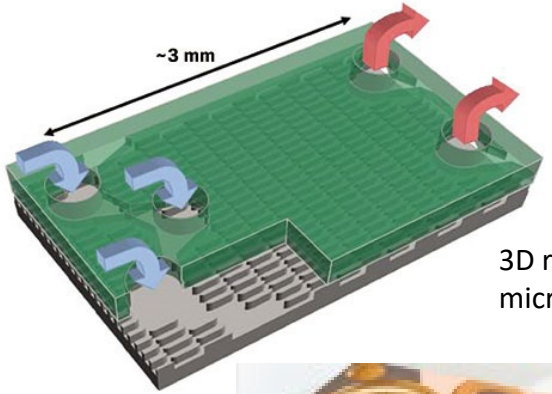






Embedded Manifold Microchannel Coolers

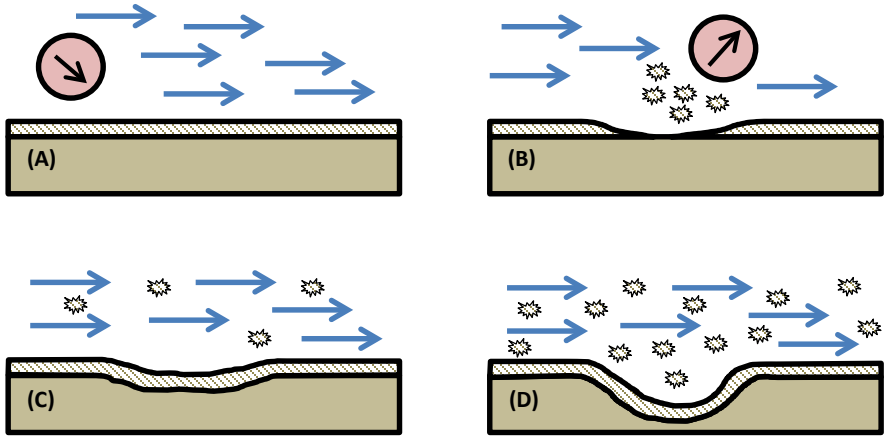
- Manifold-Microchannel coolers can be embedded directly into the substrate or chip to provide localized heat removal at high volumetric rates from the backside of active ICs and power electronic devices.
- These coolers take many forms. For example single vs. two-phase, silicon vs. ceramic substrates and
  different alloys, filter size, working fluid, fluid velocity, and temperature.
- They are used to overcome thermal limits that can cause power electronic devices to operate at voltages and currents below their inherent electrical limits.
- No “one-size-fits-all” reliability solution.



3D rendering of Si microchannel cooler

Rogers Corp. curamik ®Coolers.

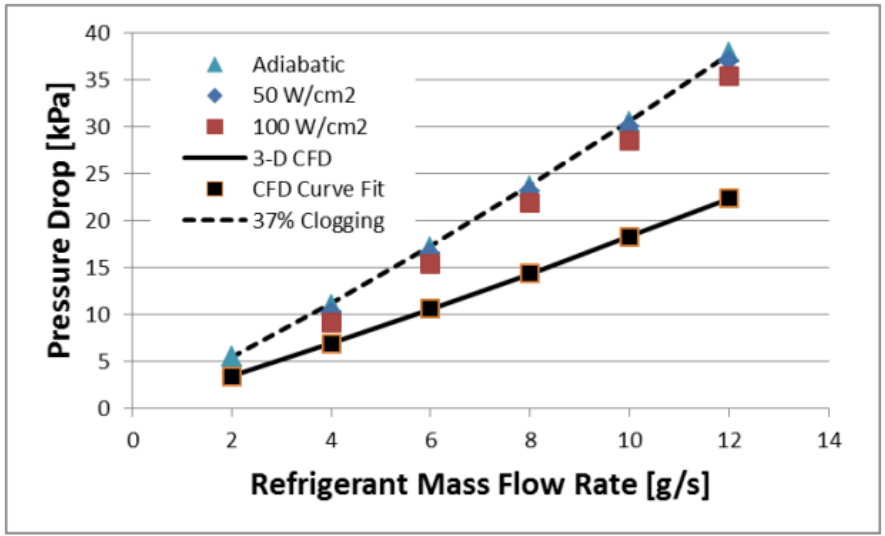
Erosion-Corrosion Concerns



- Can result in permanent modification to microfluidic geometries altering heat exchanger efficiency.
- Fluid is within close proximity to the active electronics - may result in catastrophic damage especially in jet-impingement scenarios.
- Particle impingements may generate more particles accelerating degradation.
- Increasing filtering levels increases required pumping power –not always an option.

High accuracy erosion predictions must be made to ensure reliable operation throughout the lifetime of the cooler

Clogging/Fouling Concerns



Presence of clogging indicates an increase in pressure drop compared to the CFD-based results

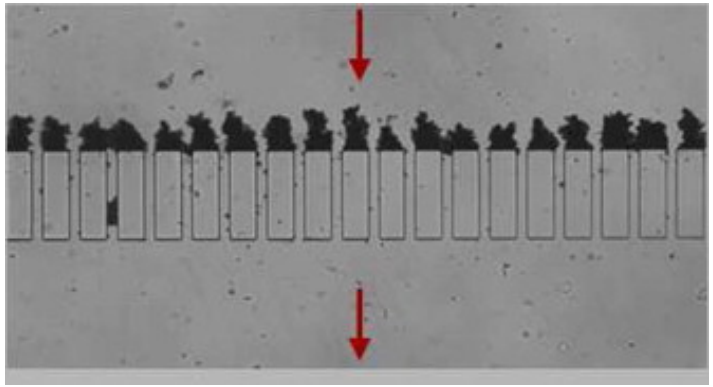
- Over time particulates buildup on surfaces and channel entrances (fouling) resulting in channel blockage .
- Clogging can prevent certain regions of the chip from being adequately cooled.
- Fouling can result in additional thermal resistances reducing heat exchanger efficiency.

As microfluidic passages become smaller and smaller, clogging and fouling concerns become increasingly critical to consider.

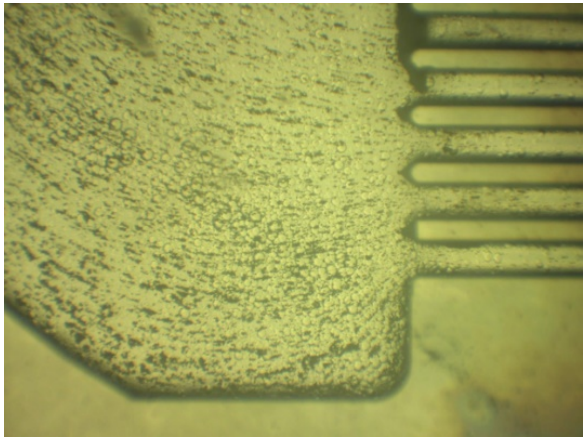
R. Mandel, S. Dessiatoun and M. Ohadi, "Embedded two-phase cooling of high flux electronics using a directly bonded FEEDS manifold," *2016 15th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, Las Vegas, NV, 2016, pp. 77-84.

Particulate Buildup in Microfluidic Passages

- Previous studies have shown that particulate build-up and clogging within the microchannels are not likely to occur.



Particulate formations on the fin surfaces connect to block the channel entrance



Fouling occurs in the manifold while clogging occurs at the channel entrances

- Major location of fouling is within header/manifold region due to the lower shear stress and abrupt changes in flow direction as fluid enters channels.
- One of the best ways to control particle agglomeration and build-up is by adjusting pH and very stringent particle filtering controls (e.g. less than 0.5µm).

Conclusions

- 3D integrated power electronics will use new packaging technologies the reliability of which will need to be understood and modeled.
  - Sintered Interconnects
  - Embedded Actives and Passives
  - 3D Integrated Thermal Management
- Power electronics will become ever more important as it is the critical enabling technology sitting at the intersection of renewable power generation, reliable power distribution and transmission, and efficient power utilization and storage.
- Addressing the reliability issues inherent in compact and high power density packaging which includes integrated thermal management will be the most important research area for realizing the full potential of power electronics.