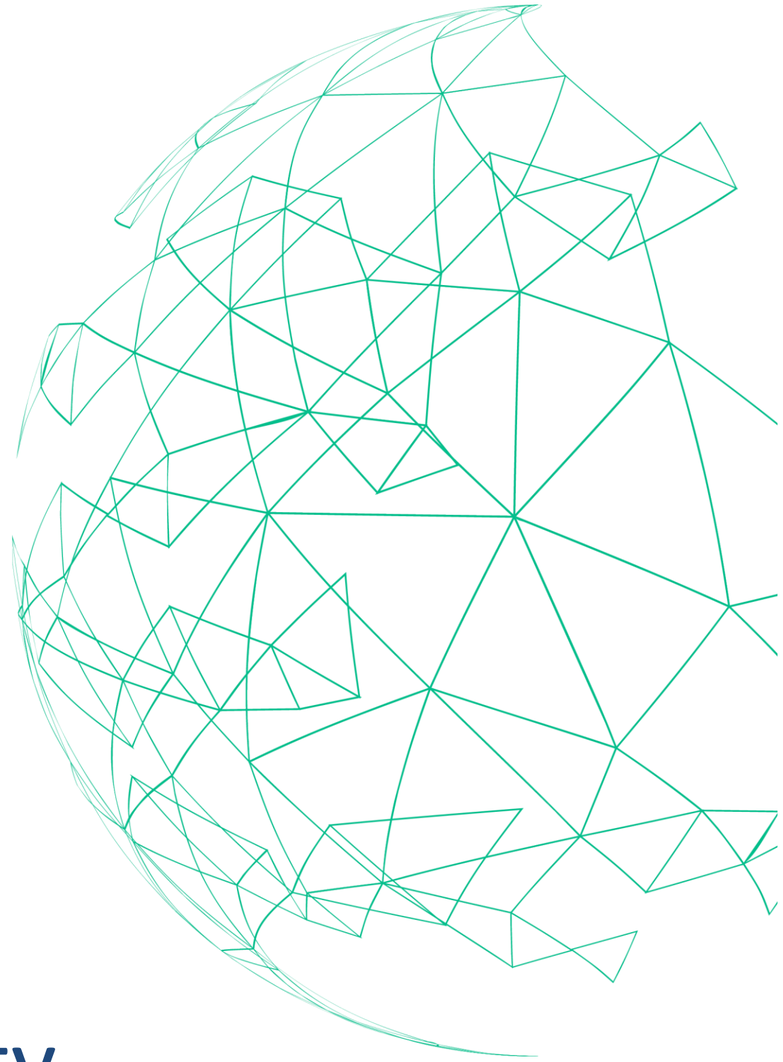


Rugged, high-performance 650 – 1200V SiC MOSFETs with flawless gate oxide integrity

Additional info here.

Martin Domeij, Fredrik Allerstam and Thomas NEYER of ON Semiconductor

Agenda

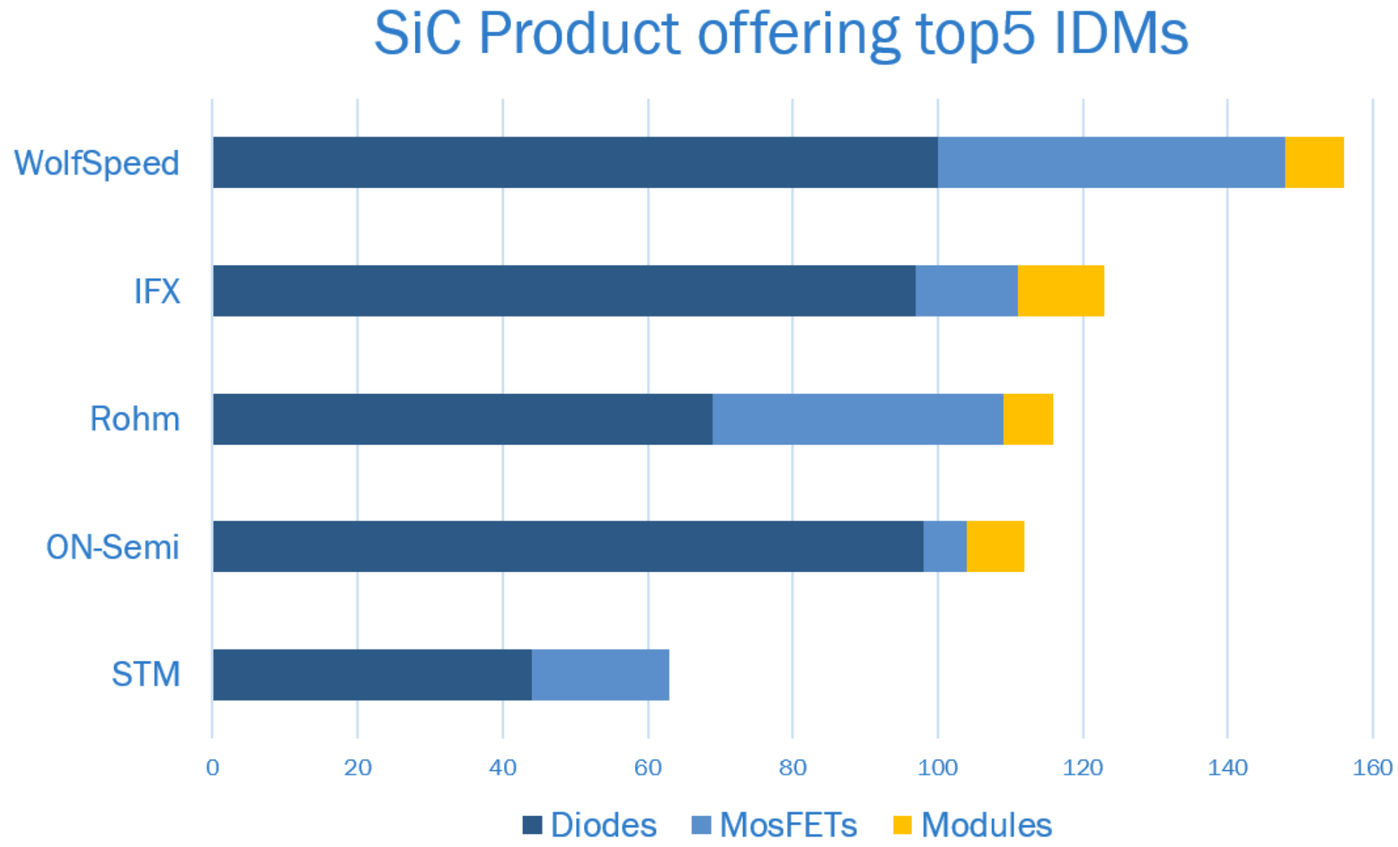
- ON’s growing SiC product portfolio
- SiC MosFET Gate drives – harmonization in sight?
- Speedlimit for discrete SiC MosFETs – the body diode
- How to sustain a flawless gateoxide on defective material
- Paralleling of MosFET (worst case spread)

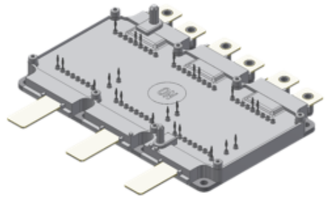
SiC products on the open market Q4/2019

ON released 1st 6” SiC product in 2015 and has grown its portfolio

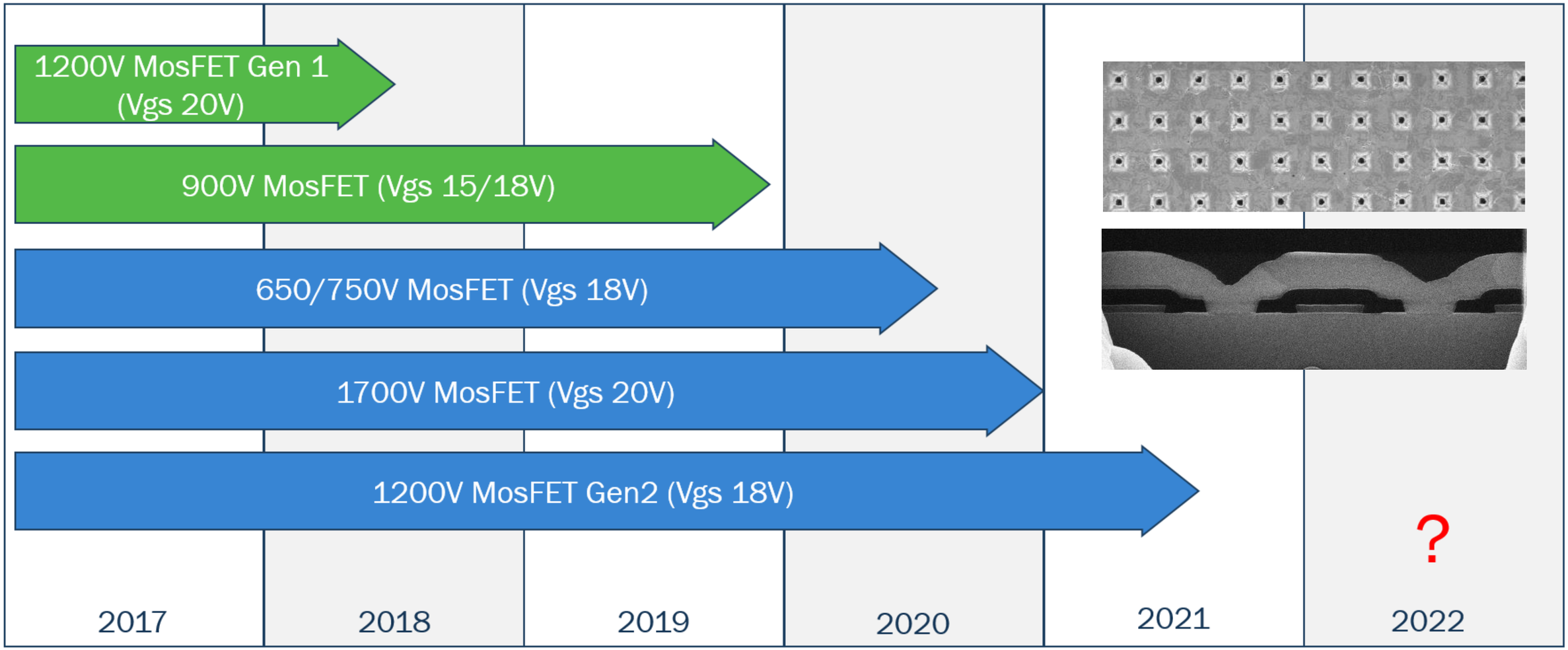
Key focus on automotive qualification and supply chain superiority

Comparable FOM on Diodes and MosFETs between top 5 suppliers





AEC-Q101 SiC MosFET platform roll-out



Gate drive voltage range – What's the right choice?

Silicon:

HV transistors allow symmetrical Gate-Source maximum ratings and recommended drive conditions

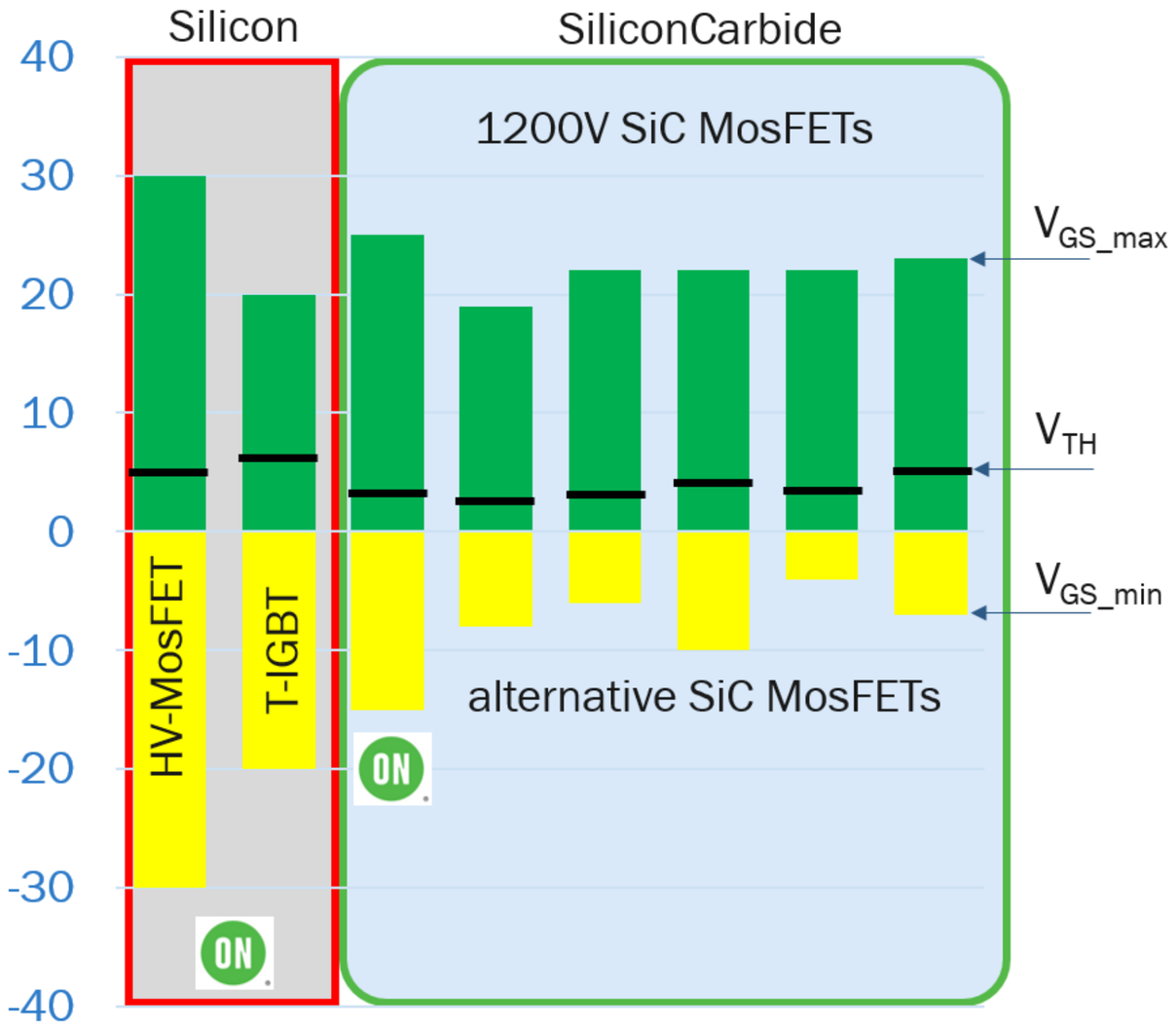
V_{TH} is standardized at >4V

SiC:

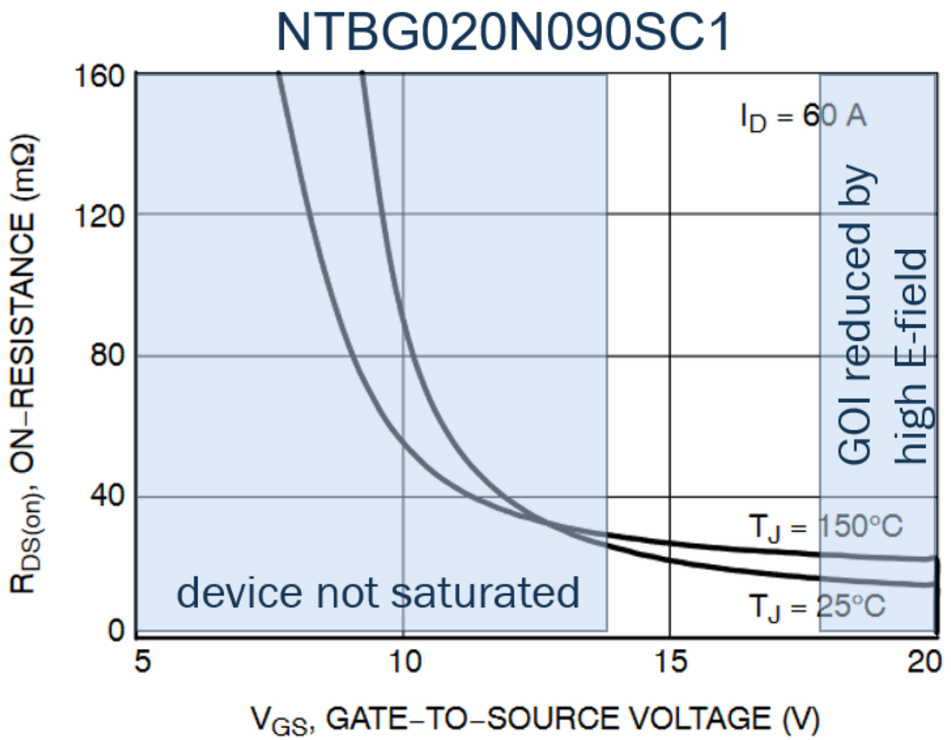
VTH of majority of suppliers is ~3V

most MosFETs are more sensitive at negative voltage

recommended drive conditions range from 15-20V / -- (5-0)V

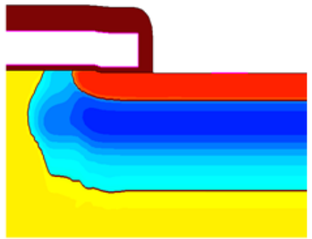


Gate drive voltage range – What's the right choice?



Device lifetime ⬆

➔ reduce TOX (at constant E-field)



- R_{Ch} reduces
- extrinsic tail reduces

➔ Lifetime increases

- V_{TH} reduces
- V_{GS_OP} range reduces

The best SiC MosFET is optimized for device lifetime not for compatibility to legacy Silicon gate drives

Gate drive voltage range – bipolar vs unipolar drive?

For convenience and cost saving desire for unipolar drive (no negative supply required)

➔ Increase of switching losses to be expected

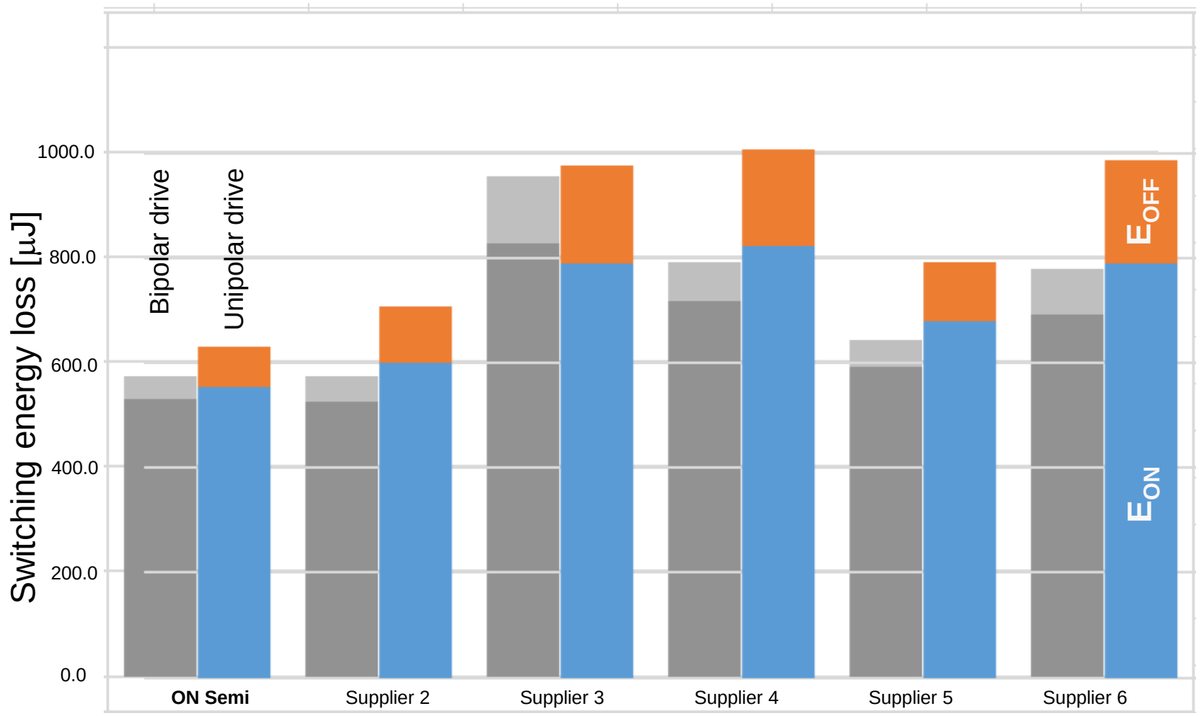
➔ risk for miller turn-on in half-bridge

➔ Increase of reverse leakage

Not recommended but acceptable for most SiC MosFETs on the market

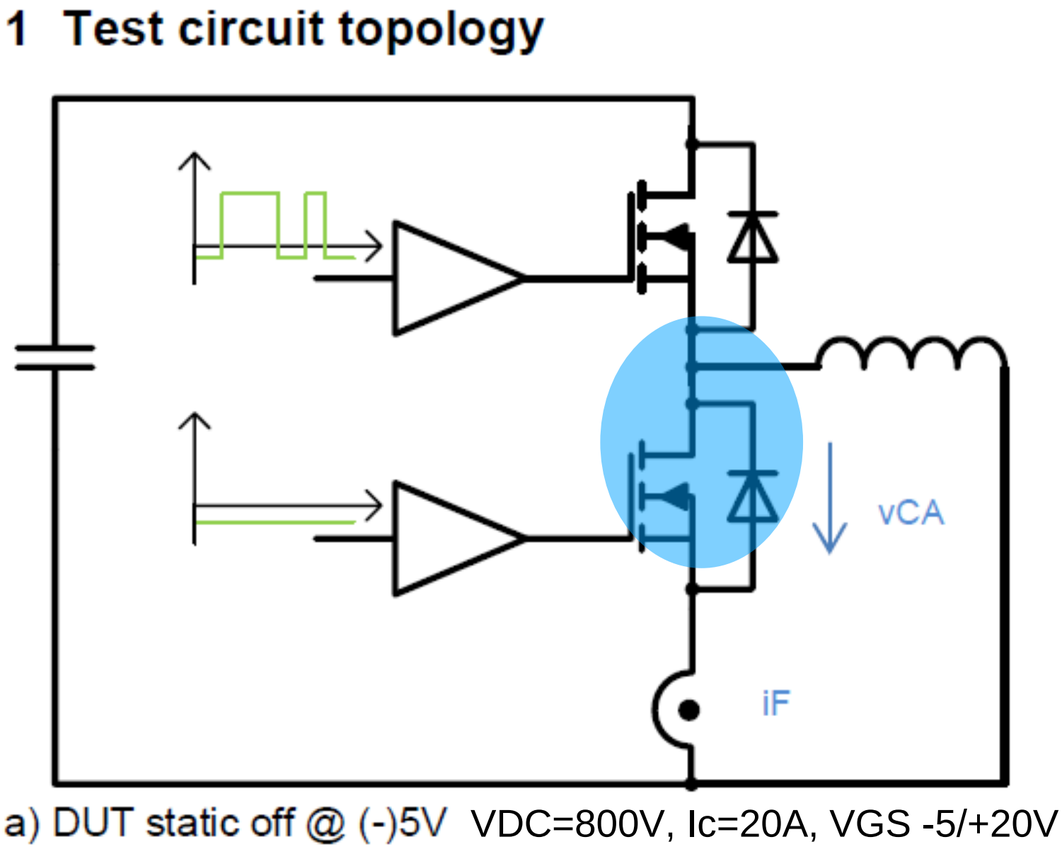
1200V 75 – 90mΩ devices – Double pulse test, 800V VDC, 20Am Rg=4.7Ω

Gate drive: as recommended vs VGS_min = 0V using NCP51705 ON-Semi



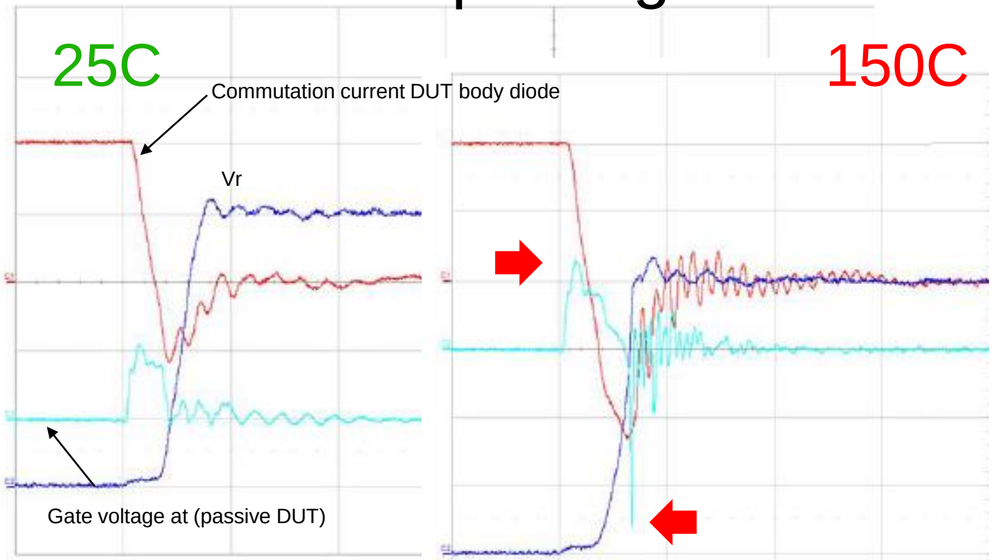
Adopting SiC MOSFETs for high speed operation

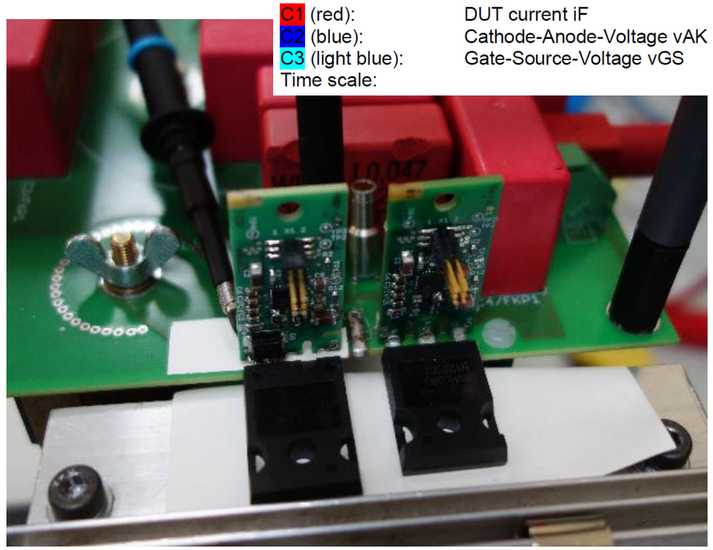
- Extreme switching speeds put requirements on a lower inductance environment, especially source inductance and use of Kelvin source
- Methods to dampen oscillations from all sources, careful choice of Rg to design for speed but maintain a stable circuit
- Low internal Rg gives bigger design space, but require more from the designer to manage the switching speed and inductive environment



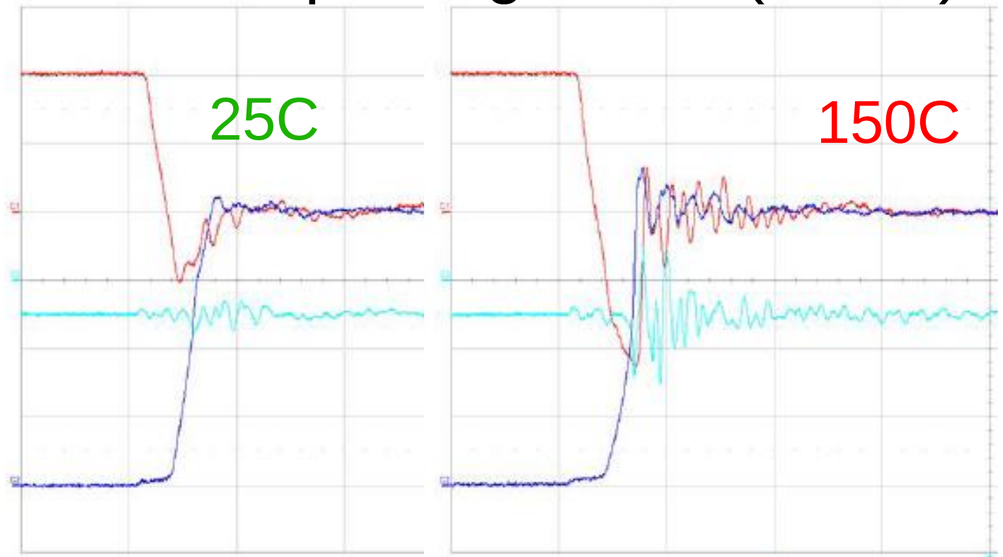
Adopting SiC MOSFETs for high speed operation

3 lead package case





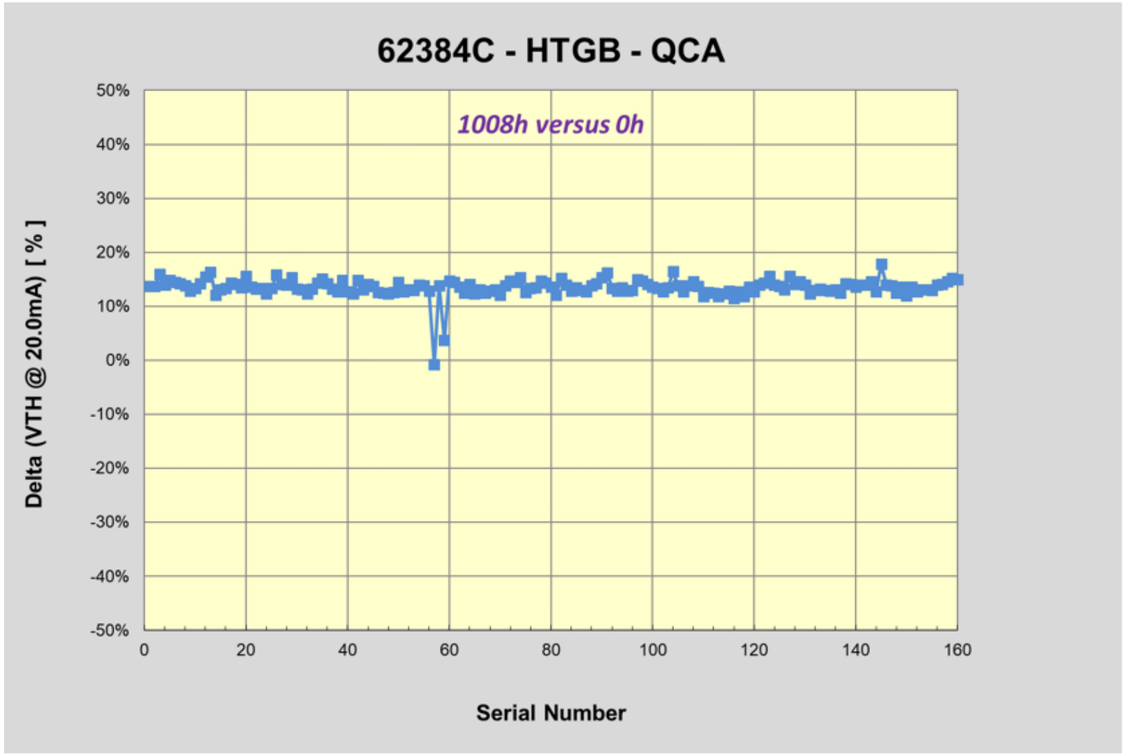
4 lead package case (kelvin)

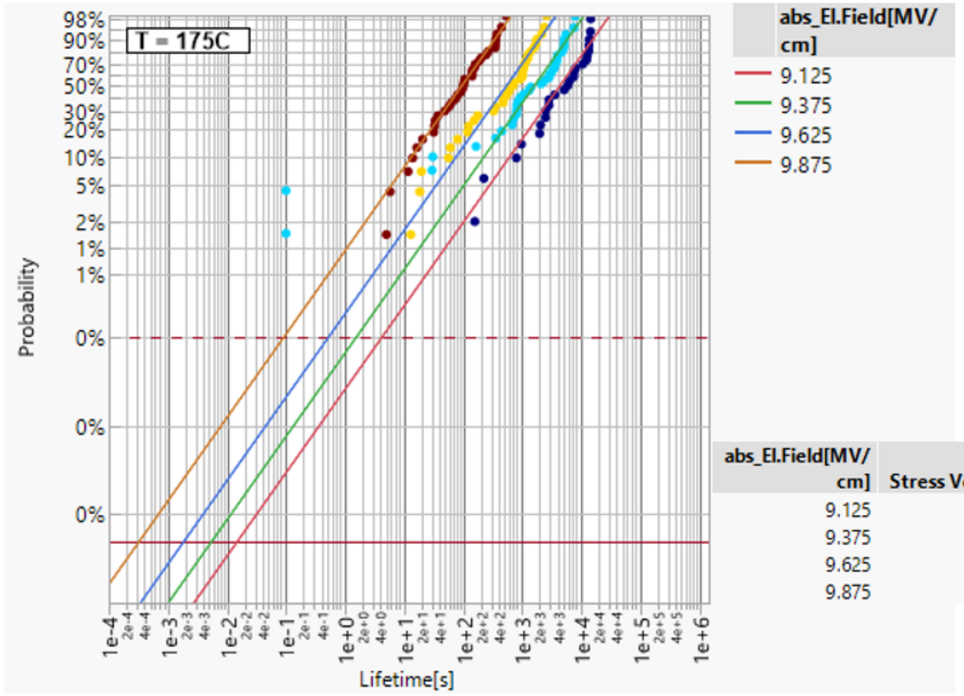


	Irr_max [A]	Vr_max [V]	trr [ns]	dv/dt [kV/us]	di/dt [A/us]	
25C	-21.6	900	32.5	102	1981	
150C	-32.2	992	33.7	112	2156	3 lead
25C	-26.5	866	11.2	186	4566	
150C	-45.5	1265	16.1	388	5477	4 lead

Even simple discrete setups can be accelerated to extreme speeds – body diode can get very snappy at high temperatures. Stay within SOA

Gateoxide reliability - intrinsic capability





abs_El.Field[MV/cm]	Stress Voltage[V]
9.125	36.50
9.375	37.50
9.625	38.50
9.875	39.50

Recoverable Vth drift after 1000hrs, 175C, Vgs=25V <20%

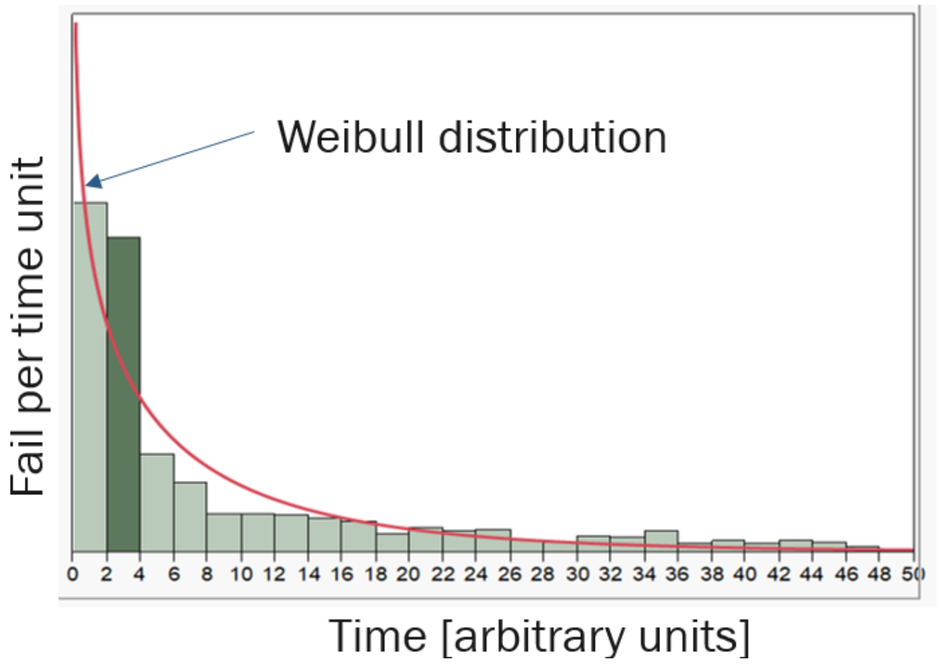
Intrinsic GOX comparable to planar Silicon devices.

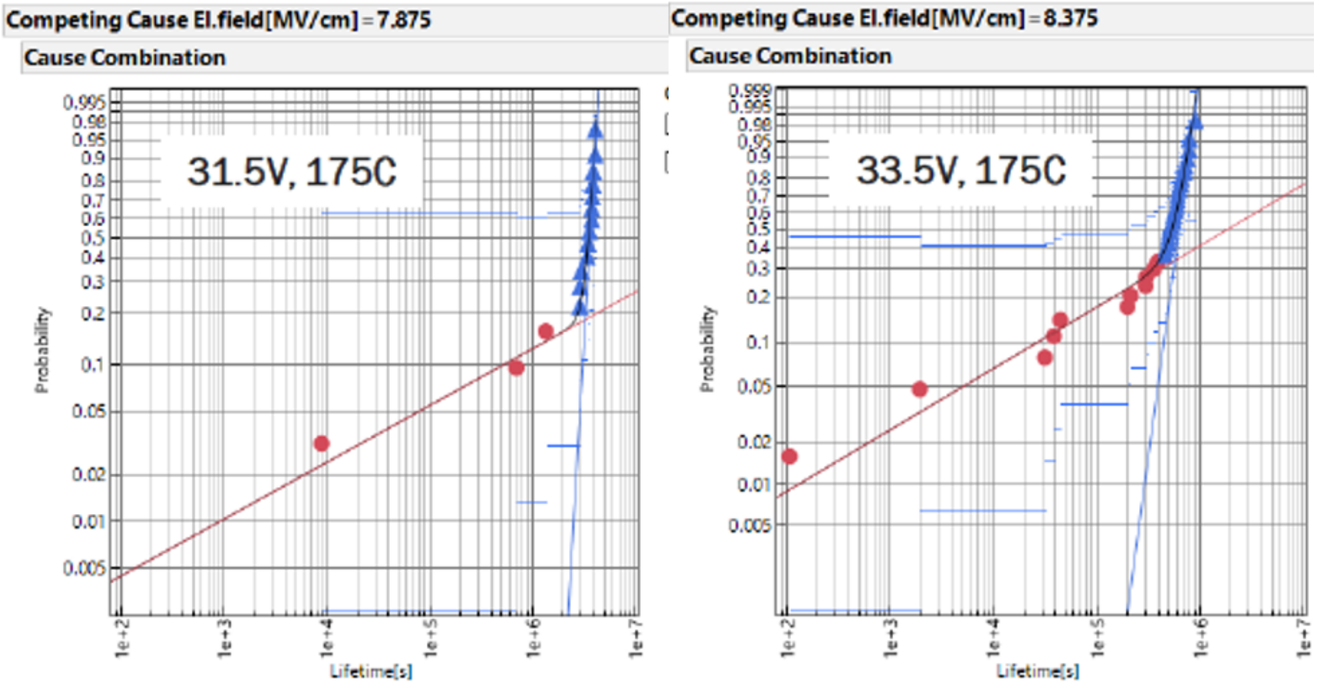
900V WLR @ 6 cm^2	Results	unit
Tox	400	*Å*
Temperature	175	*°C*
Vgs op	15	*V*
Weibull slope β	0.941	
E-model Gamma	3.03	*cm/MV*
FIT @ 20yrs VGS_max	<0.1	*ppb*

How about extrinsic tail in SiC MosFETs?

Screening methodology:

- removal of crystal defects
- gate stress test
- avalanche stress test
- parametric test on wafer and package level
- burn-in on wafer-level



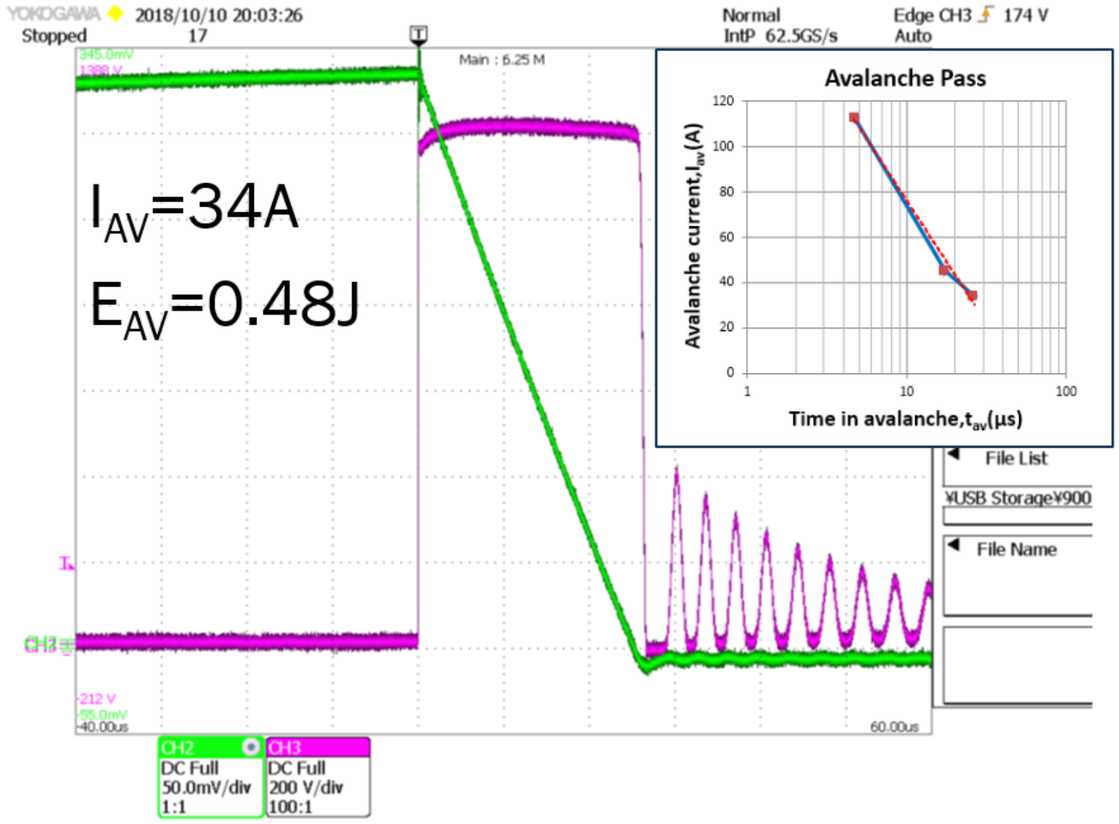


Well proven Silicon test screening methodology is not sufficient to prevent infant mortality

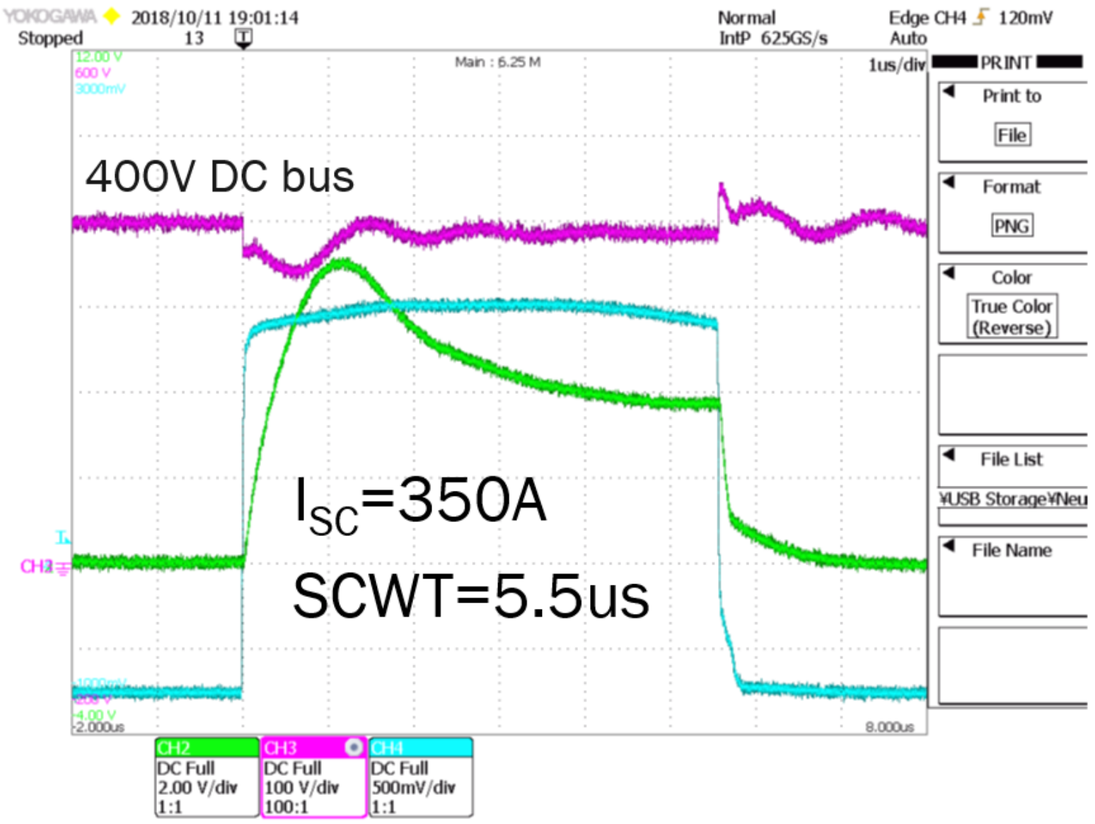
Post BI failure rate is extracted to be comparable to HV Silicon devices

Robustness testing: 900V MosFET platform

Avalanche test 60mOhm (1mH)



Short Circuit capability (Type2)

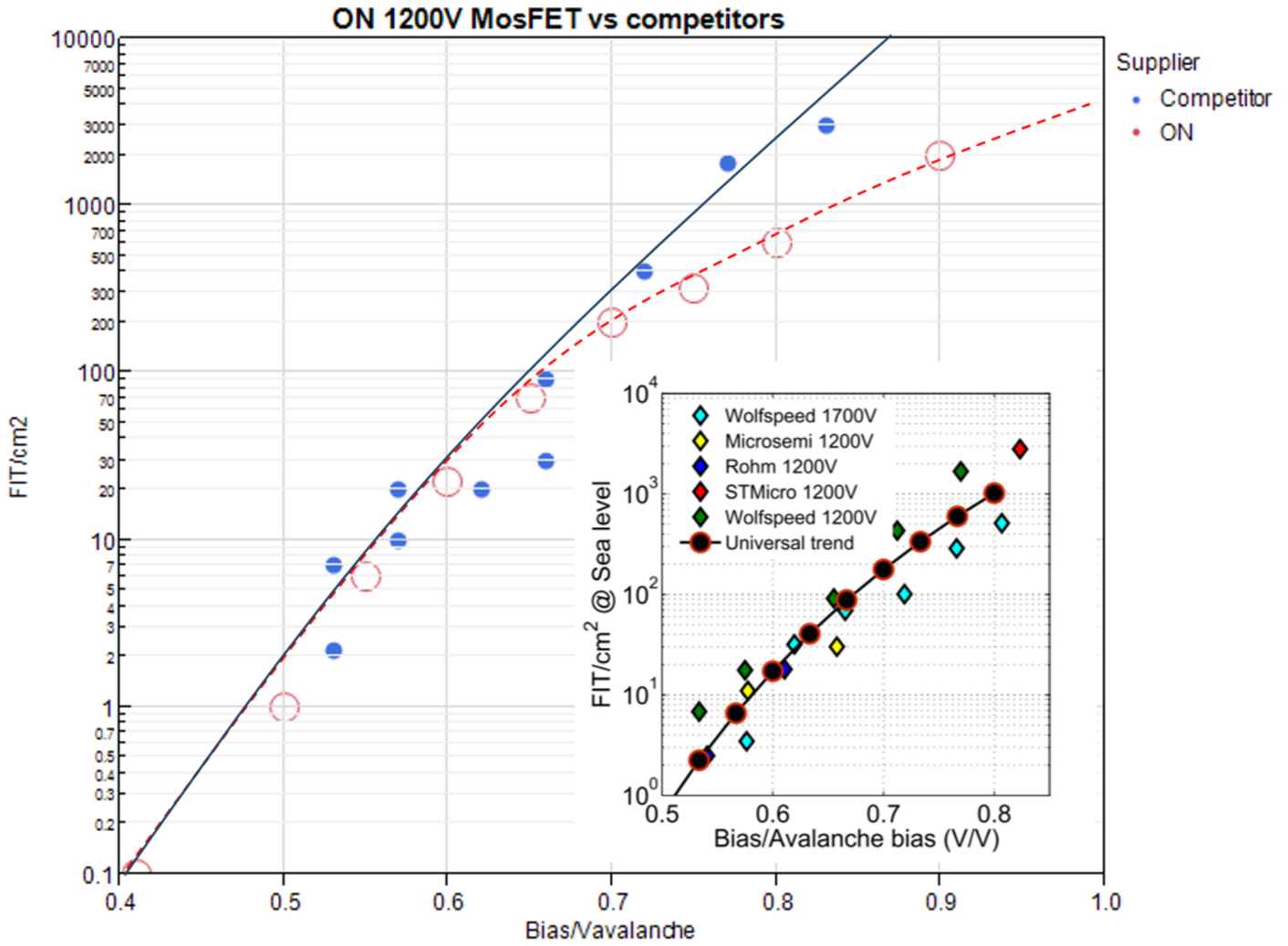


Ruggedness against cosmic rays (@sea level)

According to Akturk et al, there appears to be a universal dependency FIT vs bias

Device field optimization and drift layer design can significantly alter/improve this relationship at higher fields

Systematic optimization yields lowest failure rates

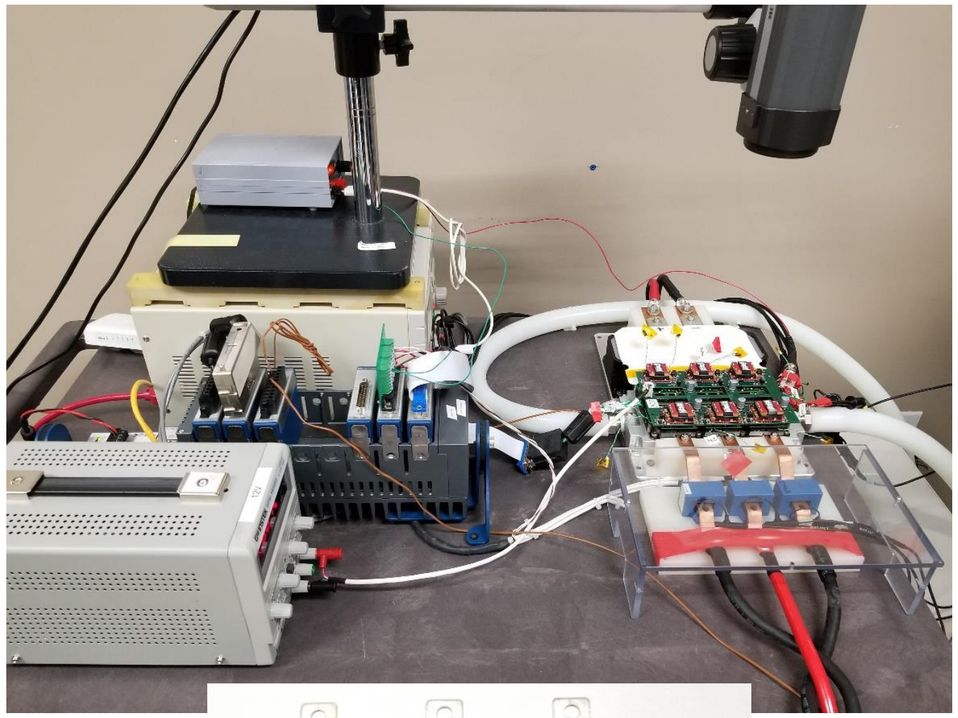


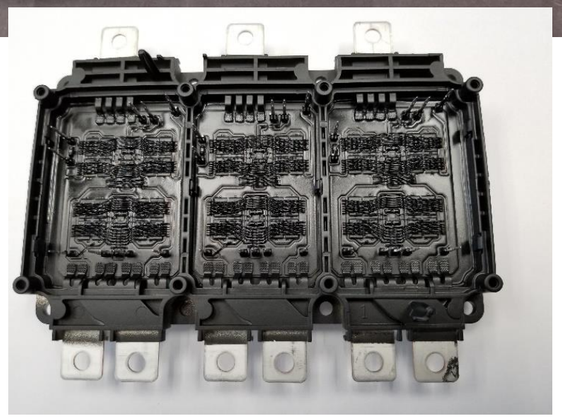
A. Akturk, J. McGarrity, N. Goldsman, D. J. Lichtenwalner, B. Hull, D. Grider, R. Wilkins, "**The effects of radiation on the terrestrial operation of SiC MOSFETs**," Int. Reliability Physics Symposium (IRPS), (11-15 March 2018).

SiC MosFET paralleling – exercise to assess Temperature offsets

- Production variation results in finite parameter distributions i.e Vth, Rdson, HVbr,...
- To enable high current ratings several large SiC MosFETs are being paralleled
- Statistical thermoelectrical models can be used to assess the dynamic effect of worst case (ref paper J. Victory)
- Cherry-pick assembly of extreme-offset Rdson are being used to confirm simulation prediction

- Opened, black module, 3 phase drive at 600VDC, glycol/water cooling loop, Flir camera

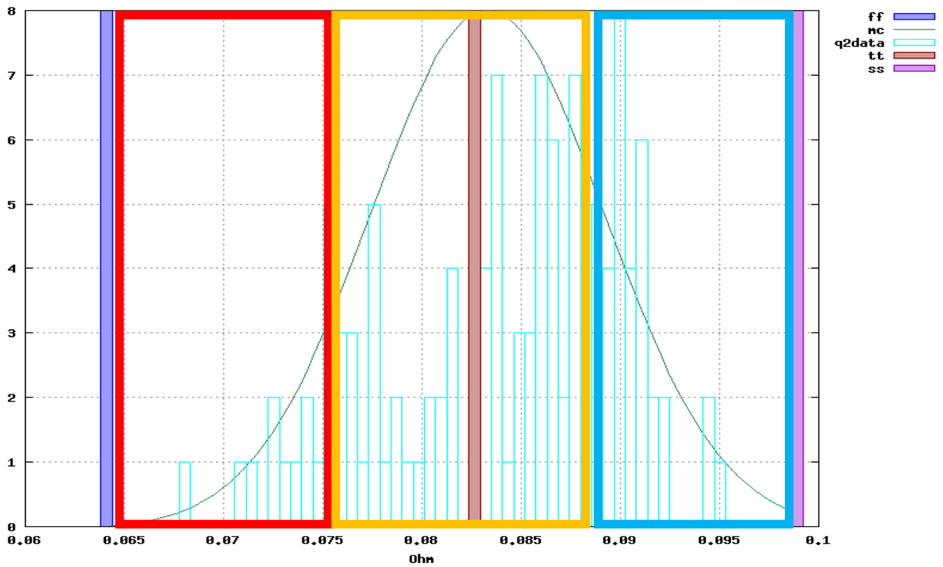


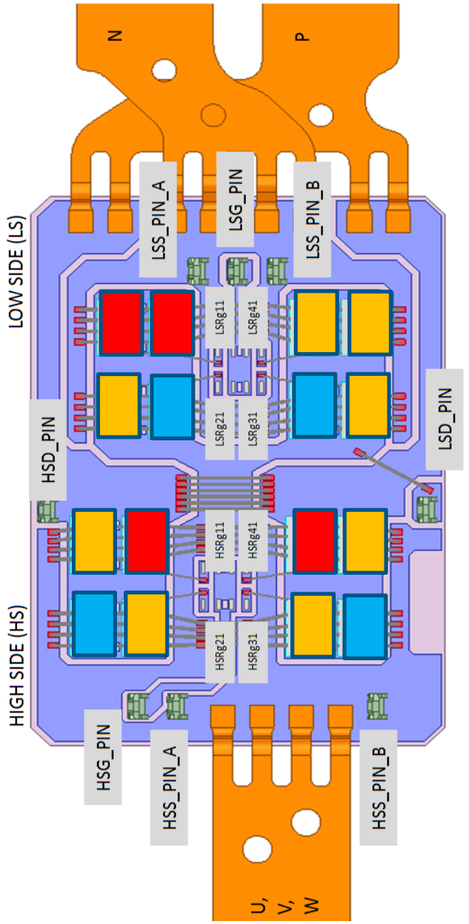


Courtesy to Roy Davies and Yifan Xiao, Ann Arbour

SiC MosFET paralleling – exercise to assess Temperature offsets

- Typical distribution on a random SiC MosFET wafer – assembled onto module





Rdson Hi/Lo/Med?	Die Location	Module 1 (U,V,W)
Lo	HS3	143,146,113
Lo	HS8	198,242,135
Lo	LS4	144,114,361
Lo	LS3	197,81,380
Med	HS4	68,92,436
Med	HS7	89,109,398
Med	LS7	258,438,34
Med	LS8	150,65,193
Med	HS2	325,327,32
Med	HS5	247,329,363
Med	LS1	91,376,375
Med	LS6	377,214,251
Hi	HS1	445,216,104
Hi	HS6	162,404,391
Hi	LS2	221,30,39
Hi	LS5	500,250,347

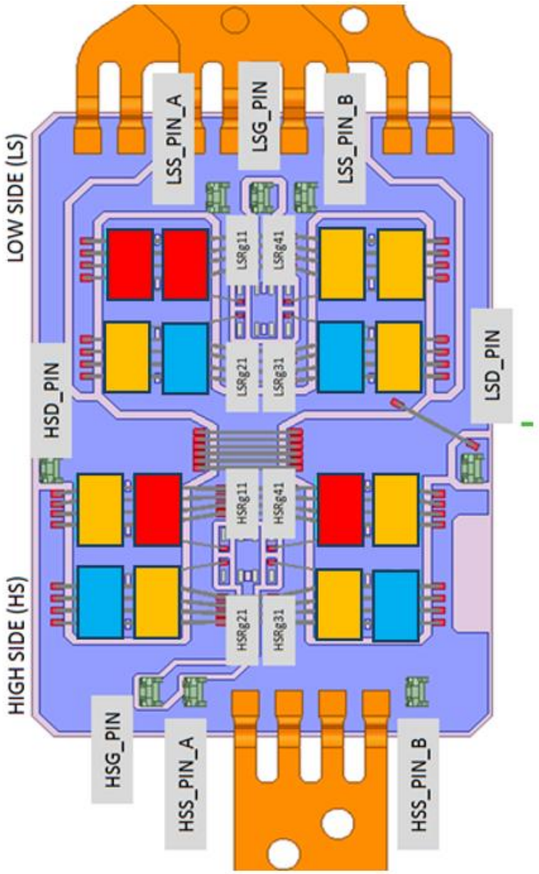
Predicted Hottest

Predicted Moderate

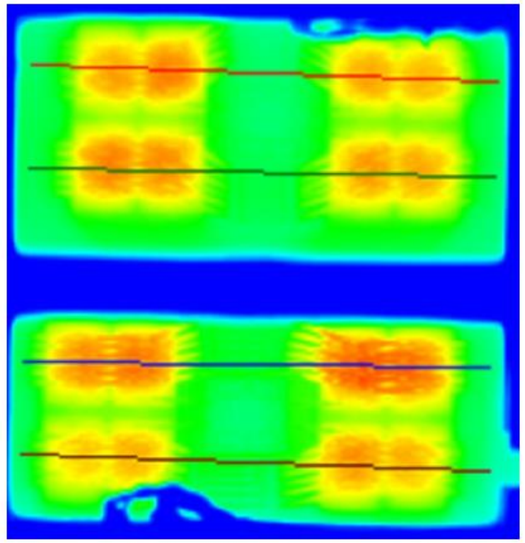
Predicted Coolest

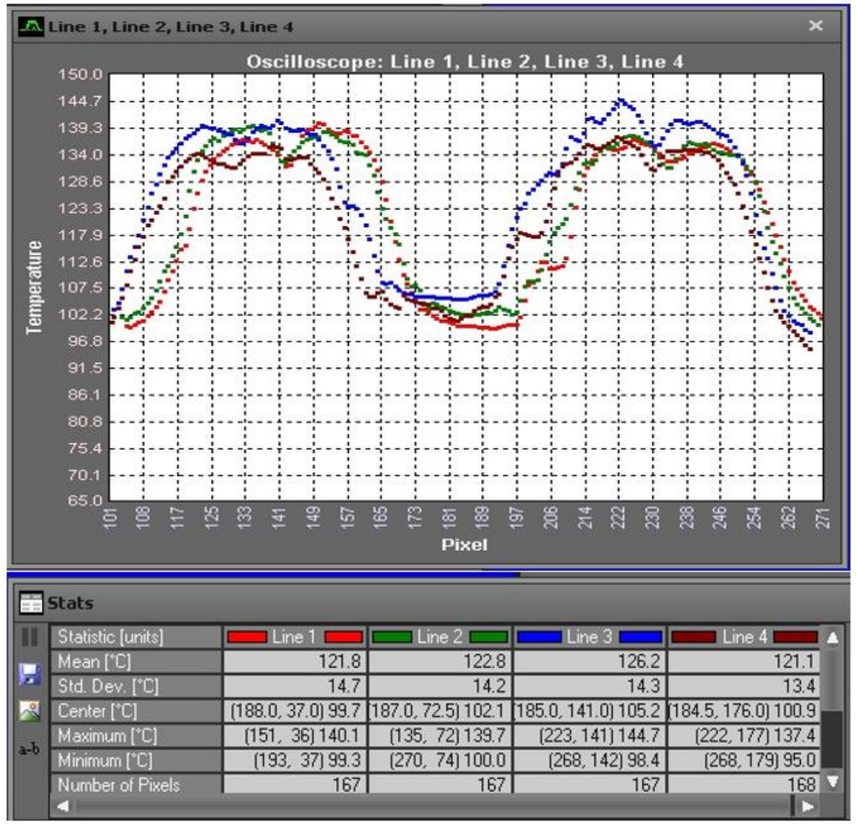
Courtesy to Roy Davies and Yifan Xiao, Ann Arbour

SiC MosFET paralleling – exercise to assess Temperature offsets



W Phase – 600VDC, 640Apk, 10 kHz f_{sw}





Stats

Statistic [units]	Line 1	Line 2	Line 3	Line 4
Mean [°C]	121.8	122.8	126.2	121.1
Std. Dev. [°C]	14.7	14.2	14.3	13.4
Center [°C]	(188.0, 37.0) 99.7	(187.0, 72.5) 102.1	(185.0, 141.0) 105.2	(184.5, 176.0) 100.9
Maximum [°C]	(151, 36) 140.1	(135, 72) 139.7	(223, 141) 144.7	(222, 177) 137.4
Minimum [°C]	(193, 37) 99.3	(270, 74) 100.0	(268, 142) 98.4	(268, 179) 95.0
Number of Pixels	167	167	167	168

Oscilloscope plot shows about 5C per vertical division, or about 7C temperature difference from hottest to coolest die.

Courtesy to Roy Davies and Yifan Xiao, Ann Arbour

OUTLOOK

- 650V – 1700V SiC devices are turning into a commodity
  - Customization for volume application
  - comparable ratings
  - tradeoff btw current density and thermal performance
- High reliability and robustness standards are being established
- SiC device and package innovation will enable several more product generations

Thank you