GaN Systems

TRANSFORMING THE WORLD

WITH SMALLER, LOWER COST, MORE EFFICIENT POWER ELECTRONICS

GaN Systems Demonstrates Reliability Based on Qualification and Lifetime Data

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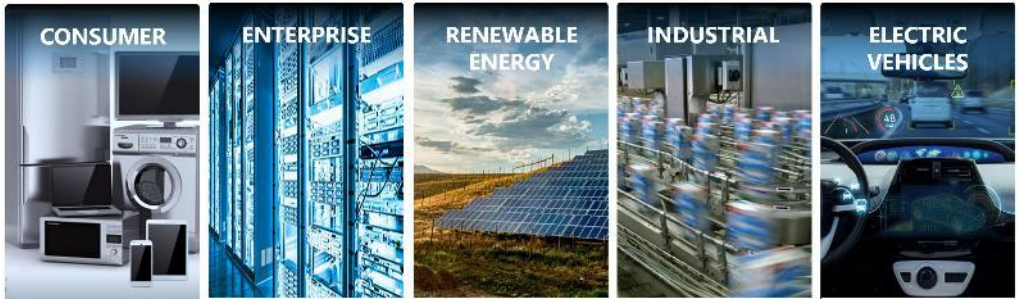
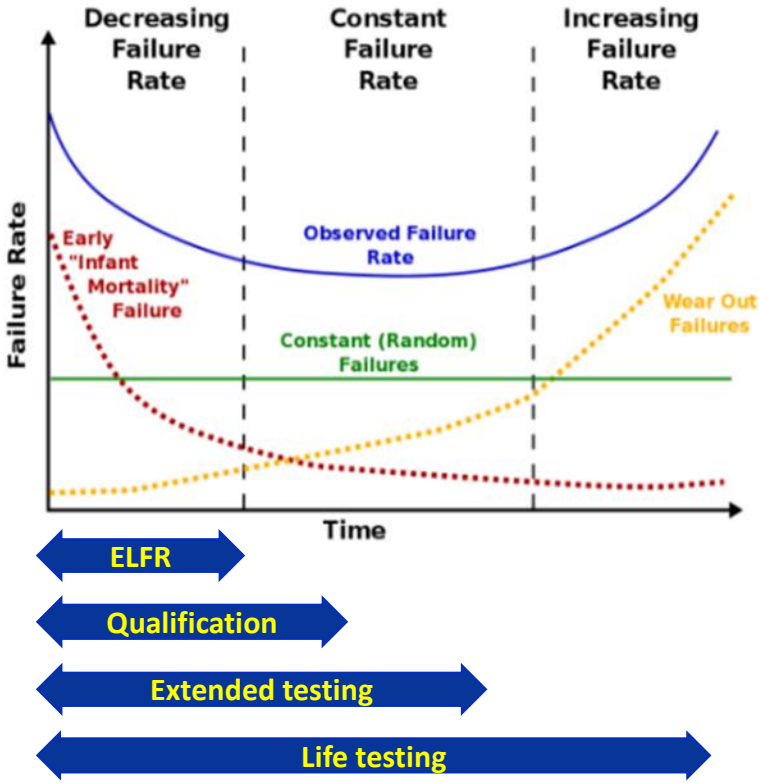
Is GaN reliable ?

- Test theory and approach
- Qualification standards
- Beyond the standards
- Lifetime and FIT
- Industry benchmarks

GaN Reliability



- Independent of market segment, customers require reliable devices
- Standard JEDEC & AEC-Q101 tests are applied as a baseline
- Additional test methods are implemented for the differences between Silicon and GaN
- To assure reliability, GaN Systems tests for both extrinsic and intrinsic failures
- Failure modes and mechanisms are identified using FMEA & test-to-failure methods



GaN JEDEC Qualification: 650V

- GaN Systems successfully achieved full JEDEC qualification on 650V product line.

Test	Conditions	Sample size (parts x lots)							Failures
		GS66502B 200mΩ	GS66504B 100mΩ	GS66506T 67mΩ	GS66508B 50mΩ	GS66508T 50mΩ	GS66516B 25mΩ	GS66516T 25mΩ	
HTRB	T_j = 150°C, V_{DS} = 80%, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
HTGB	T_j= 150°C, V_{GS} = 100%, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
	T_j= 150°C, V_{GS} = -100%, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
H3TRB	T_j= 85°C, RH= 85%, V_{DS}= 100V, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
TC	-40°C to +125°C, 1000 cycles	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
HTS	T_a= 150 °C, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
IOL	ΔT_j= 100°C, 2 min on, 2 min off, 5k cycles	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
MSL3	T_a= 60°C, RH=60%, t= 40 hrs followed by 3x reflow cycles	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
ESD	HBM+CDM	30x1	30x1	30x1	30x1	30x1	30x1	30x1	0
Solderability	Dry bake (condition E)	10x3	10x3	10x3	10x3	10x3	10x3	10x3	0

GaN JEDEC Qualification: 100V

- GaN Systems successfully achieved full JEDEC qualification on 100V product line.

Test	Conditions	Sample size (parts x lots)			Failures
		GS61004B 15mΩ	GS61008P 7mΩ	GS61008T 7mΩ	
HTRB	T_j = 150°C, V_{DS} = 80%, t= 1000 hrs	77x3	77x3	77x3	0
HTGB	T_j= 150°C, V_{GS} = 100%, t= 1000 hrs	77x3	77x3	77x3	0
	T_j= 150°C, V_{GS} = -100%, t= 1000 hrs	77x3	77x3	77x3	0
H3TRB	T_j= 85°C, RH= 85%, V_{DS}= 80%, t= 1000 hrs	77x3	77x3	77x3	0
TC	-40°C to +125°C, 1000 cycles	77x3	77x3	77x3	0
HTS	T_a= 150 °C, t= 1000 hrs	77x3	77x3	77x3	0
IOL	ΔT_j= 100°C, 2 min on, 2 min off, 5k cycles	77x3	77x3	77x3	0
MSL3	T_a= 60°C, RH=60%, t= 40 hrs followed by 3x reflow cycles	77x3	77x3	77x3	0
ESD	HBM+CDM	30x1	30x1	30x1	0
Solderability	Dry bake (condition E)	10x3	10x3	10x3	0

GaN AEC-Q101 Qualification

- Select GaN Systems' 650V transistors are qualified to AECQ-101.

Test	Conditions	Sample size (parts x lots)						Failures
		GS66508B 50mΩ	GS66508T 50mΩ	GS66516B 25mΩ	GS66516T 25mΩ	GS-065-060-5-T-A 25mΩ	GS-065-060-5-B-A 25mΩ	
HTRB	T_j = 150°C, V_{DS} = 100%, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	0
HTGB	T_j= 150°C, V_{GS} = 100%, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	0
	T_j= 150°C, V_{GS} = -100%, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	0
H3TRB	T_j= 85°C, RH= 85%, V_{DS}= 100V, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	0
UHAST	T_j= 130°C, RH= 85%, t= 96 hrs	77x3	77x3	77x3	77x3	77x3	77x3	0
TC	-40°C to +125°C, 1000 cycles	77x3	77x3	77x3	77x3	77x3	77x3	0
HTS	T_a= 150 °C, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	0
LTS	T_a= -55 °C, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	0
IOL	ΔT_j= 100°C, 2 min on, 2 min off, 15k cycles	77x3	77x3	77x3	77x3	77x3	77x3	0
MSL3	T_a= 60°C, RH=60%, t= 40hrs followed by 3x reflow cycles	77x3	77x3	77x3	77x3	77x3	77x3	0
ESD	HBM+CDM	300x1	300x1	300x1	300x1	300x1	300x1	0
Solderability	Dry bake (condition E)	10x3	10x3	10x3	10x3	10x3	10x3	0

GaN JEDEC+ Qualification

- GaN Systems has implemented a JEDEC+ design and test methodology
- The tests incorporate the differences between GaN and Silicon transistors
- Each test was designed based on a specific failure mechanism in FMEA

Test	Test Duration	Failures
Switching HTRB (AC)	1000 hrs	0
HTRB with Negative Gate Voltage	1000 hrs	0
Switching HTGB (AC)	1000 hrs	0
Low Temperature Reverse Bias (LTRB)	1000 hrs	0
Highly Accelerated Stress Test (HAST)	96 hr	0
Low Temperature Storage (LTS)	1000 hrs	0

GaN AEC-Q101+ Qualification

- AEC-Q101+ product reliability test methods were developed to properly evaluate the differences between GaN and Silicon transistors
- Each test was designed based on a specific failure mechanism in FMEA

Test	Test Duration	Failures
Higher Voltage H3TRB	1000 hrs	**0**
Dynamic High Temperature Operating Life (DHTOL)	1000 hrs	**0**
Wider Temperature Range Temperature Cycling	1000 cycles	**0**
Thermal Shock (TS)	1000 cycles	**0**
Faster Ramp IOL testing	1000 hrs	**0**

Extended Testing Demonstrates Significant Margin

- GaN Systems increases confidence levels by testing beyond duration requirements

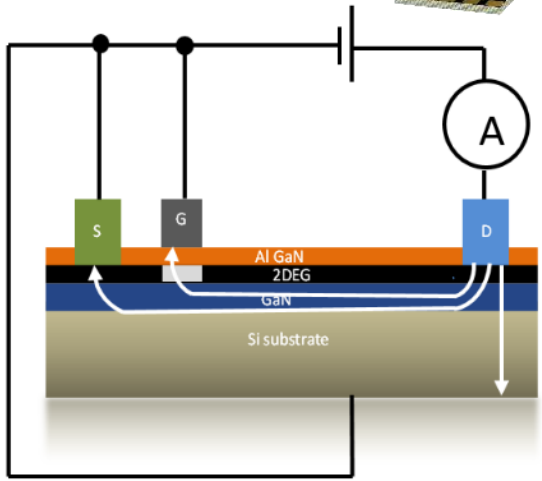
Test	Status	Extended*
HTRB	27,000 hrs **(>3 years!)**	27x
LTRB	3,000 hrs	3x
HTGB	5,000 hrs	5x
DHTOL	5,000 hrs	5x
H3TRB	5,000 hrs	5x
TC	5,000 cycles	5x
LTS	3,000 hrs	3x
HTS	4,000 hrs	4x
IOL	70,000 cycles	14x

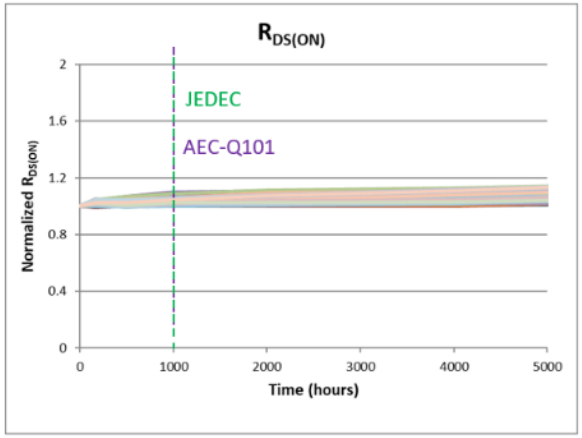
**Stable performance significantly beyond JEDEC requirement*

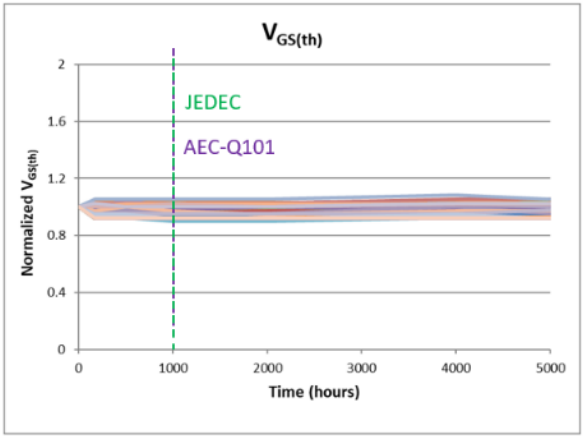
Extended Qualification testing demonstrates significant margin over standard JEDEC durations

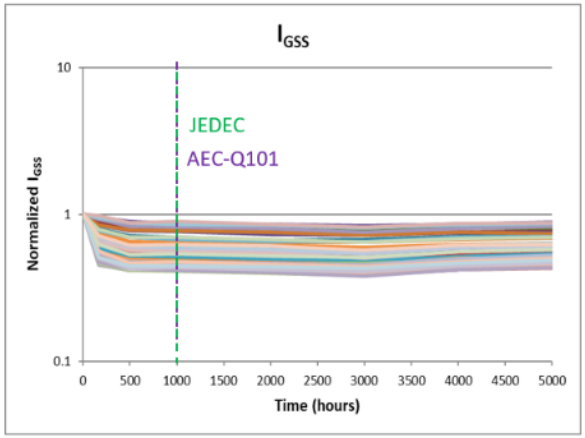
Extended Testing Example

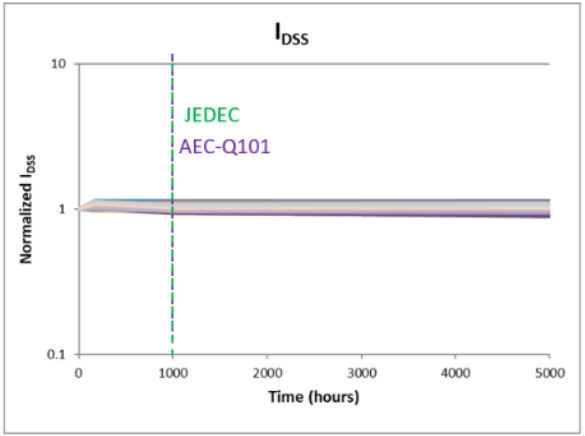
Test	H3TRB
Conditions	85°C/85% RH, 100V
Readings	168/500/1000/2000/3000/4000/5000 hours
Test Method	JESD22-A101
Part	GS66508B











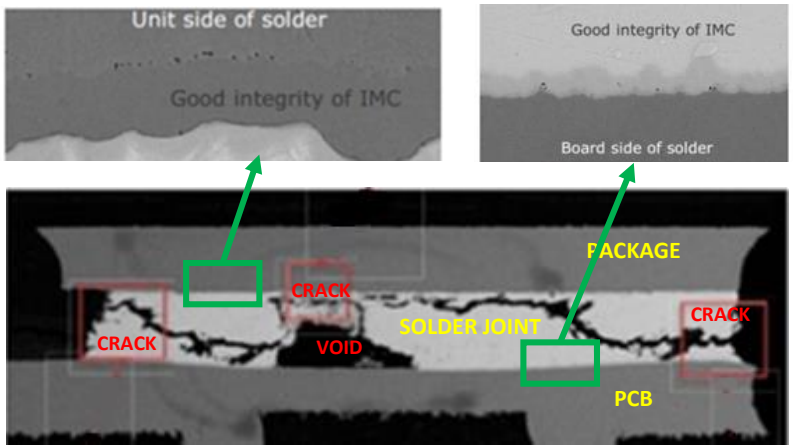
Stable performance over 5000 hours of extended biased humidity

IPC9701 Solder Joint Reliability

1. Standard: No Failures
   - 1000 cycles, -40 to 125°C
   - 8 and 12 layer PCBs
2. Extended to 2000 cycles: No Failures
   - Good integrity of package intermetallics (IMC) and no cracking through the IMC
3. Test to failure
   - Package intermetallics: No Failures
   - Solder joint: Crack originated at solder joint void

Test to failure

- **Good integrity, no failure of IMC on both package side and board side after >2000 cycles**



- **Crack initiation from a solder joint void after >2000 cycles**

Conclusion

- Lifetime results are similar to standard QFN package
- As with all components, assembly process should minimize solder joint voiding

GaN Lifetime

- GaN Systems' product reliability:

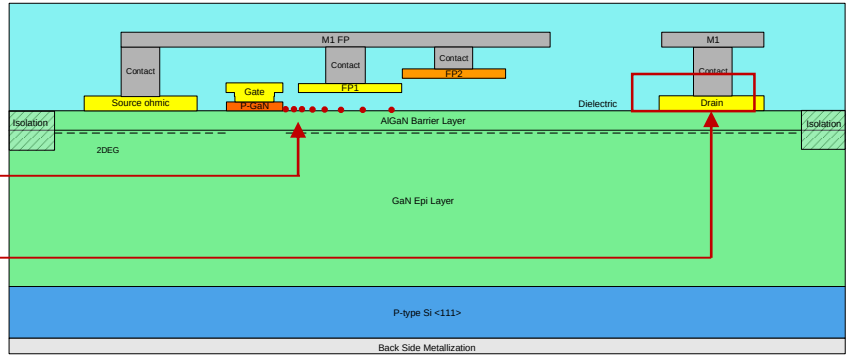
- Device failure modes and mechanisms are well-understood and modeled
- Step stress test results define stress level conditions for life testing
  - Critical to use conditions that achieve the relevant failure in a reasonable timeframe, and at the same time, do not activate any other failure mechanisms
- Voltage acceleration model
  - For reliability and acceleration testing, model can significantly affect the lifetime results
  - GaN Systems uses the most conservative model (Eyring)
  - GaN Systems uses conservative 90% confidence level for life calculations

Failure Modes and Mechanisms

- GaN Systems has identified, modeled and tested different failure modes. Here are four:

Drain

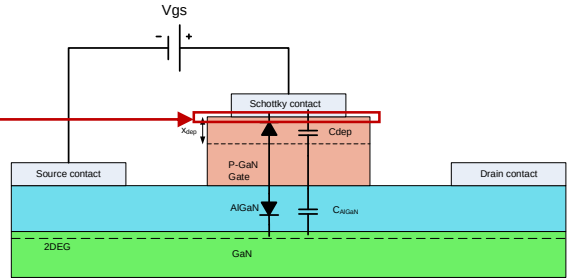
1. Charge Trapping
   - **Failure mode:** Increase in $R_{DS(on)}$
2. Drain Time-Dependent Dielectric Breakdown (TDDB)
   - **Failure mode:** Drain catastrophic failure



Gate

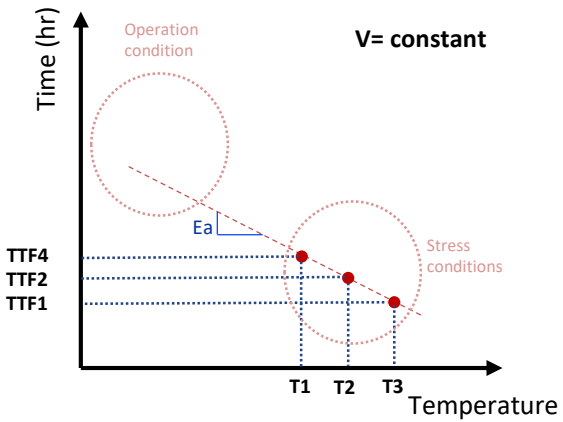
1. Gate Time-Dependent Schottky Breakdown (TDSB)
   - **Failure mode:** Gate catastrophic failure
2. Gate Oxide Time-Dependent Dielectric Breakdown (TDDB)
   - **Failure mode:** Gate catastrophic failure

GaN Systems has no Gate Oxide

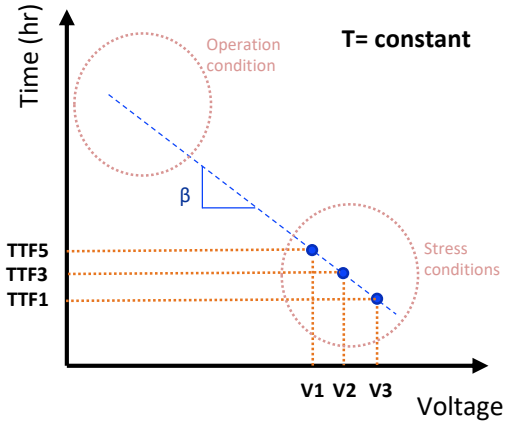


Failure modes are well understood and factored into the product design process

Lifetime Models



Temperature acceleration



Voltage acceleration

Acceleration Models

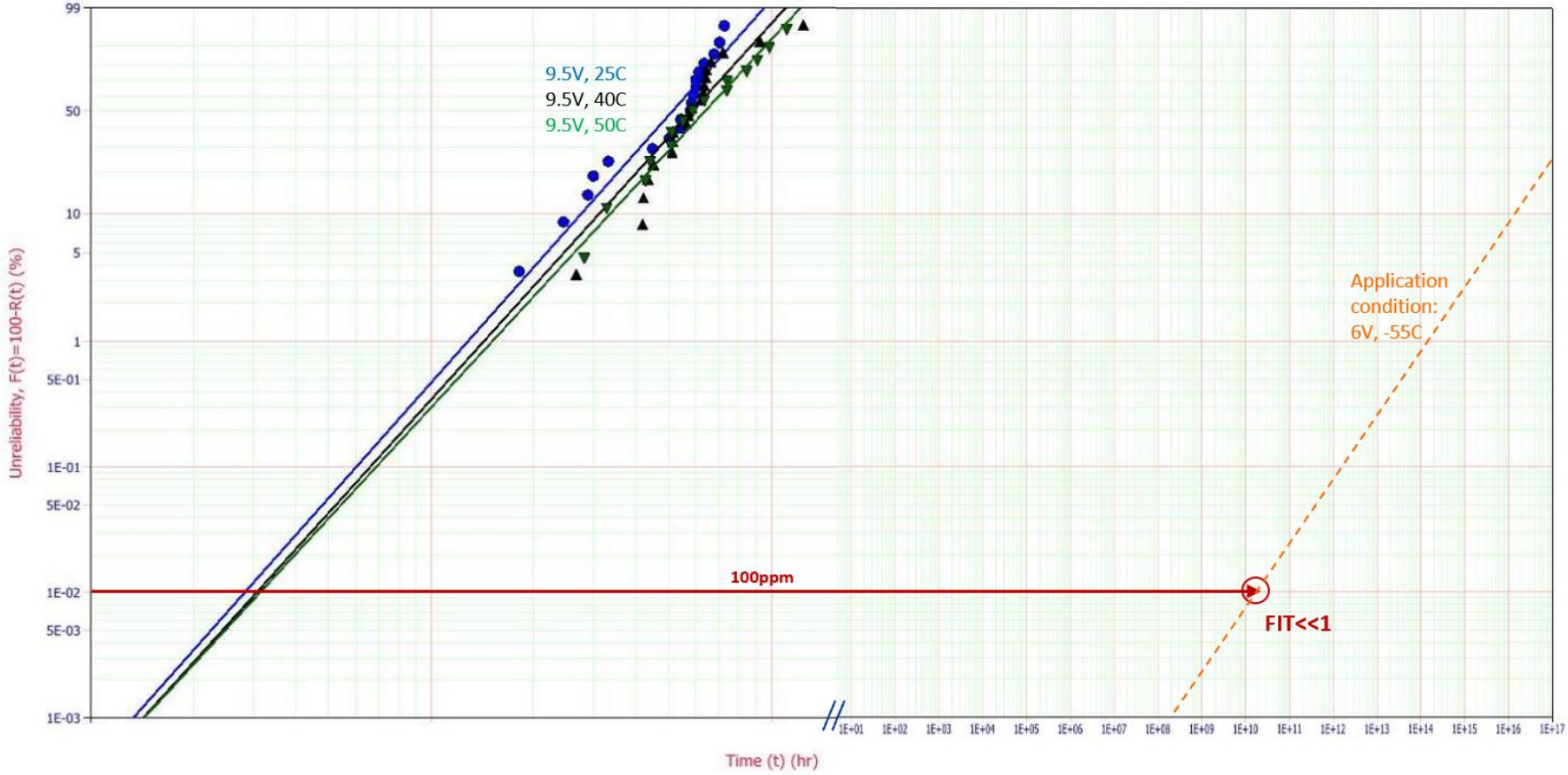
Voltage Acceleration Factor
= AF (V)
$= e^{\beta(Vstress - Vop)}$

Temperature Acceleration Factor
= AF (T)
$= e^{Ea/K(1/Top - 1/Tstress)}$

*AF = AF (V) * AF (T)*

- Acceleration Factors (AF) are calculated by plotting: 1) Voltage data at constant Temperature, and 2) Temperature data at constant Voltage
- AF used to determine Failure in Time (FIT) under operating conditions
- The most conservative model was used for these calculations

Example of TDSB Weibull Plots



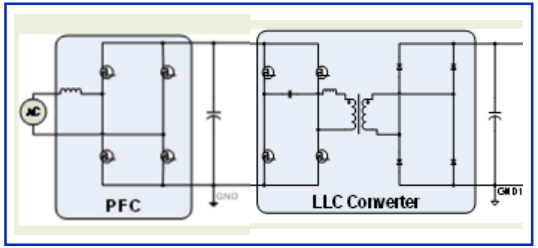
FIT <<1 for gate failure mechanism TDSB

Mission Profile Example – Datacenter

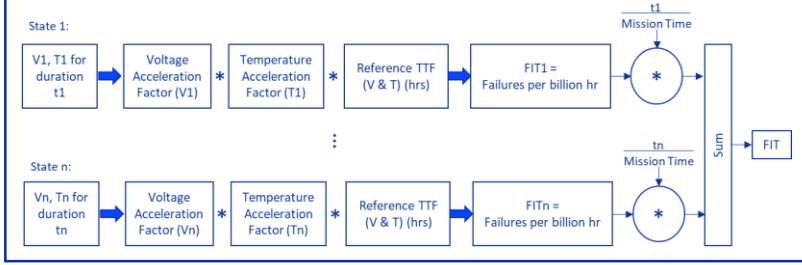
Methodology

1. Accelerated stress test-to-failure of parts
2. Determined acceleration factors
3. Define mission profiles
4. Calculate FIT for each mission profile

Mission Profile States



FIT Calculation



FIT Results

Mission Profile	FIT	MTTF (yr)
Data Center BT-PFC & LLC DC/DC	0.037	3,076,407

FIT is <<1 for charge trapping mechanism

Transistor Technology Benchmarking

GaN, SiC and Silicon transistor comparison

Item	**GaN Systems**	GaN Supplier 1	GaN Supplier 2	SiC Supplier 1*	Silicon Supplier 1	Silicon Supplier 2
JEDEC	☑	☑	☑	☑	☑	☑
AECQ-101	☑	☑	none reported	☑	☑	☑
AECQ-101+	☑	☑	none reported	none reported	none reported	none reported
JC-70	☑	☑	☑	☑	not applicable	not applicable
FIT	<0.1	<1	5	4	<0.1	3

* FETs, not diodes!

- GaN reliability is on the same order of magnitude as Silicon reliability
- Not all GaN is alike, nor is all Silicon alike

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AECQ-101+	☑	☑	none reported	none reported	none reported	none reported
JC-70	☑	☑	☑	☑	not applicable	not applicable
FIT	**<0.1**	**<1**	**5**	4	**<0.1**	**3**

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FIT	**<0.1**	**<1**	**5**	4	**<0.1**	**3**

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- GaN reliability is on the same order of magnitude as Silicon reliability
- **Not all GaN is alike**, **nor is all Silicon alike**

Conclusion – GaN is Reliable

GaN Systems data summary

- ✓ JEDEC and AECQ-101 baseline
- ✓ JEDEC+ and AECQ-101+
- ✓ Solder joint reliability
- ✓ FIT<1

Conclusion

- GaN reliability has been demonstrated
- GaN exhibits higher performance than SiC and many Silicon transistors