# SiC MOSFET Reliability for EV Drivetrain

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Reliability of Wide Bandgap Semiconductors
**Session:** IS23
**Session Location:** R07
**Session Date:** 2020-03-19
**Session Time:** 08:30 - 11:25

Acknowledgments:
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Paper Number 3547

# Outline

- Introduction
  - The device reliability and ruggedness of SiC vertical power MOSFETs parallels that of Si devices, even while experiencing much higher drift fields
- Accelerated High-Field Testing
  - <u>High Gate Field Tests</u>
    - Threshold voltage stability (PBTI/NBTI)
    - Gate oxide breakdown (TDDB/RBD)
  - <u>High Drain Field Tests</u>
    - High-temperature reverse-bias (HTRB)
    - Terrestrial neutron single-event breakdown (SEB)
  - <u>High Power Dissipation events</u>
    - Avalanche ruggedness
    - Short Circuit capability
- Summary

## SiC IN AUTOMOTIVE DRIVETRAIN

# Drivetrain Inverter

CREE Wolfspeed

**What**: Silicon Carbide MOSFETs

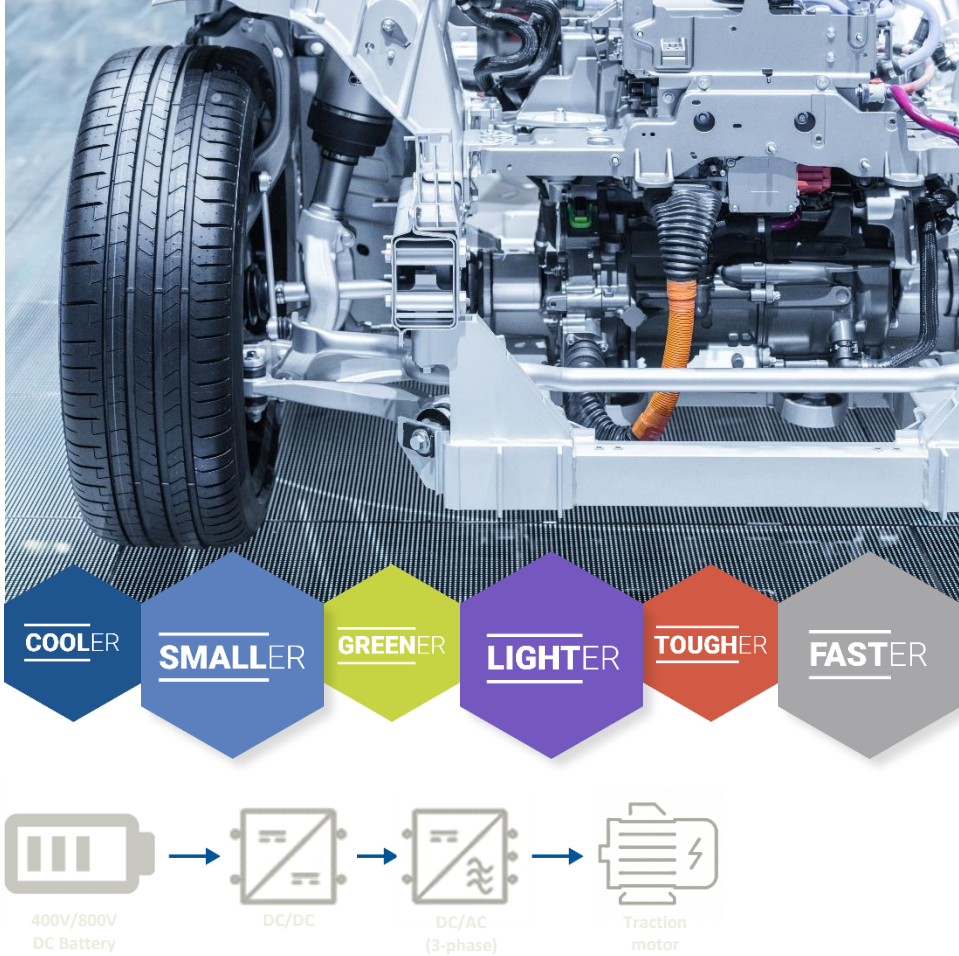
**Where:**

- 90 – 350kW+ EV drivetrain inverter
- Single, dual, or in hub drives

**Why**: Maximize EV range while minimizing overall system and battery cost. Bi-directionality also enables regenerative braking.

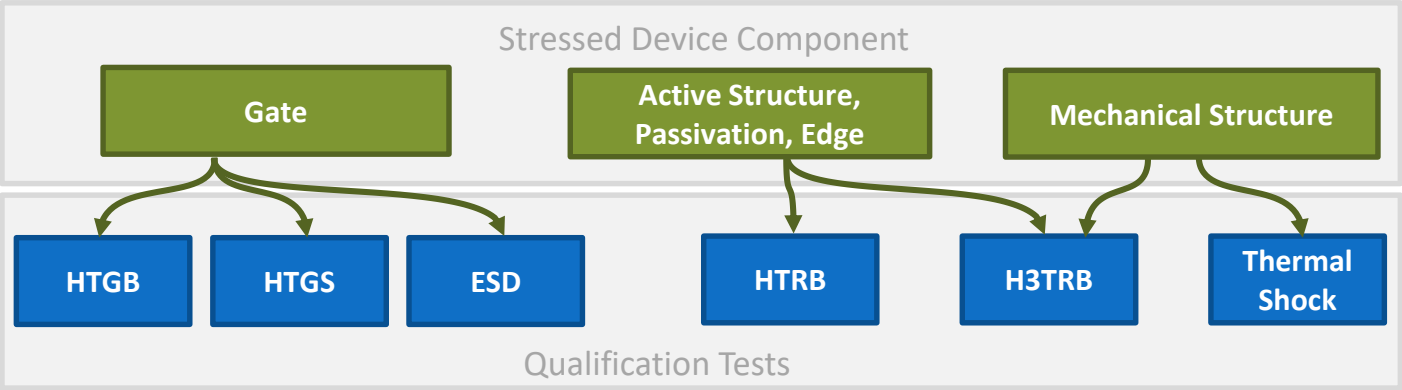
**SiC Advantage**:

- ~80% lower losses
- ~30% smaller size
- Lower system cost



# Overview of SiC Power Device Reliability & Ruggedness

- Wolfspeed Commercial SiC Power Devices are Fully Qualified
- Tested packaged production parts for qualifications
  - 3 lots x 25 parts each stress test: Industrial
  - 3 lots x 77 parts each stress test: Automotive AEC-Q101
- Stresses performed typically at or near rated voltage and temperature for 1000hrs




- HOWEVER, *lifetime prediction* requires taking parts to failure
- Need to use accelerated conditions: field, temperature,…
- Extrapolate to use conditions for lifetime prediction

# ACCELERATED HIGH-FIELD TESTING

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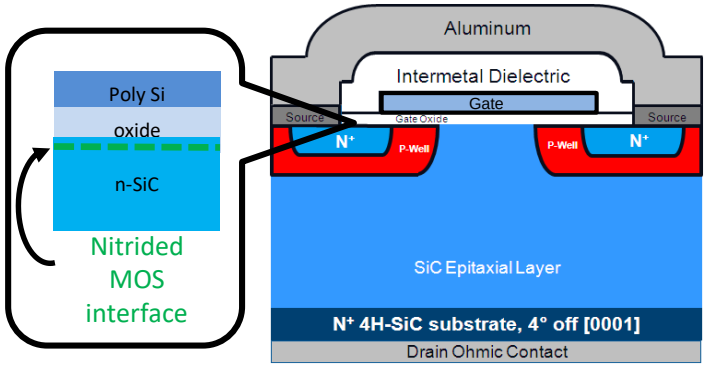
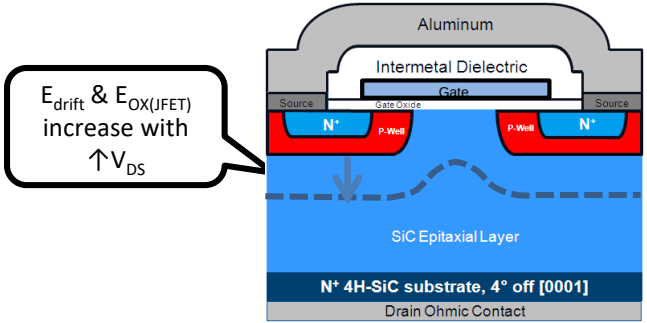
# SiC Power MOSFET Schematic




- **High Gate Oxide Fields ($V_{GS}$)**

1) $V_T$ stability (PBTI/NBTI)
2) Oxide breakdown (TDDB & R-BD)




- **High Drain Fields ($V_{DS}$)**

3) Accelerated HTRB ($V_{rated} < V_{DS} > V_{aval}$)
4) Neutron SEB

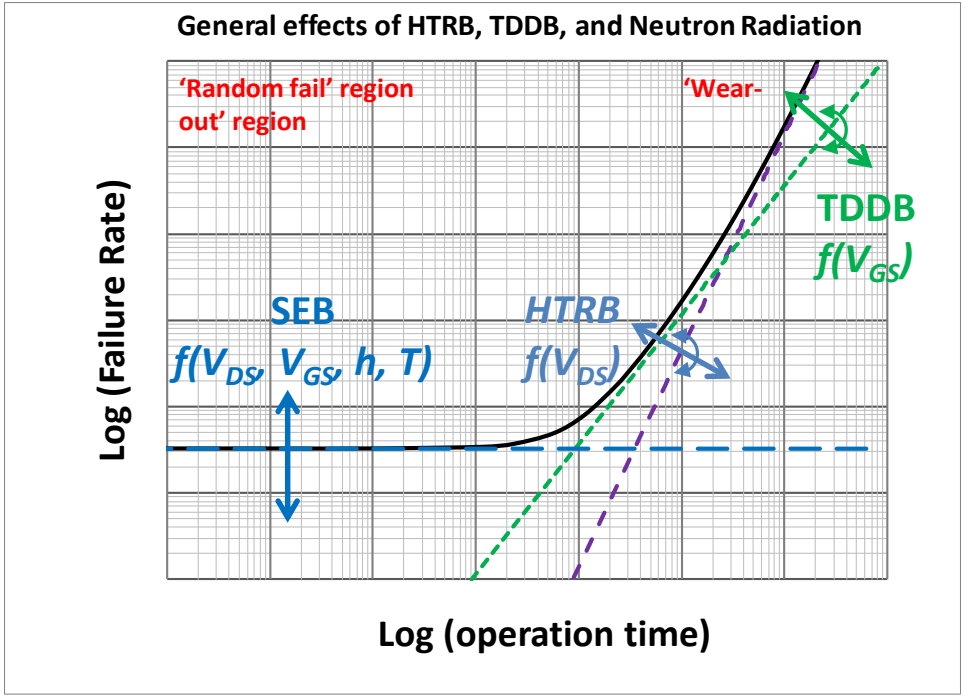
# Device Lifetime schematic: HTRB, TDDB, Neutron SEB

- **Wear-out:**
- **TDDB = $f(V_{GS}, T)$**
- **HTRB = $f(V_{DS}, T)$**

- **Random fail:**
- **Neutron-SEB**

  **= $f(V_{DS}, V_{GS}, h, T)$**

- Device design, oxide quality & oxide thickness affect slopes of HTRB & TDDB lifetime curves

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Positive and Negative Bias Temperature Instability (PBTI, NBTI)

# THRESHOLD VOLTAGE STABILITY

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# Threshold Voltage ($V_T$) Stability

- $V_T$ can shift over time and change the device on-state and/or blocking characteristics

- Threshold shift ($\Delta V_T$) relates to **interface & oxide traps** [1,2]:
  - $\Delta V_T = q*(\Delta N_{ox}+\Delta N_{IT})*[(q*T_{ox})/(K_{ox}*\varepsilon_o)]$

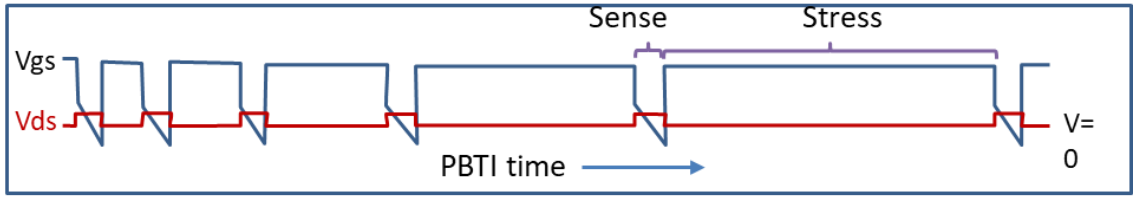
- $\Delta V_T$ of Si MOSFETs depends on the gate **electric field**, **temperature**, and **time** [1,2]:
  - $\Delta V_T = A*\exp(\gamma E_{ox})*\exp(-\mathbf{E_A}/kT)*t^n$

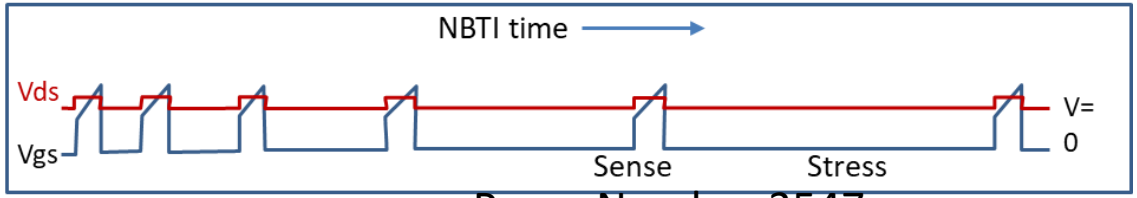
- **SiC has an order of magnitude more interface traps ($N_{IT}$) than Si devices**
- **The nitrided oxide interface may introduce additional effects**


- [1] J.H. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: A review," *Microelectronics Reliability* 46 (2006) pp. 270-286.
- [2] D.K. Schroder, "Negative bias temperature instability: What do we understand?" *Microelectronics Reliability* 44 (2007) pp. 841-852.

# PBTI, NBTI Test Procedure

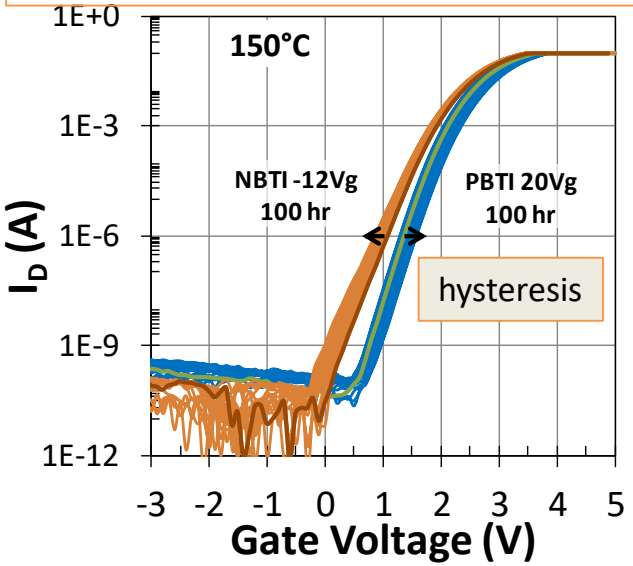
1. Heat sample to test temperature, and hold temperature constant
2. Apply Vgs stress for given time interval, with S = D = 0 V
3. Sweep Vgs from stress V towards Vgs = 0 V, with S = 0 V and D = 0.1 V
    1. Positive stress: sweep down
    2. Negative stress: sweep up
4. Repeat 2) and 3) using logarithmically increasing time intervals at step 2)
5. Extract $V_T$ at a given current level to plot $V_T$ versus time

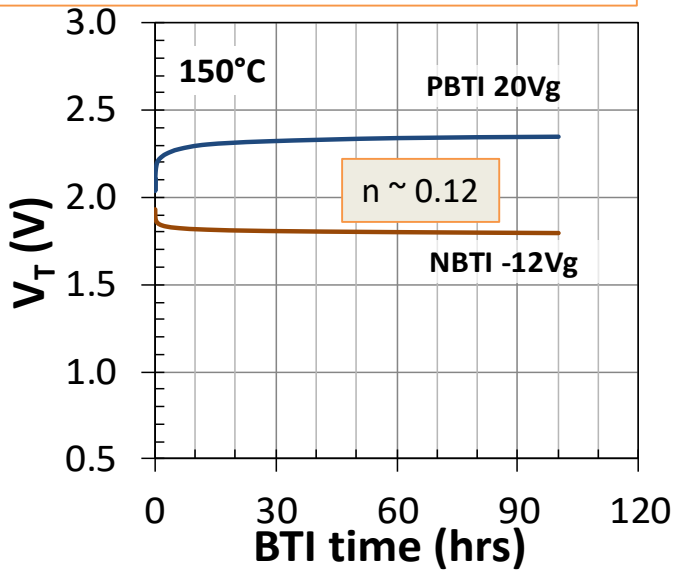


# $V_T$ Stability

Wolfspeed Gen3 1200V 100A SiC MOSFETs (VGSop: +15V/-4V))




- For Wolfspeed devices, $V_T$ drifts only a few hundred mV under constant bias stress
- Weak power law -> $DV_T$ saturates over time
- Drift will be much lower than this in typical switching applications

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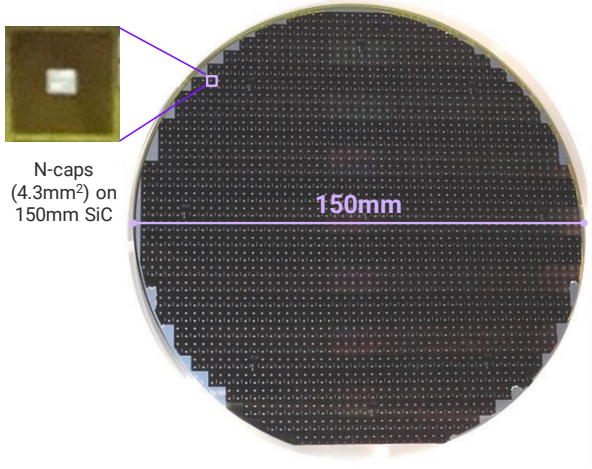
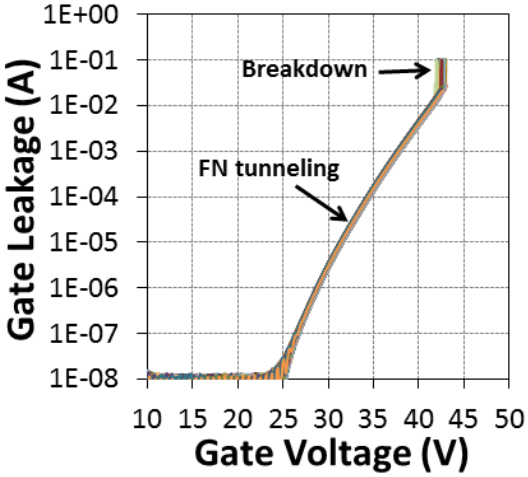
# Ramped Voltage Breakdown

- Constant bias TDDB:
  - Time consuming
  - Limited sample size
- Ramped voltage breakdown:
  - On-wafer
  - Capacitor test structures: reduced processing time
  - Larger sample sizes

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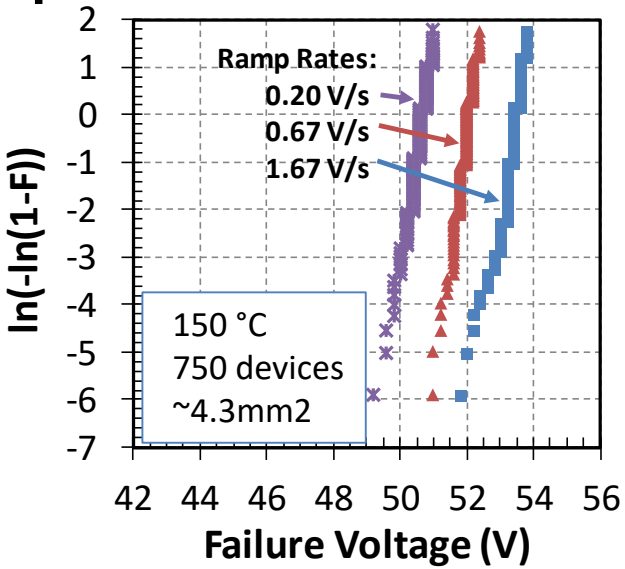
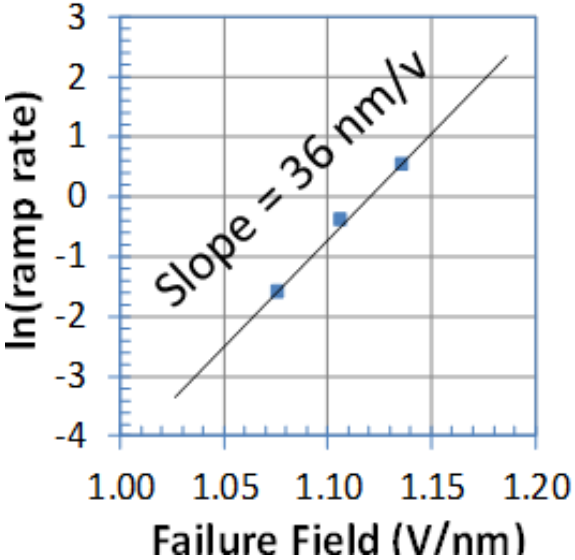
# Ramped Breakdown of Large-Area Ncaps

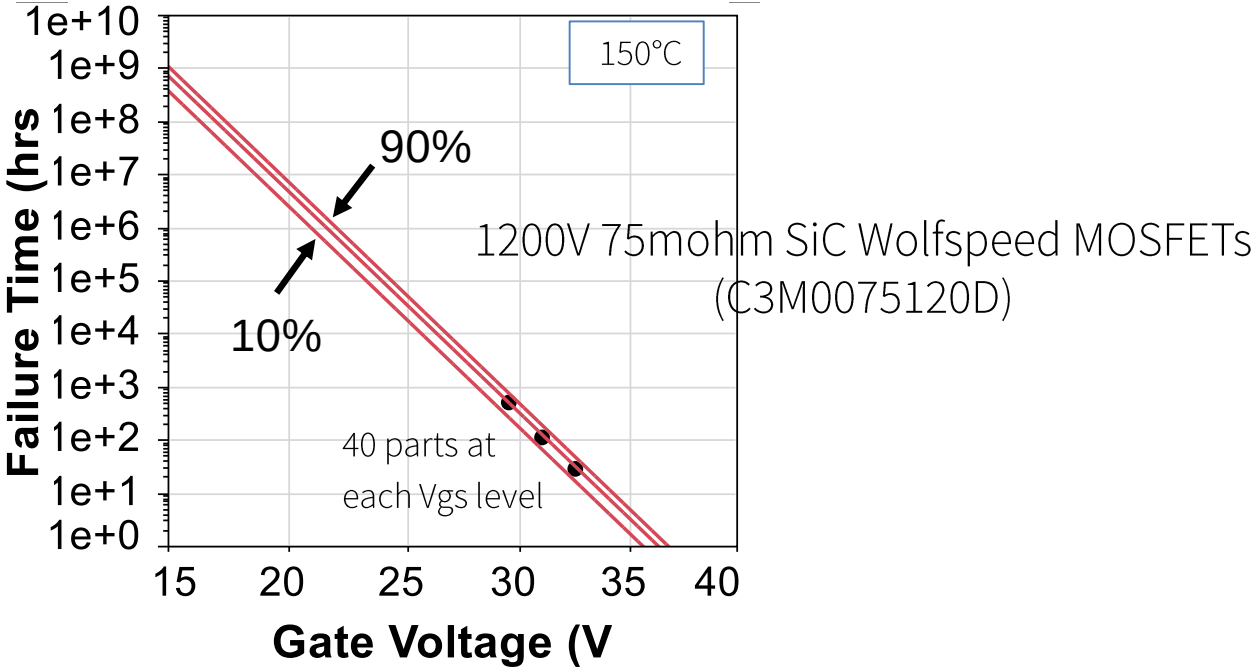



- Good Weibull failure distributions
- **Linear field model** used for lifetime extrapolation: $\tau_{BD} \sim \exp(-\gamma E_{ox})$
- Field acceleration parameter ($\gamma$) ~36 nm/V - consistent with $SiO_2$ on silicon
- Ramped breakdown is a good method for determining extrinsic failure levels


J.S. Suehle, "Ultrathin gate oxide reliability: Physical models, statistics, and characterization," *IEEE Trans. Electron Dev.* 49 (2002) pp. 958-971.
Y-C. Yeo, Q. Lu, and C. Hu, "MOSFET gate oxide reliability: Anode hole injection model & applications," *Inter. J. High Speed Electron. & Systems* 11 (2001) pp. 849-886.
H.C. Cramer, J.D. Oliver, and R.J. Porter, "Lifetime of SiN capacitors determined from ramped and constant voltage testing," *Proc. 2006 CS MANTECH Conf.*, pp. 91-94.

# MOSFET Time-dependent dielectric-breakdown (TDDB)




- TDDB median lifetime @ 15 VGS ~3 x $10^8$ hrs at 150°C
- Lifetime prediction consistent with ramped voltage breakdown prediction

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# ACCELERATED HIGH-FIELD HTRB TESTING

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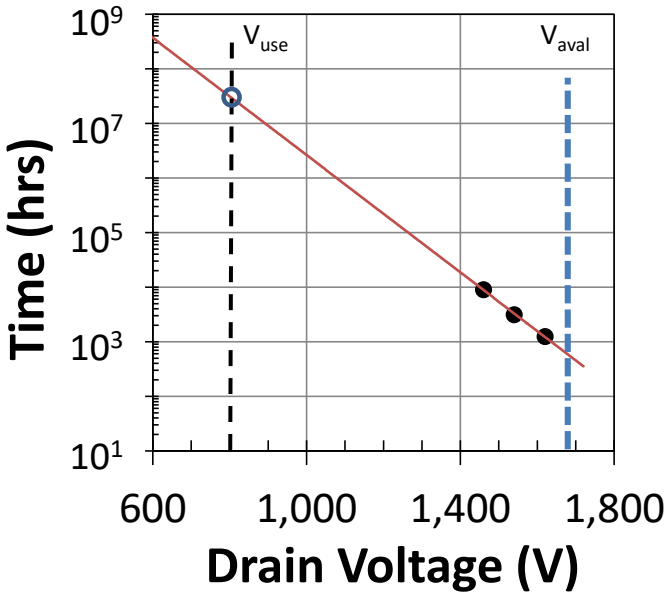
# High-temperature reverse-bias (HTRB) accelerated testing

- **<u>1200V 20A G2 MOSFETs</u>, $V_{GS}$= 0 V (C2M0080120D)**
- **Groups of devices stressed at $V_{DS}$ @ 1460V, 1540V, or 1620V**
- Extrapolation line gives predicted mean failure time at given $V_{DS}$ (each data point is a mean failure time)
- Failure acceleration limited by $V_{aval}$
- **HTRB median lifetime @ 800 $V_{DS}$ ~3x$10^7$ hrs**

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# ACCELERATED HIGH-FIELD TESTING FOR TERRESTRIAL-NEUTRON SINGLE-EVENT BURNOUT

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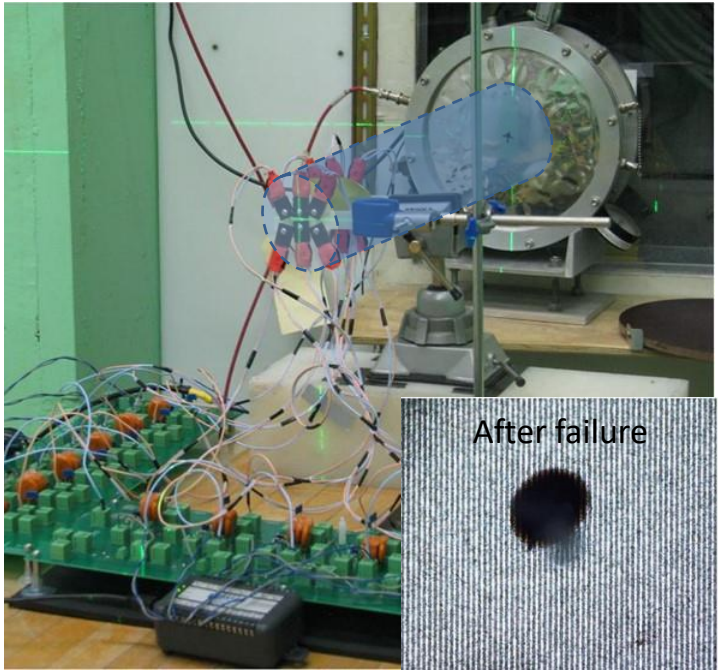
# Single-Event Burnout (SEB) due to terrestrial Neutrons

- **Los Alamos National Lab spallation neutron source:** ~$10^9$ X the sea level flux
- **No lifetime extrapolation required!**
- ***We measure the actual failure rate due to neutron irradiation @ device use fields***
- **FIT = failures per $10^9$ devices*hrs** scaling to sea level n flux

- Modeling: ABB Appl. note 5SYA 2046-03
- $$\mathbf{FIT = C_3 * \exp(C_2/(C_1 - V_{DS}))}$$





- E. Normand, D. L. Oberg, J. L. Wert, J. D. Ness, P. P. Majewski, S. Wender, and A. Gavron, *IEEE Trans. Nucl. Sci.* 41 (1994) pp. 2203-2209.
- H. R. Zeller, *Sol. State Electronics* 38 (1995) pp. 2041-2046.
- J. F. Ziegler, "Terrestrial cosmic rays," *IBM J. Res. Develop.* 40 (1996) pp. 19-39.
- A. Akturk, R. Wilkins, J. McGarrity, and B. Gersey, *IEEE Trans. Nucl. Sci.* 64 (2017) pp. 529-535.
- N. Kaminski, A. Kopta, ABB Application Note 5SYA 2042-04 (2013).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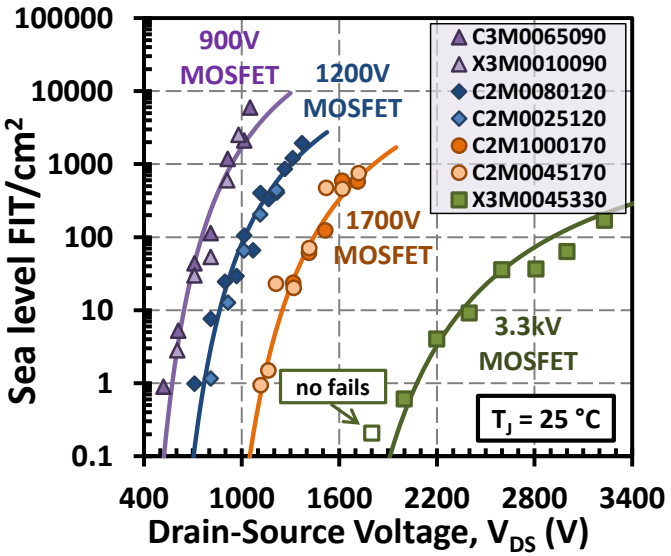
# Wolfspeed SiC MOSFET FIT rates: scaling by active area

- FIT/cm$^2$ vs $V_{DS}$ for different Wolfspeed SiC MOSFET devices:
  - **900V 65 mohm**
  - **900V 10 mohm**
  - **1200V 80 mohm**
  - **1200V 25 mohm**
  - **1700V 1000 mohm**
  - **1700V 45 mohm**
  - **3.3kV 45 mohm**
- Each data point is the mean FIT rate for that sample group



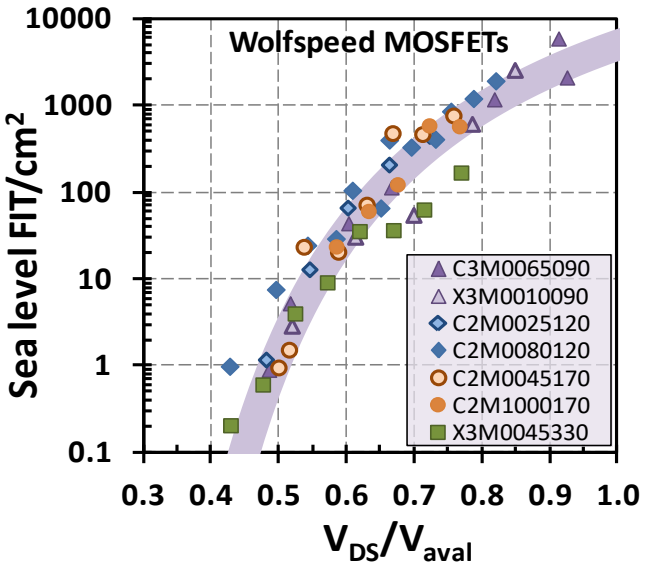

- **Failure rate increases proportionally with device area**
- **Failure rate decreases as voltage rating increases**

D.J. Lichtenwalner et al., *Mat. Sci. Forum*, vol. 924, pp. 559-562 (2018)

# Wolfspeed SiC MOSFET FIT rates: <u>scaling by drift field</u>

- All SiC MOSFET FIT rates scale similarly with **<u>active area</u>** & **<u>drift field</u>** (relative to avalanche)

**<u>Active area</u> & <u>drift design</u> can be tailored to meet application-specific SEB system lifetime requirements**




D.J. Lichtenwalner et al., *Mat. Sci. Forum*, vol. 924, pp. 559-562 (2018)

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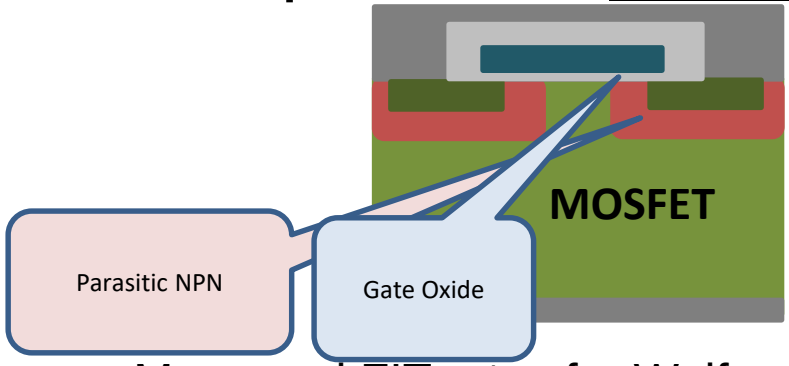
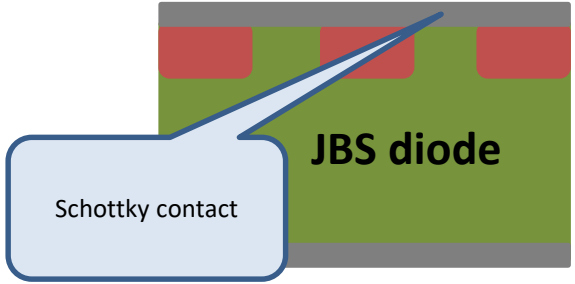
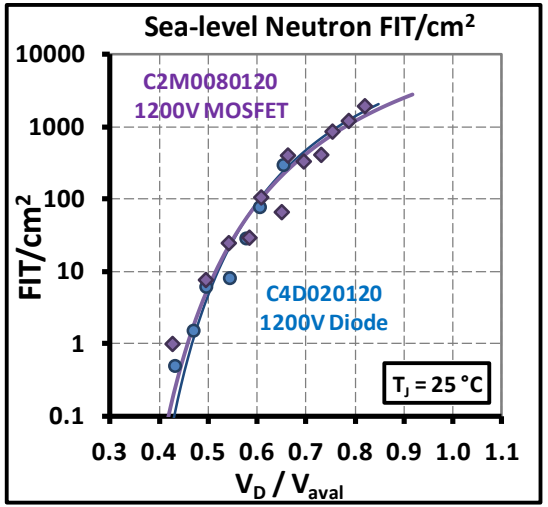
# Wolfspeed SiC MOSFET vs Wolfspeed SiC Diode




- Measured FIT rates for Wolfspeed 1200V 20A MOSFET & 20A Diode under neutron irradiation




- **MOSFETs act like Diodes…**
  - **Active area & drift effects dominate failure characteristics**
  - **No indication of MOSFET parasitic NPN turn-on, or gate-rupture**

D.J. Lichtenwalner et al., *Mat. Sci. Forum*, vol. 924, pp. 559-562 (2018)

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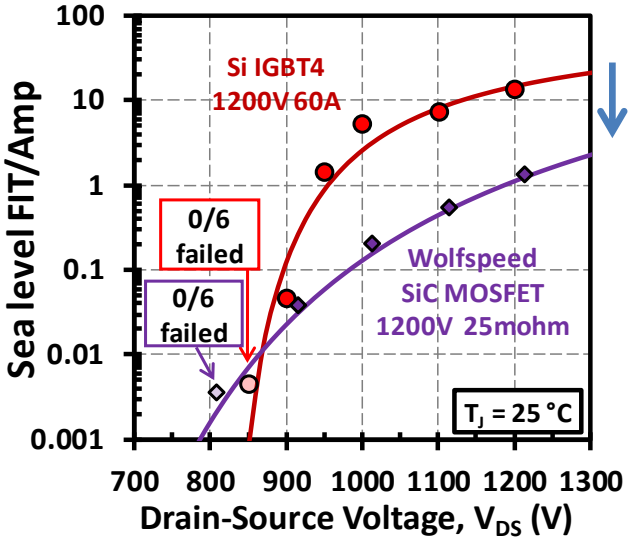
# SiC vs Si: 1200V Wolfspeed MOSFET vs Si IGBT4

- Si IGBTs show sharper failure onset, but higher max failure rate
- **Both the SiC & Si parts may require a $V_{DS}$ derating, but *SiC is more immune to $V_{DS}$ overshoot***




**Si IGBT – IGW60T120-ND**

**SiC MOSFET**

SiC MOSFET has 10X lower FIT rate at high $V_{DS}$

D.J. Lichtenwalner et al., *Mat. Sci. Forum*, vol. 924, pp. 559-562 (2018)

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# UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE RUGGEDNESS TESTING

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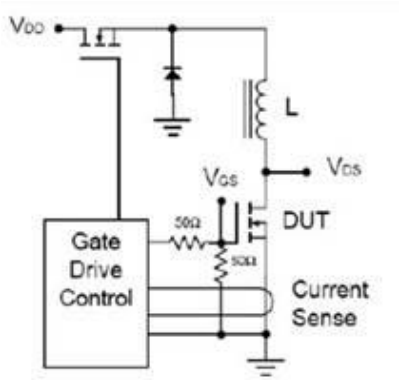
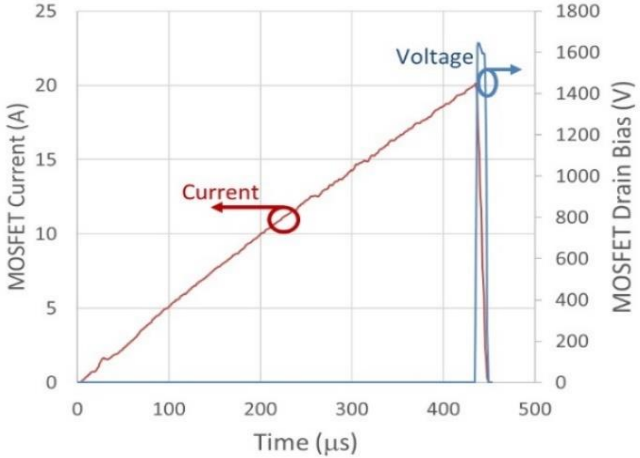
# Unclamped Inductive Switching (UIS) Ruggedness




**Also known as Avalanche Ruggedness (Non-Repetitive)**

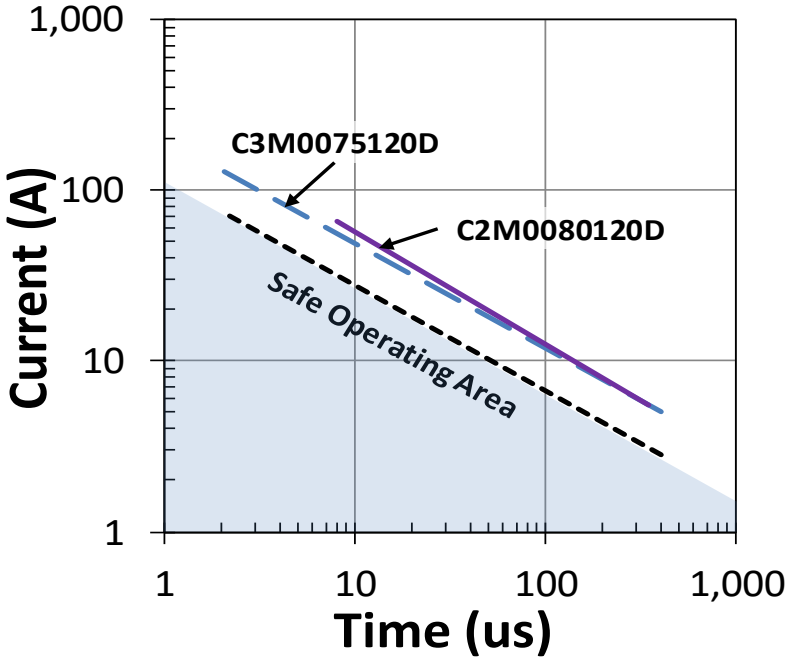
- Turn the MOSFET **on** with a pre-set inductance (L) in series
- Current ramps over time
- Turn the MOSFET **off** when a pre-set current is reached
- MOSFET is forced into avalanche breakdown to dissipate the current that continues to flow through the inductor
  - The inductance is incrementally increased with successive tests until MOSFET failure is observed
  - Statistics are collected over a range of currents to create a SOA curve of Avalanche Current vs. Time in Avalanche

Paper Number 3547

# UIS Comparison of Cree Gen 2 and Gen 3 MOSFETs

- The safe operating area (SOA) is defined from a statistical margin of safety applied to the typical last surviving test

Gen 3 MOSFETs match the UIS Ruggedness of Gen 2 MOSFETs, despite the smaller chip size

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# Avalanche SOA: Silicon versus SiC devices

- **SiC devices (Gen2 1200V 160mohm SiC MOSFETs) behave in general similarly to Si MOSFETs, with an avalanche ruggedness SOA as below**
- Lateral devices (such as GaN) typically cannot survive a single high $V_{DS}$ event, as the structure does not support sustained semiconductor avalanche breakdown

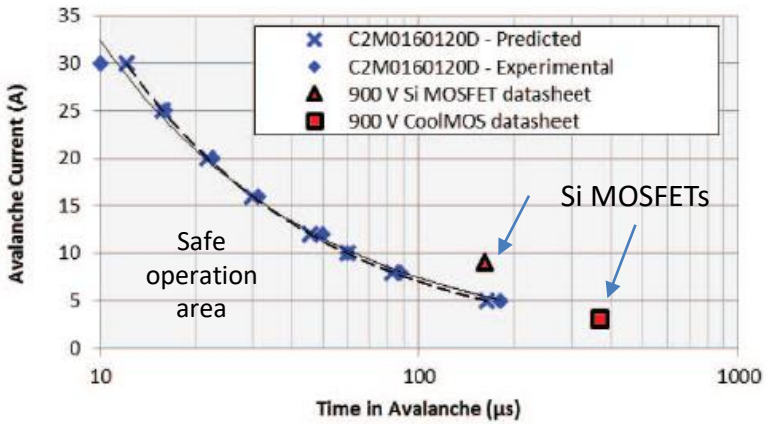


Fig. 5. Predicted (dashed) and experimental (solid) avalanche current versus time in avalanche curves for the C2M0160120D SiC MOSFET. The datasheet avalanche ratings for a 900 V, 18 A (at 25 °C) Si MOSFET [16], and a 900 V, 9.5 A (at 100 °C) CoolMOS [17] are also plotted.

C. DiMarino & B. Hull, IEEE ISPSD (2015) pp. 263-267.

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# Summary

- Wolfspeed SiC diodes & MOSFETs are qualified under JEDEC standards, and some device families are also automotive (AEC) qualified

- **Accelerated testing reveals:**
- **Long predicted lifetime in standard use conditions for:**
  - MOS threshold stability ($V_T$)
  - Oxide lifetime in TDDB
  - Accelerated HTRB measurements

- Neutron SEB failure in SiC devices is **sufficiently low for reliable device operation.** Failure scales by the drift field & the active area.

- SiC MOSFETs have a demonstrated avalanche safe operating area (SOA)

# Questions?

**APEC 15-19 Mar. 2020**
**New Orleans, LA (USA)**
**Industry Session:**
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