Selected Topics on Power GaN and SiC Device Reliability

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Outline

1. Introduction
2. Qualification methodology for wide bandgap
3. Selected topics on power GaN reliability
4. Selected topics on power SiC reliability
5. Wide bandgap standards
6. Conclusions

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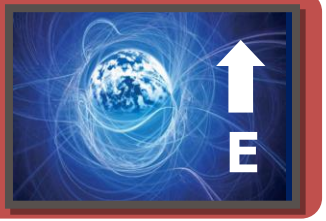
Mega social trends

Mega Cities and

Increased Population



CO_2 Emission

Automotive Electrification

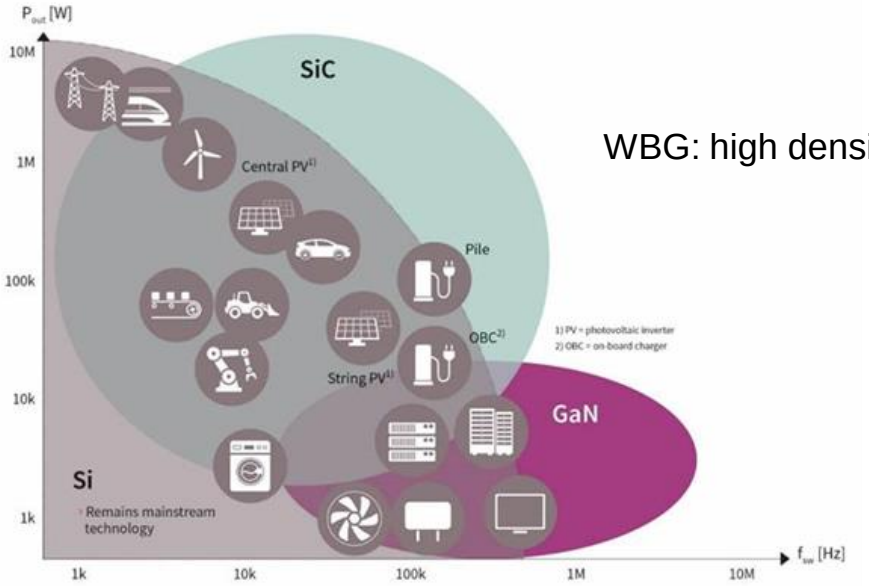
Security in Communiction

Efficient Power Processing

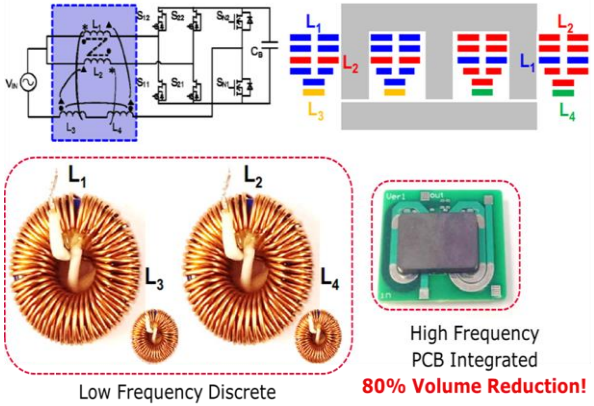
High Density Solutions

CoolSiC™
CoolGaN™

Co-existence is expected between the three main material systems: Silicon, SiC and GaN



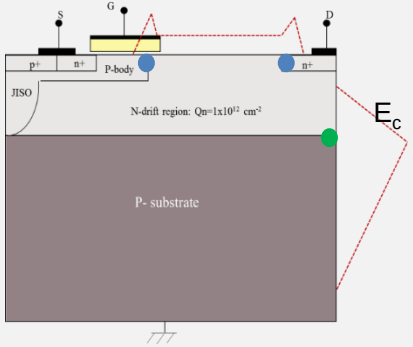
WBG: high density, high efficiency



- Integration of the magnetics will result in reduced size, weight and simplify manufacturing process
- **Balance-of-system** cost reduction

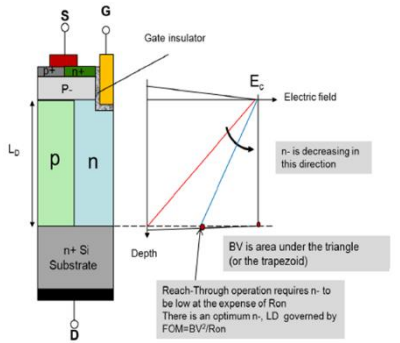
Ability to offer Si, SiC and GaN ensures impartial value proposition offering to the customer

Design of power devices – optimizing the drift region for low losses and smart electric field distribution



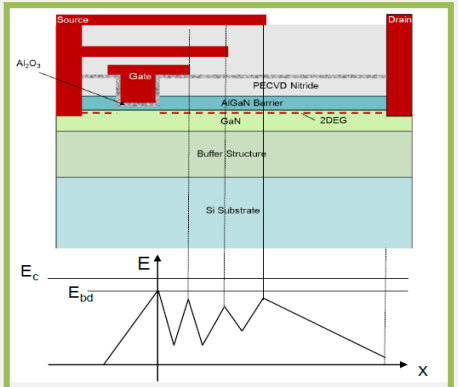
RESURF Concept

- Double peak E_field at the surface & triangle in the bulk
- Breakdown via avalanche (non destructive)
- Charge ~ $1x10^{12}cm^{-2}$
- **E_{Crit} =0.3 MV/cm**



Charge Compensation Concept

- Near flat electric field
- Breakdown via avalanche (non destructive)
- Charge ~$2x10^{12}cm^{-2}$ in the pillars for Si and potentially $2x10^{13}cm^{-2}$ for SiC
- **E_{Crit} =0.3 MV/cm for Si**
- **E_{Crit} =3 MV/cm for SiC**



HEMT Concept

- Saw tooth distribution of field
- Moderated by field plate
- Destructive Breakdown
- Over design to account for Time-dependent dielectric like Breakdown
- **E_{Crit} =3 MV/cm**

Breakdown voltage is reached when the electric field peak reaches the critical electric field E_{crit} of a material .

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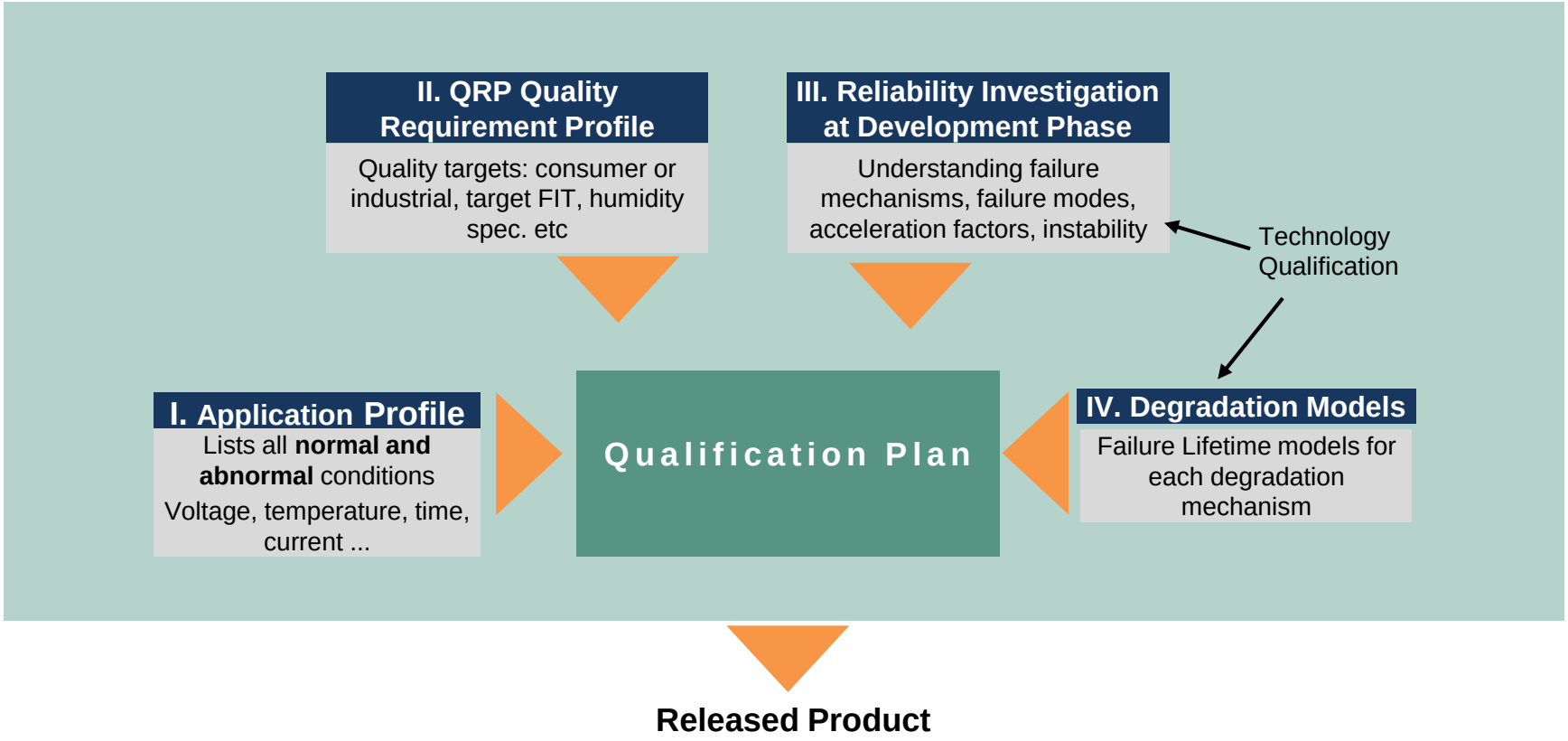
The 4 main ingredients for WBG qualification involving technology & Product qualification



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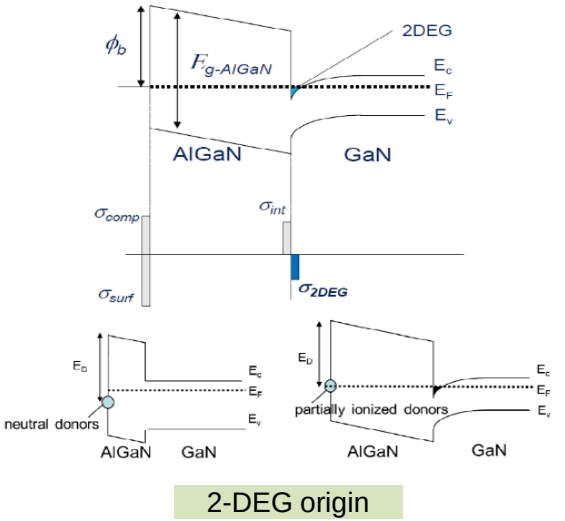
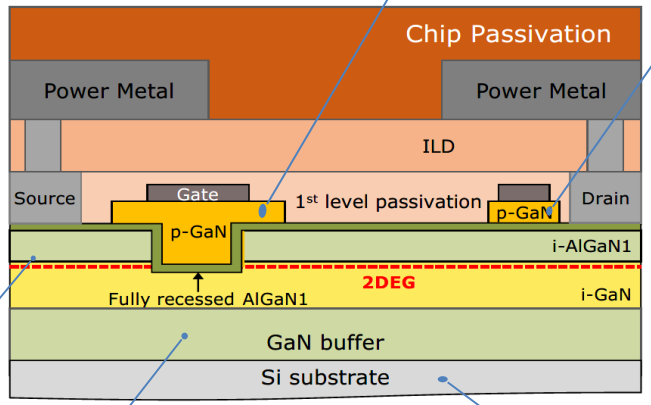
Lateral e-mode GaN device structure (GIT) – major structural elements



2-DEG origin

Ohmic PGaN Gate: to deplete 2DEG below gate for Normally off operation



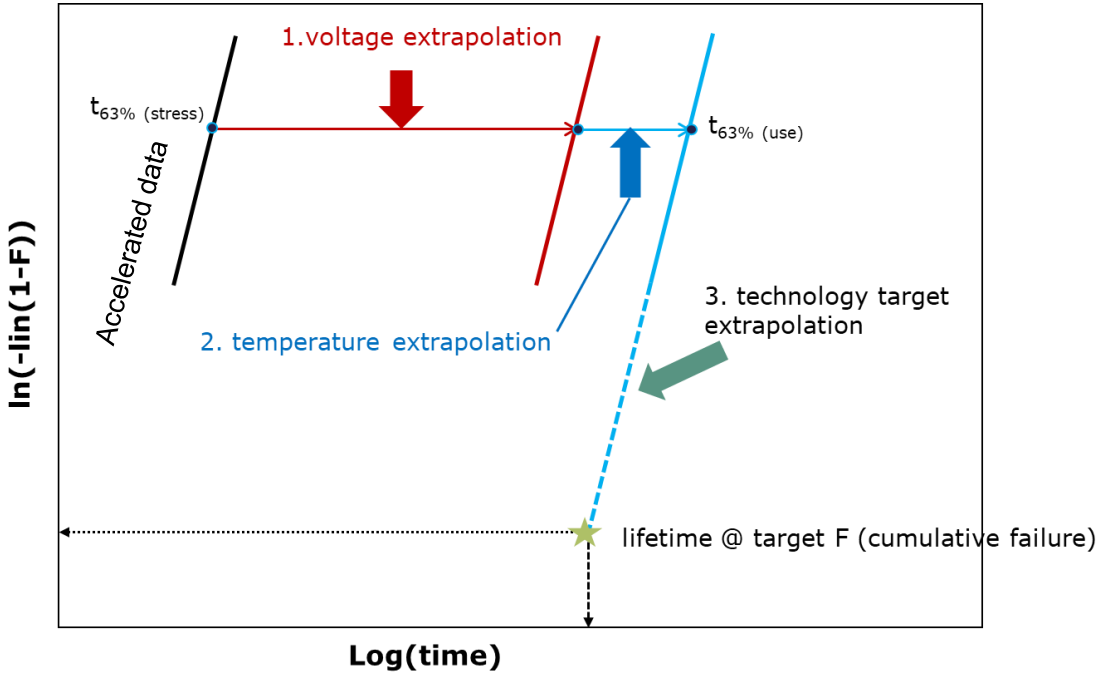
P-GaN layer: hole injection promotes de-trapping of electrons during off-state and hard switching

Heterojunction: high 2DEG density and high mobility for low R_{on}

Buffer layer: highly resistive, high vertical breakdown voltage with minimum trap density. Has to address mismatch in lattice constant and thermal expansion coefficient between GaN and Silicon and ensure minimal stress in the GaN Epi stack (simplified view)

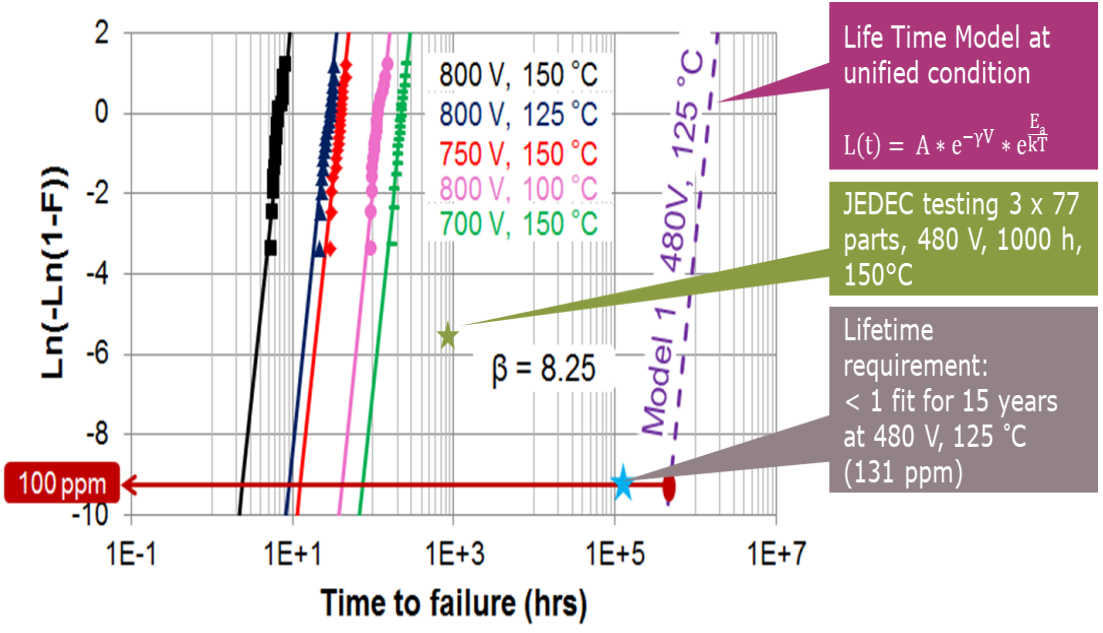
Si Substrate: cost effective, potential monolithic integration with Si ICs and leverage economies of scale of Si technology

Accelerated lifetime testing and extrapolation – principle of accelerated testing



Key factor for a reliable extrapolation is verified knowledge about acceleration factors (for bias and temperature e.g.)

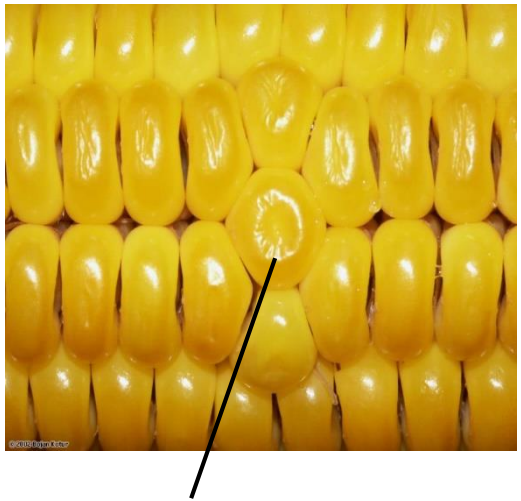
Lifetime parameter extraction and extrapolation to use conditions (example TDDB like evaluation for GaN)



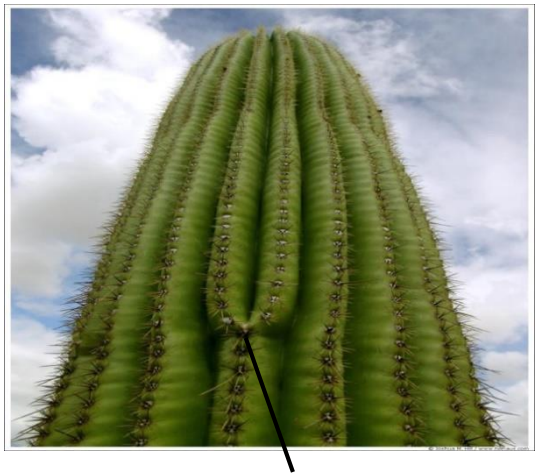
- The acceleration model is developed for voltage and temperature
- The predicted lifetime is **~55 years** at 100 ppm, (480 V and 125 ° C) which clearly exceeds the target for telecom rectifiers of 15 years
- **> 3X safety margin from Infineon's criteria**

Drift of essential device parameters – role and origin of traps

- A trap is a defect originating from a structural defect or the presence of an impurity or a sudden loss of continuity in the crystal lattice (as in interfaces)
- A defect disrupts the periodicity of the crystal lattice and introduces an energy level within the bandgap (undesirable)



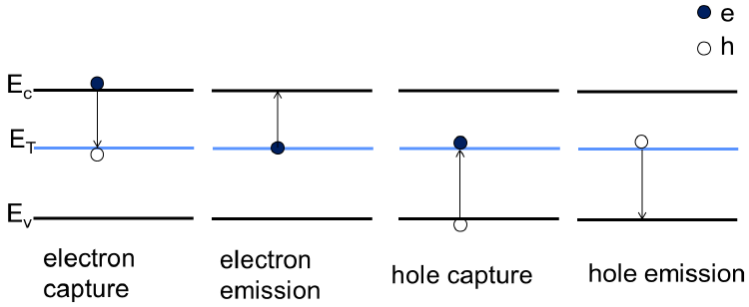
Self-interstitial in the corncob



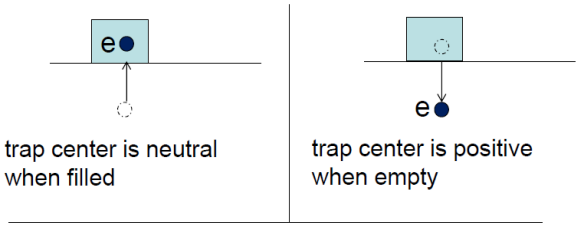
Stacking fault in the saguaro cactus

[Credit of illustration idea to D. Schroder, Semiconductor Material and Device Characterization, third edition: John Wiley & Sons, Inc., Publication, 2006]

Charge trapping



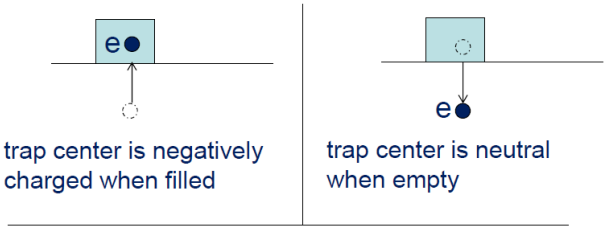
Donor-like trap



Capture: trap center becomes more negative

Emission: trap center becomes more positive

Acceptor-like trap

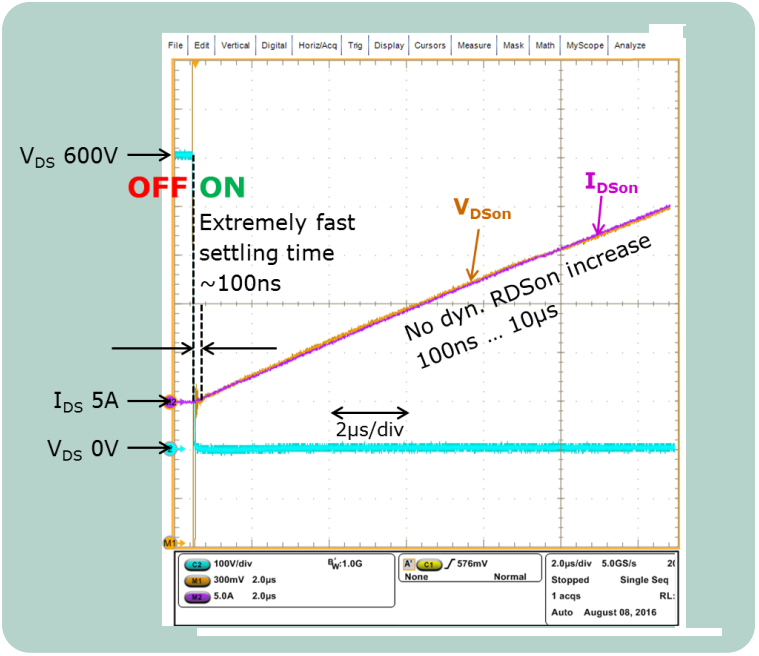


Capture: trap center becomes more negative

Emission: trap center becomes more positive

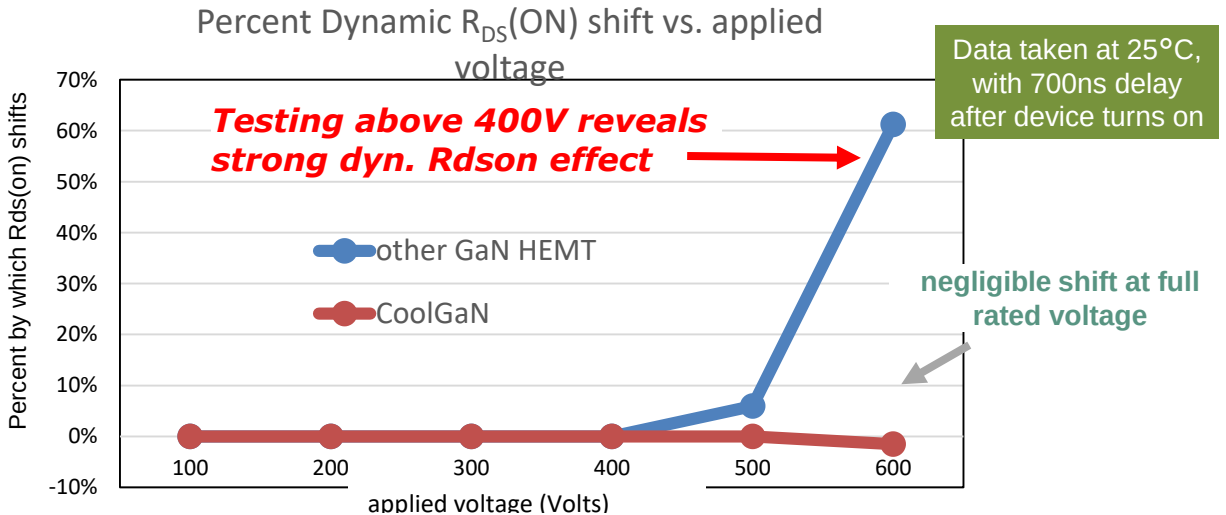
A typical trap related effect in GaN HEMTs is the so called dynamic R_{dson}: How to test?

- Charge trapping changes the effective Rdson ➔ e.g. 40% dynamic R_{DSon} turns a 35mΩ device into a 50mΩ one, characterization essential
- As implicated by it‘s name dynamic R_{DSon} testing is strongly dependent on timing as the **charge trapping** relaxes with time
- Typically measured data for dynamic R_{DSon} are stated at **2.5µs** after turn-on for **400V**
  - For hundreds of kHz up to MHz switching this is not enough
- CoolGaN™ has been characterized down to **100ns** for at V_{dsmax} **600V** with **no R_{DSon} increase**
- We have 100% of all shipped parts tested with 600V / 700ns
- Test now adopted by JEDEC



Dynamic R_{dson} 600V CoolGaN™ technology reliability - application level test example

Dyn. R_{ds}ON measured real time during hard switching! At full rate



True application measurements taken a few hundreds ns after hard switching device turn on! Still no impacts on datasheet!

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SiC module qualification summary – standard tests complemented by mission profile based procedures

Test	Chips in Test	Test conditions	stress time – for product release	Robustness validation
HTRB	72	V_{DS}=1080V, T=150°C	1000h	+4000h
HTGS	72	V_{DS}=0V, V_{GS}=+20/-20V, T=150°C	1000h	+4000h
H3TRB	72	V_{DS}=80V, T=85°C, rH=85%	1000h	+2000h
HV-H3TRB ★	72 (std.) 700 (RV)	V_{DS}=960V, T=85°C, rH=85%	1000h	1000h +2000h
PCsec	72	$T_{vj,max}$=150°C, ΔT=80K	25.000c (until EoL)	
PHV-H3TRB ★	72	V_{DC}=750V, V_{peak}=950V, T=85°C, rH=85%		1000h
AC HTC ★	24	T_{cycle} = -20 °C / 85 °C; rH = 93% V_{DS} = 400V / 800 V (AC); f = 16.000 Hz t_{on} = 430 min; t_{off} = 170 min	21d (only SiC)	120d
PC		$T_{vj,max}$=150°C, ΔT=80K ton=0.5s // 1.5s // 15s // 60s		EoL to define t_{on} dependence
TST	72	T=-40°C – 125°C	50c	

- Tests extended beyond standardized test time
  - Tests continue to run, to be updated
- Currently no EOL visible (occasional peculiarities, but predominantly not chip related resp. still better than observed with state of the art IGBT technology
- Special application oriented moisture tests added
  - AC-HTC – special outdoor test
  - HV-H3TRB
  - PHV-H3TRB

Why do we need to define new tests – example AC-HTC and HV/PHV-H3TRB

HV/PHV-H3TRB

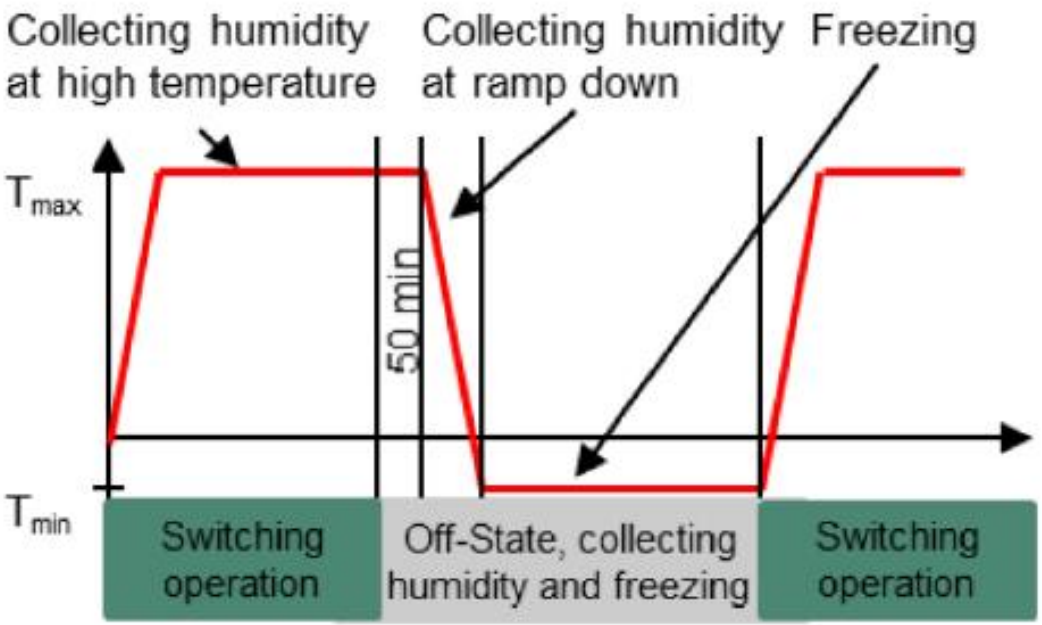
- Traditional moisture test does not reflect real stress in the device ➔ 80V bias for a 1200V device creates just a very small electric field
- Increase of applied voltage and pulse pattern emulate real stress much better and can trigger more failure modes which are not seen with traditional H3TRB, but in the real operating environment

AC-HTC

- Solar systems are often located outdoor
  - In winter time and during night system is off – significant amount of moisture enters the system by bedewing
  - If moisture reaches semiconductor surface combined with electric fields anodic oxidation can destroy the chip
- Technological measures developed to counteract moisture penetration
- Qualification process developed to verify effectiveness
  - Rolled out to all outdoor relevant products

Verification test for moisture resistance in solar - AC-HTC test

Basic test concept*



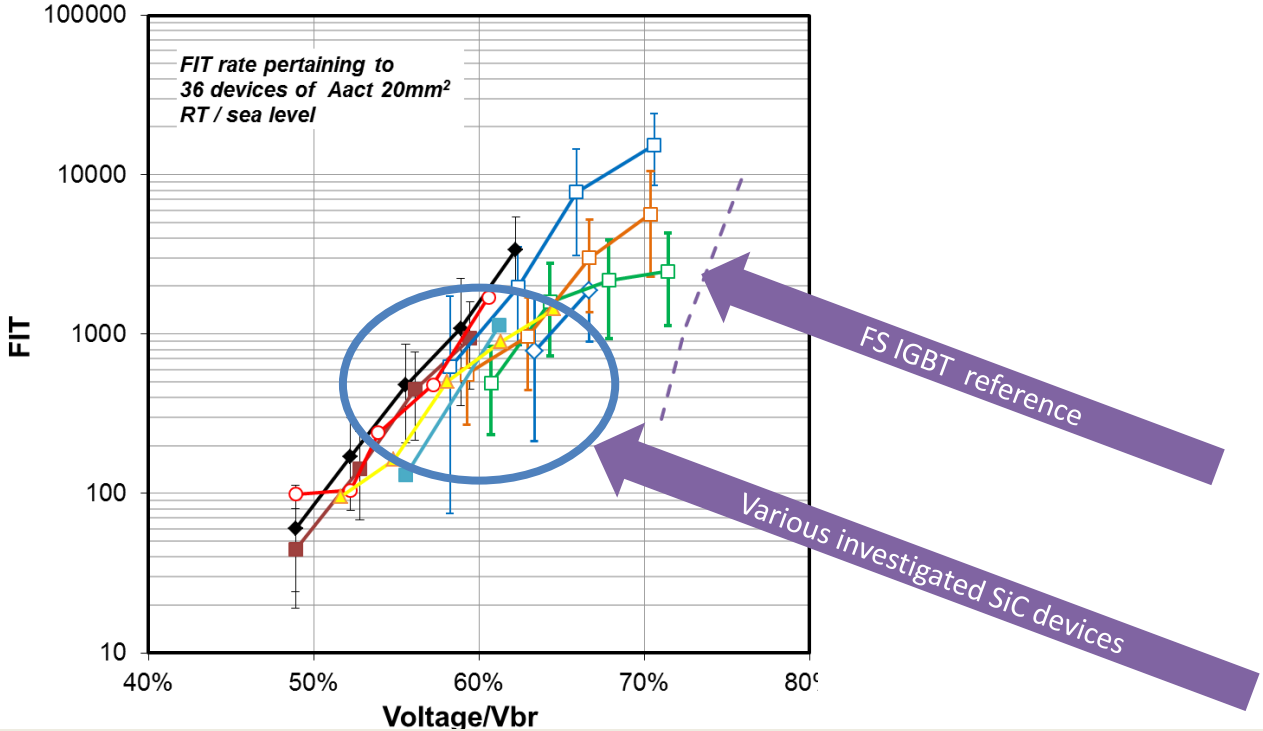
*N. Kaminski, “Reliability Challenges for SiC Power Devices in Systems and the Impact on Reliability Testing”, Materials Science Forum 2018, Vol.924. pp. 805-810.

Weak devices usually detected already after a few cycles, test duration currently >100d

Cosmic ray and SiC

- **General understanding of cosmic ray :**
  - Effect (FIT rates) heavily dependent on the actual electric field in the device ➔ typical de-rating via reduced U_{DS} in the application
  - Case of SiC : about 10x higher internal fields as major benefit ➔ what kind of influence has this on the cosmic ray behavior ?
- **Findings :**
  - Despite the 10x higher electric fields SiC components come close to silicon performance
  - Current status of investigations shows that de-rating efficiency is not as good as in silicon due to flatter dependence of FIT on U_{max} in the application
- **Benefit of unipolar MOSFET :**
  - Adaption of maximum field with much smaller penalty on performance compared to IGBT

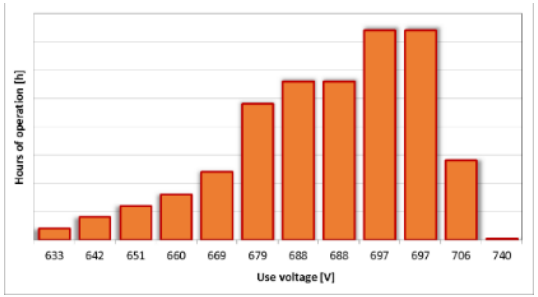
FIT rate vs. U_{DS} related to ACTUAL breakdown voltage (not U_{DS_max} from datasheet)

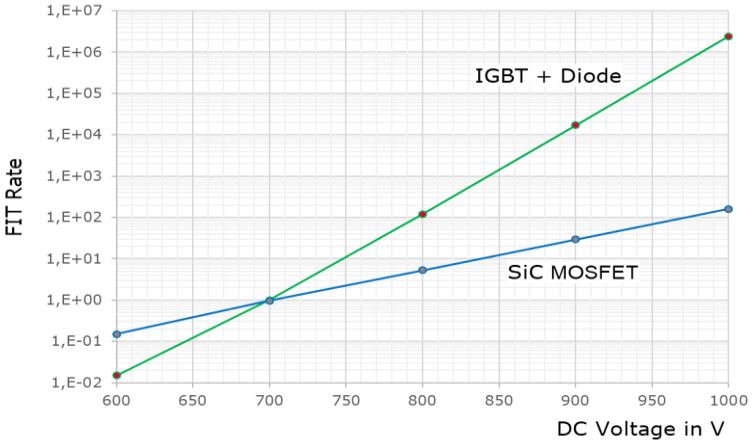


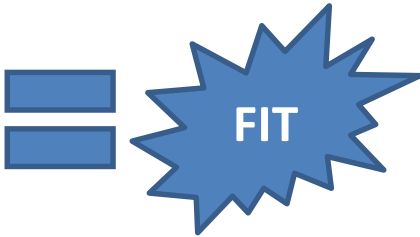
FIT rate depends on electric field, flat slope compared to IGBT observed for the current state of the art

Cosmic ray and SiC

- Similar to the procedure in Silicon the device supplier can model cosmic ray fit rates based on experimental results
- With a mission profile given by the customer the FIT rate in a real application can be estimated

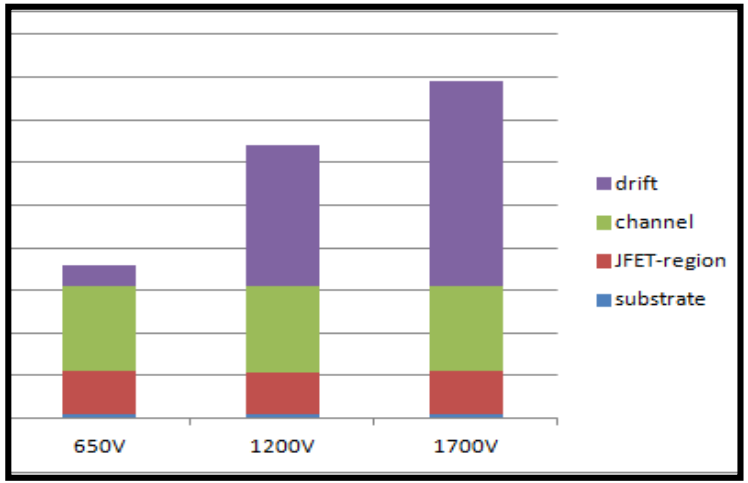






- Benefit of SiC vs. IGBT :
  - The SiC MOSFET has a smaller active area than the Si IGBT/Diode for the same current.
  - The SiC MOSFET does not need a free wheeling diode, which also contributes to CR FIT.
  - Note Si FIT rate reduces much more with increasing T_j than a SiC MOSFET

Effect of electric field adaption on the expected performance



- Adaption of electric field in order to meet FIT requirements is realized via the **drift zone design**
- Drift zone in SiC MOSFETs has a less significant contribution to R_{on} compared to silicon

- Conclusion :
  - Adaption of electric field in order to meet FIT rates with less impact on performance than in silicon
  - Mainly dynamic losses nearly not influenced at all

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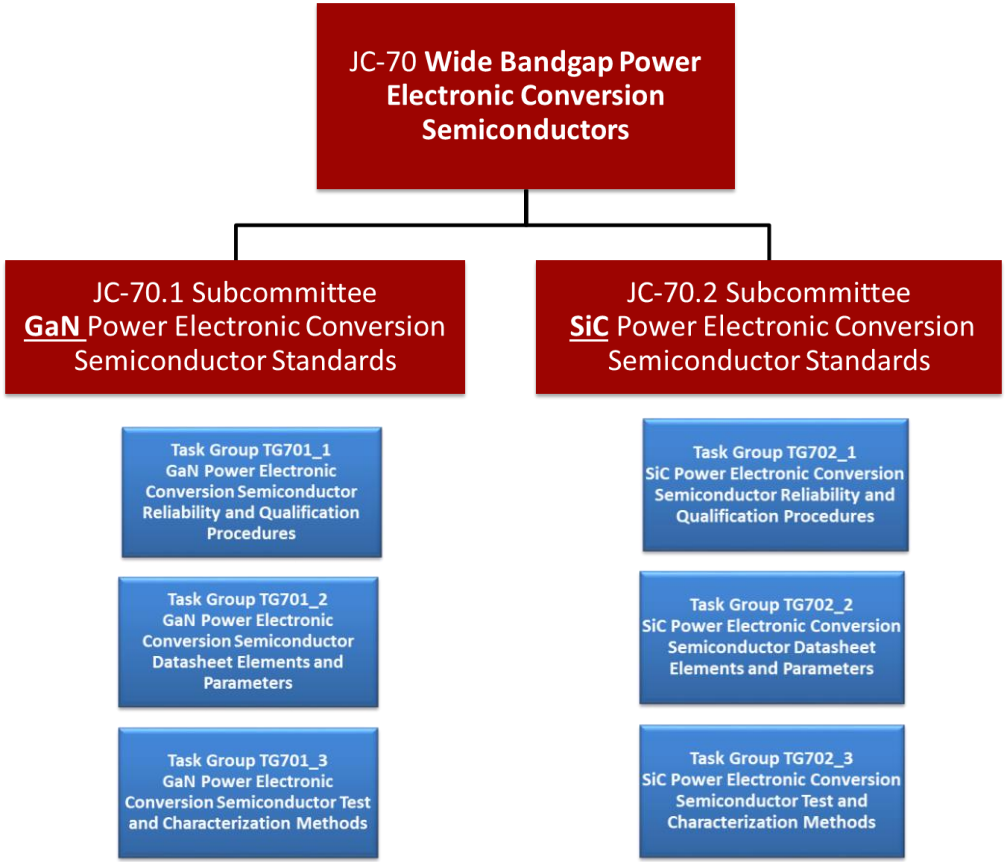
Wide bandgap standards JC-70

- **Motivation**: Establishing Wide Bandgap Standards (initially guidelines) is perceived as means to accelerate WBG customer acceptance and therefore is an accelerant to market penetration
- By **harmonizing** tests, datasheet requirements, reliability and qualification methods across the industry, the customer is assured of the test conditions and procedures thus removing ambiguity and uncertainty in the methodology and the data
- Significant support by Infineon was provided through the early incubation of GaN Standards for Power Electronic Conversion (GaNSPEC) and continued through the transition to JC-70



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- Four ingredient methodology starting from product mission profile and involving rigorous technology and product reliability evaluation was presented.
- Performing accelerated life tests and modeling of the key failures are key to assure both the manufacturer and the customer of product quality including predicting FIT rate at use conditions.
- Key reliability topics in focus were highlighted for both GaN and SiC Power devices.
- An industry-wide effort to generate Standards (initially Guidelines) is supported by industry to accelerate adoption – also a clear evidence of the ongoing maturity of WBG technologies.