Extreme Reliability and Test-to-Fail Methodology for GaN Devices

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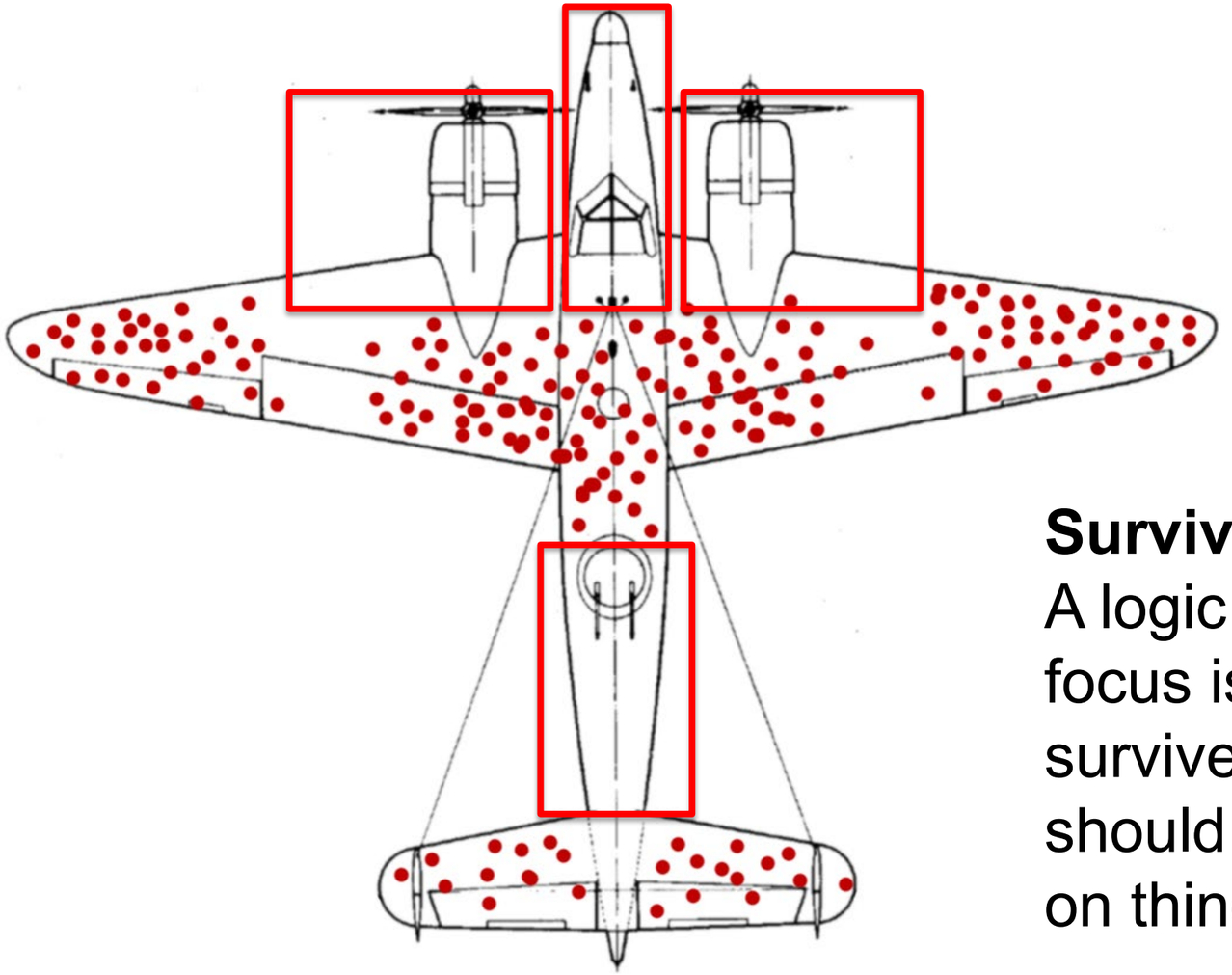
Survivor Bias



Areas that should be reinforced

Survivor Bias:
A logic error where the focus is on things that survived…when focus should really have been on things that did not.

Die and Package Stress Tests

- EPC has broken down the various stressors and the various tests we use to express the failure mechanisms.
- From an understanding of root cause we can generate models that predict failure rates under different conditions.

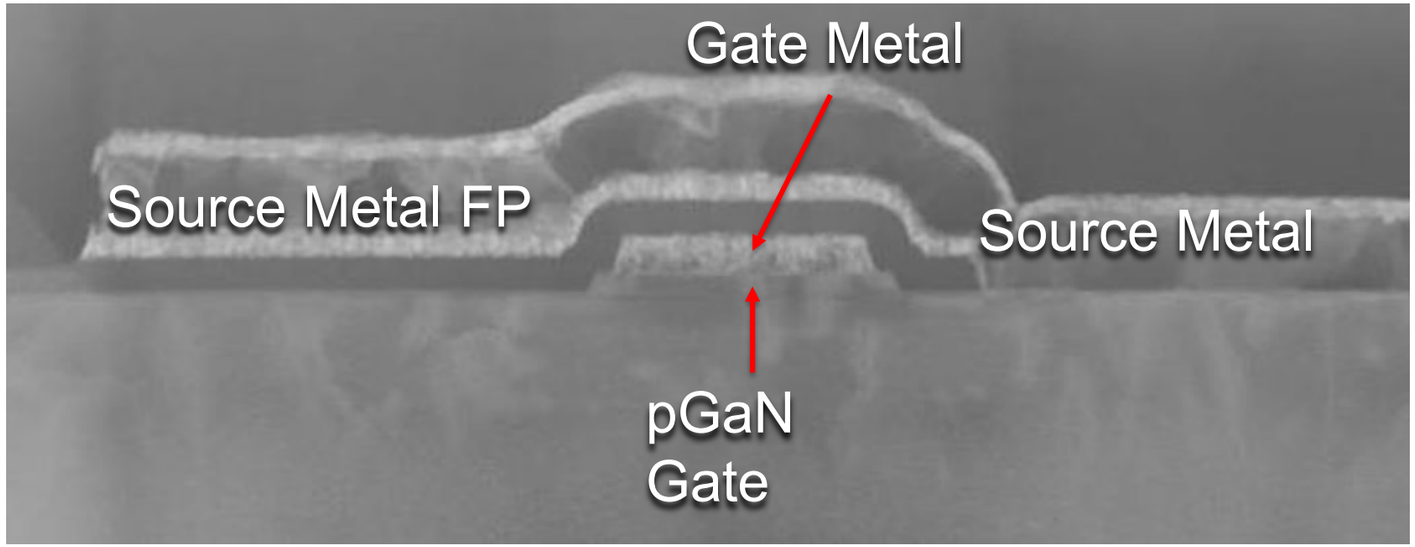
Stressor	Device/ Package	Method	Intrinsic Failure Mechanism	Evidence
Voltage	Gate-Source	HTGB	Dielectric failure (TDDB)	Gate-Source Leakage
			Threshold shift	Gate-Source Threshold
	Drain-Source	HTRB	$R_{DS(on)}$	$R_{DS(on)}$ Shift vs. Time
Current	Drain-Source	DC current	Electromigration	$R_{DS(on)}$ Failure
			Thermomigration	$R_{DS(on)}$ Failure
			Thermal	DC SOA failures
		Pulsed current	Thermal	Pulsed SOA failure
			Unknown mechanism	Hyper-fast high current pulses
dv/dt	Drain-Source	Super-hard switching tests	$R_{DS(on)}$	$R_{DS(on)}$ Shift vs. Time
di/dt	Drain-Source	High current narrow pulse	Unknown mechanism	Hyper-fast high current pulses
Temperature	Package	Storage Temperature	Unknown mechanism	MSL1 testing
				High temp storage
Chemical	Package	Humidity	Dendrite formation/ corrosion	H3TRB testing
				HAST testing
Mechanical strain	Package	Temperature cycling	Solder fatigue	Temperature cycling test
		IOL	Solder fatigue	Temperature and Current test
		Bending force test	Delamination	I_{DSS} failures
		Die shear	Solder strength	Solder strength test
		Package force	Device breakage	Device pressure testing
Piezoelectric strain	Drain-Source	Pulsed	Unknown mechanism	Hyper-fast high current pulses
Radiation	Gate-Source	Gamma radiation	Charge trapping	V_{TH} shift vs. RAD(Si)
	Drain-Source	Single event	Propriety	I_{DSS} vs. LET and dose

Stress – Voltage

Gate-Source

Gate-Source Voltage Stress

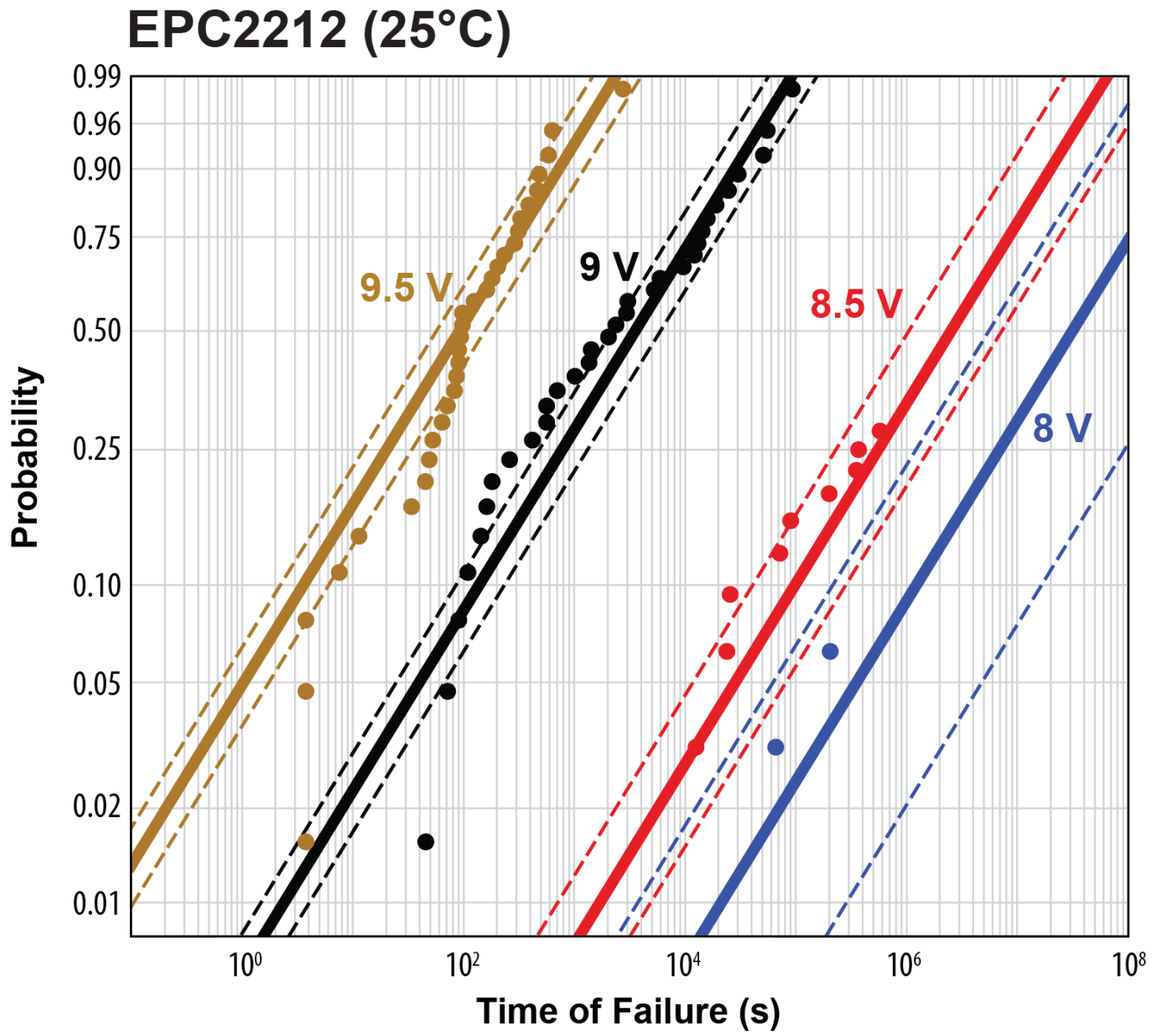
Basic structure of eGaN products in the region of the gate electrode

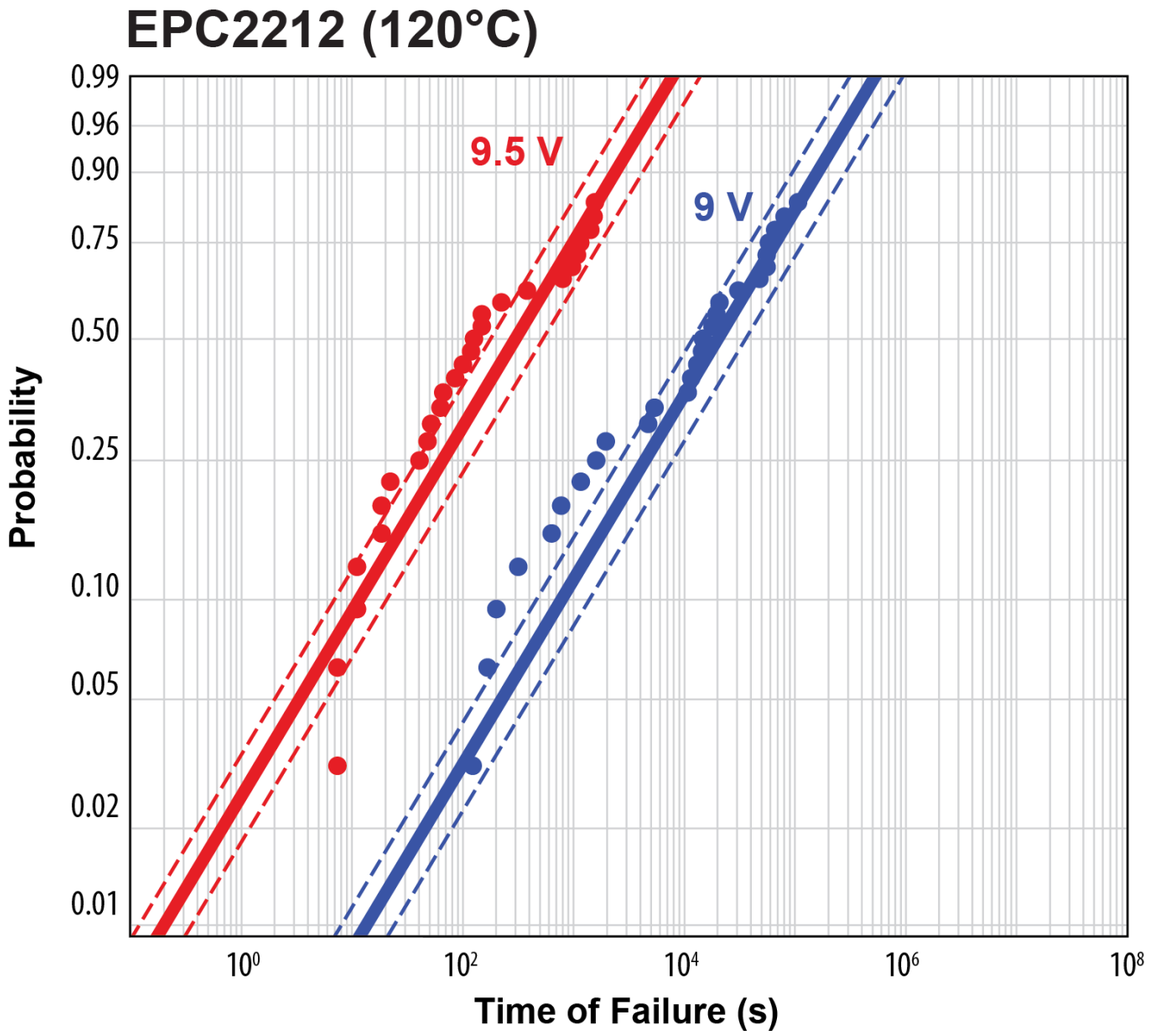


4639 eGaN FETs with this gate structure have been tested to 1000 hours each at 150°C **without failure**.

Gate Acceleration: Analysis

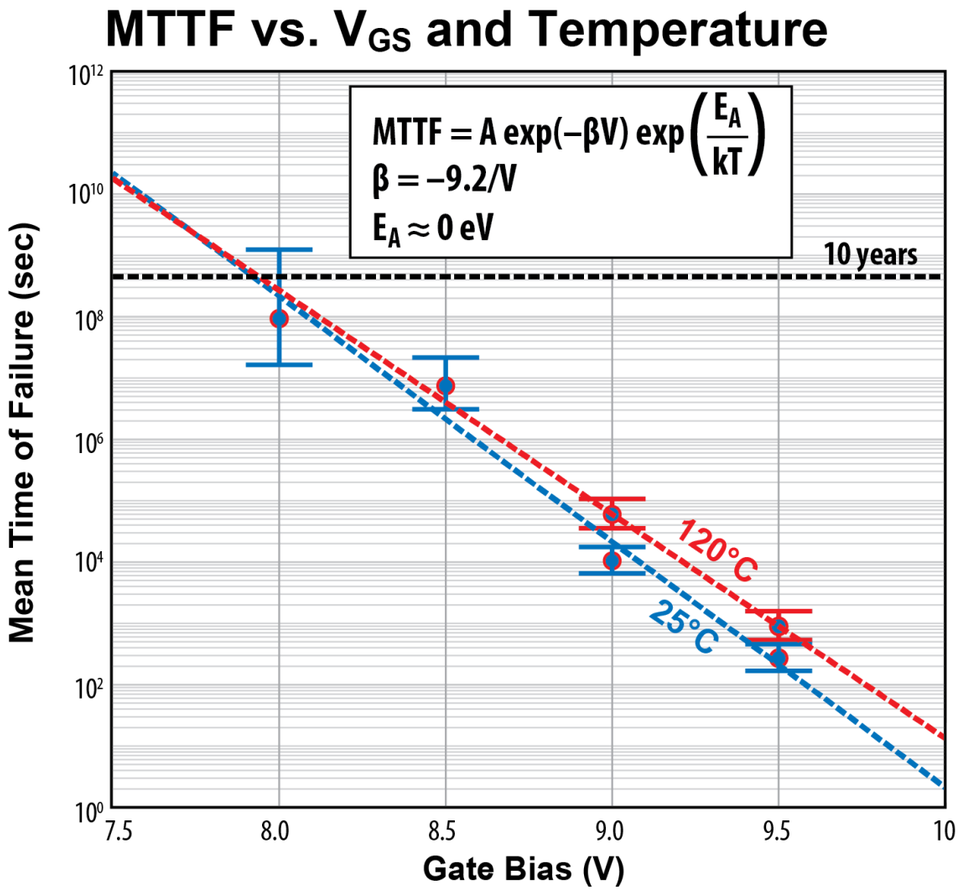
Data Sheet Maximum = 6 V_{GS}

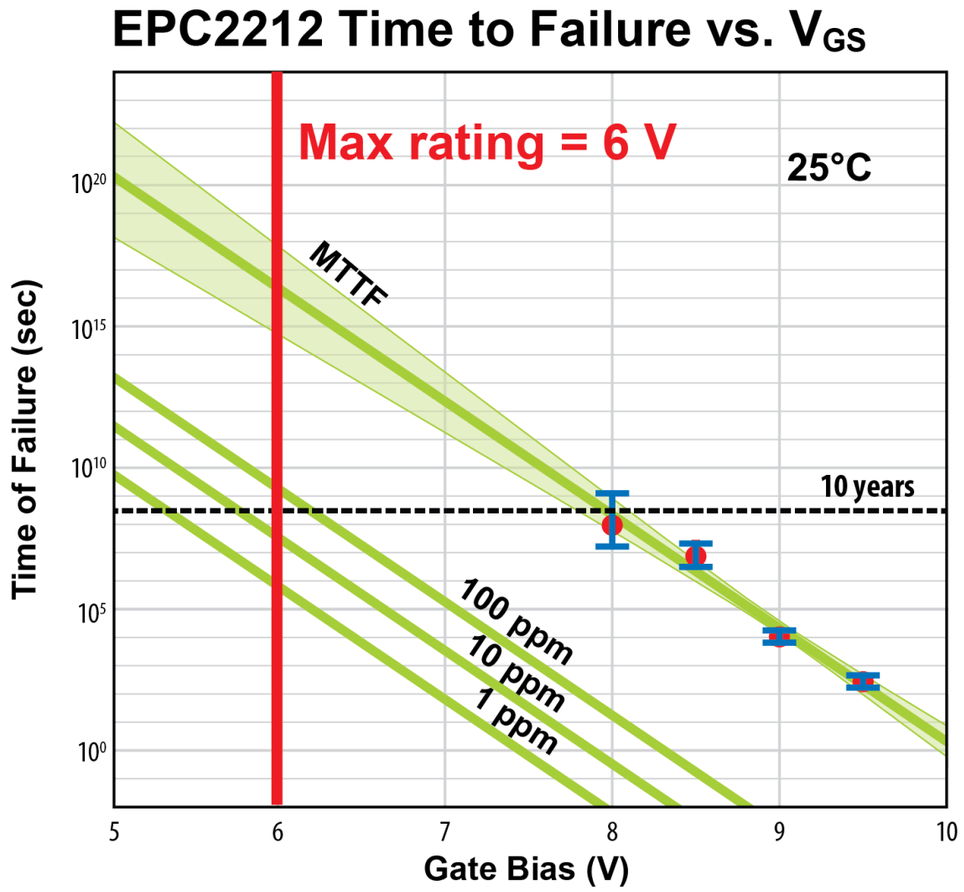




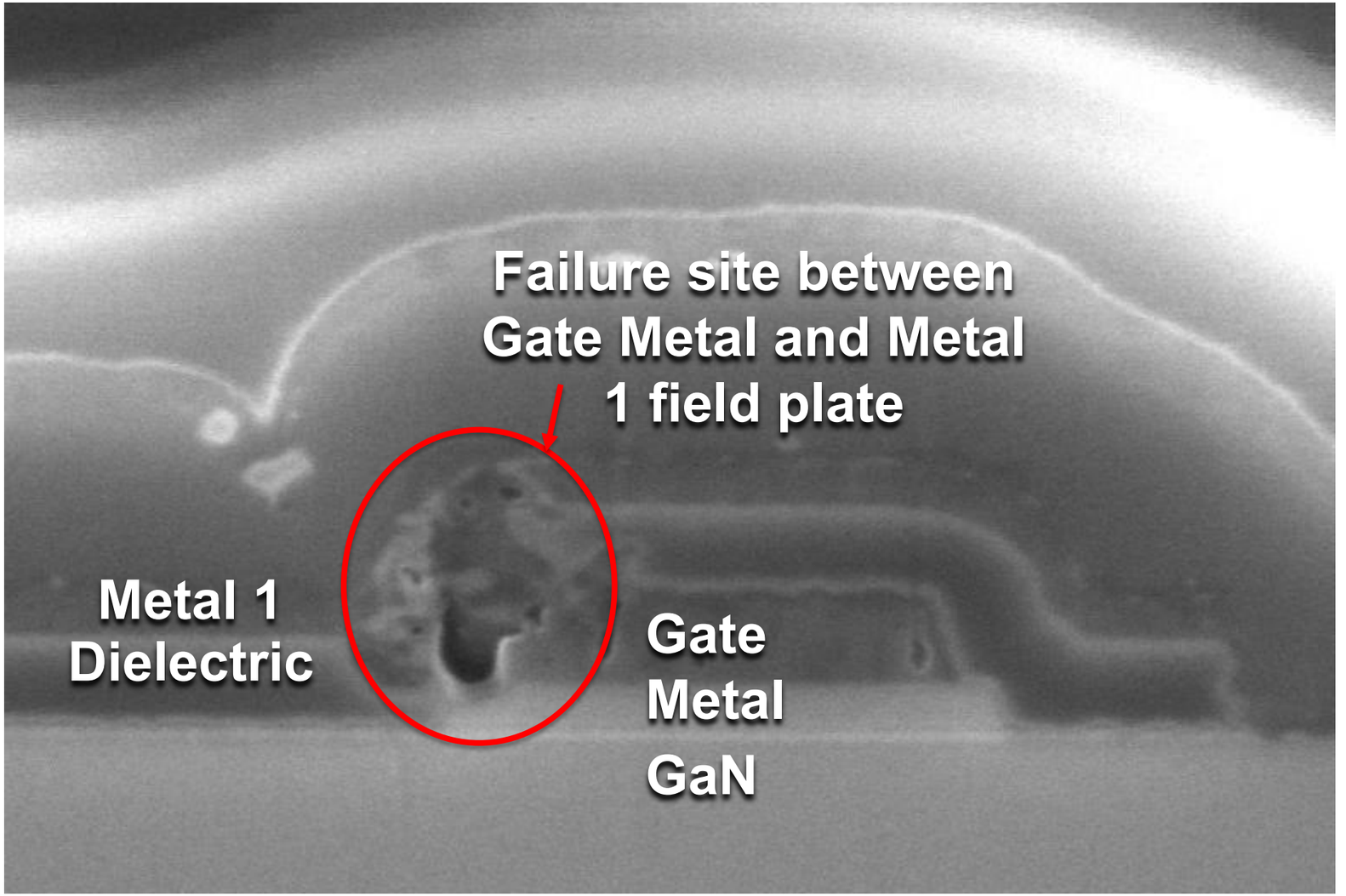
Gate Acceleration: Time to Failure

- Less than 100 ppm intrinsic failure rate in 10 years at data sheet maximum
- Less than 1 ppm intrinsic failure rate at 5 V recommended operating voltage
- More stringent definition for V_{GSmax} than for Si MOSFETs





Gate Failures Not in GaN

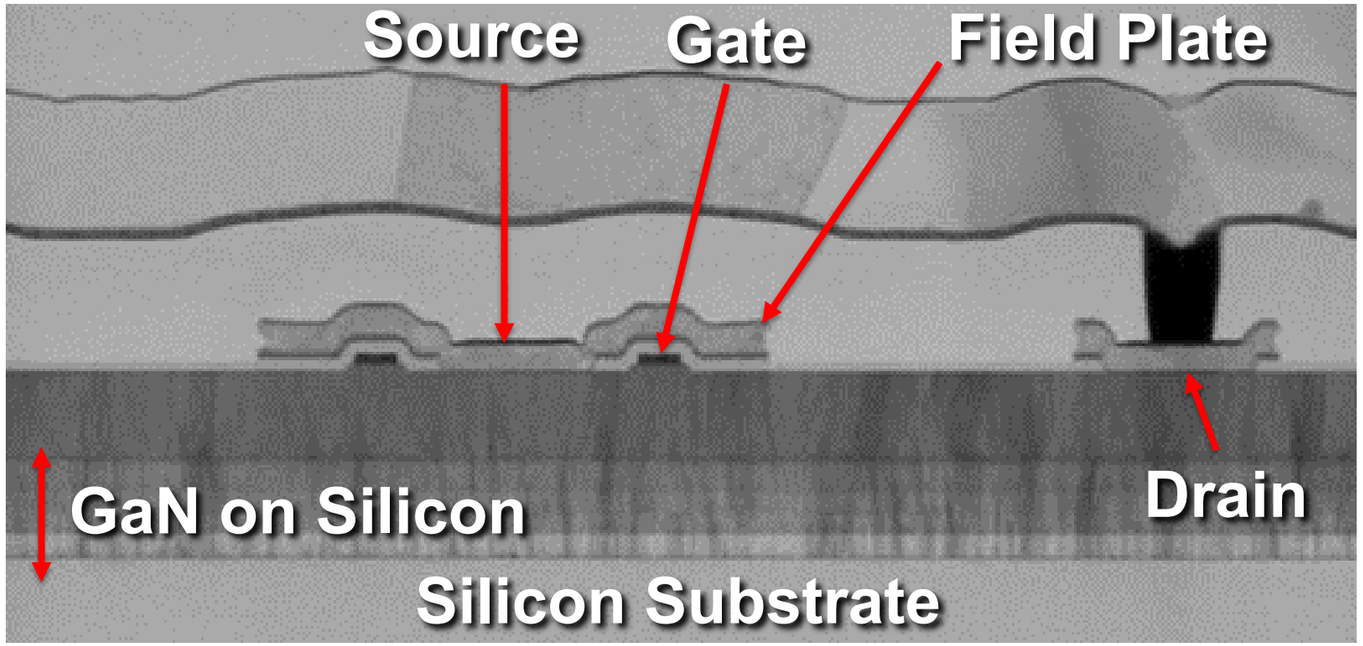


Stress – Voltage

Drain-Source

Drain-Source Voltage Stress

- Basic structure of eGaN products.
- There are several variations that would impact the failure rate under drain-source stress.

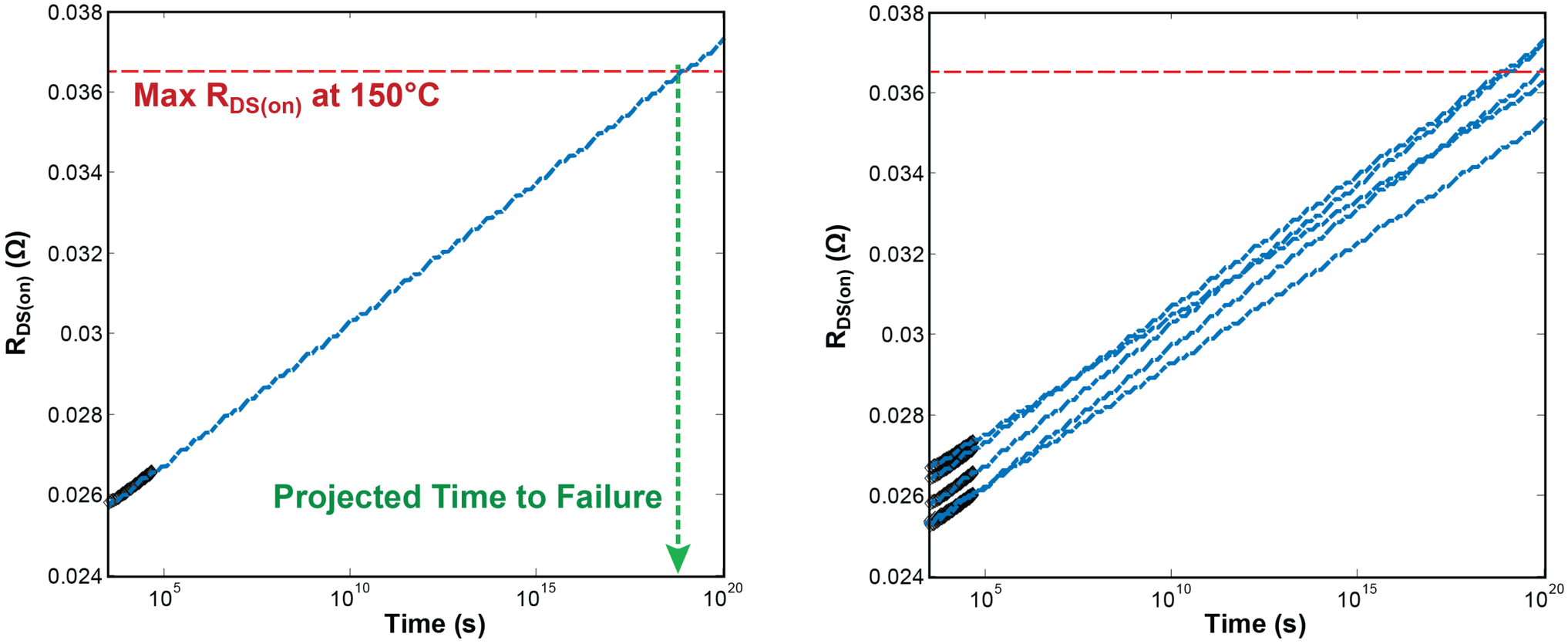


5133 eGaN FETs have been tested to 1000 hours each at 150°C **without failure.**

Characterizing $R_{DS(on)}$ Shift in Time

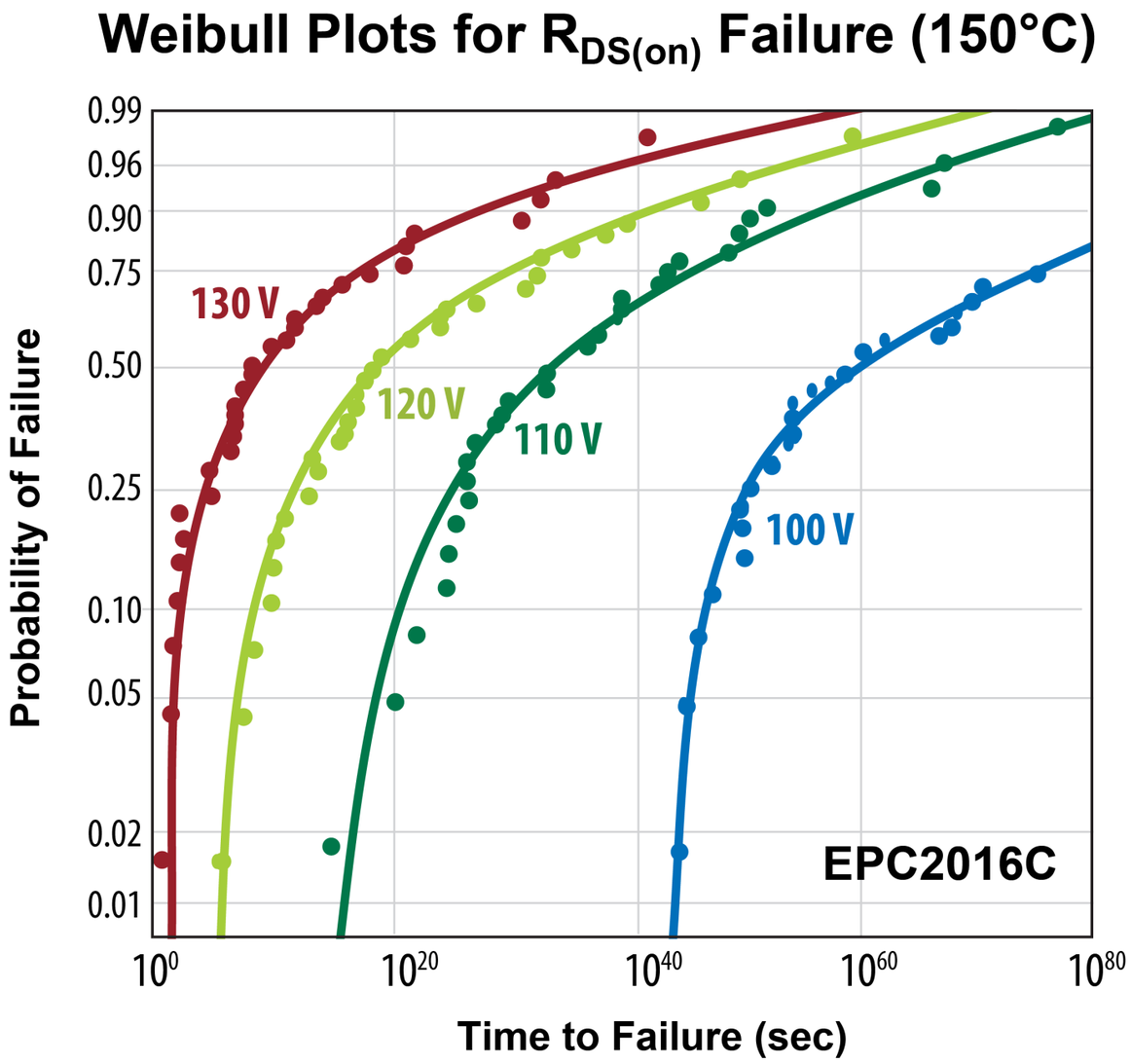
Data suggests a single trapping mechanism, reinforcing the assumption that short-term data can be extrapolated to accurately predict longer term data.

120 V overstress at 150°C (100 V Rated Device)

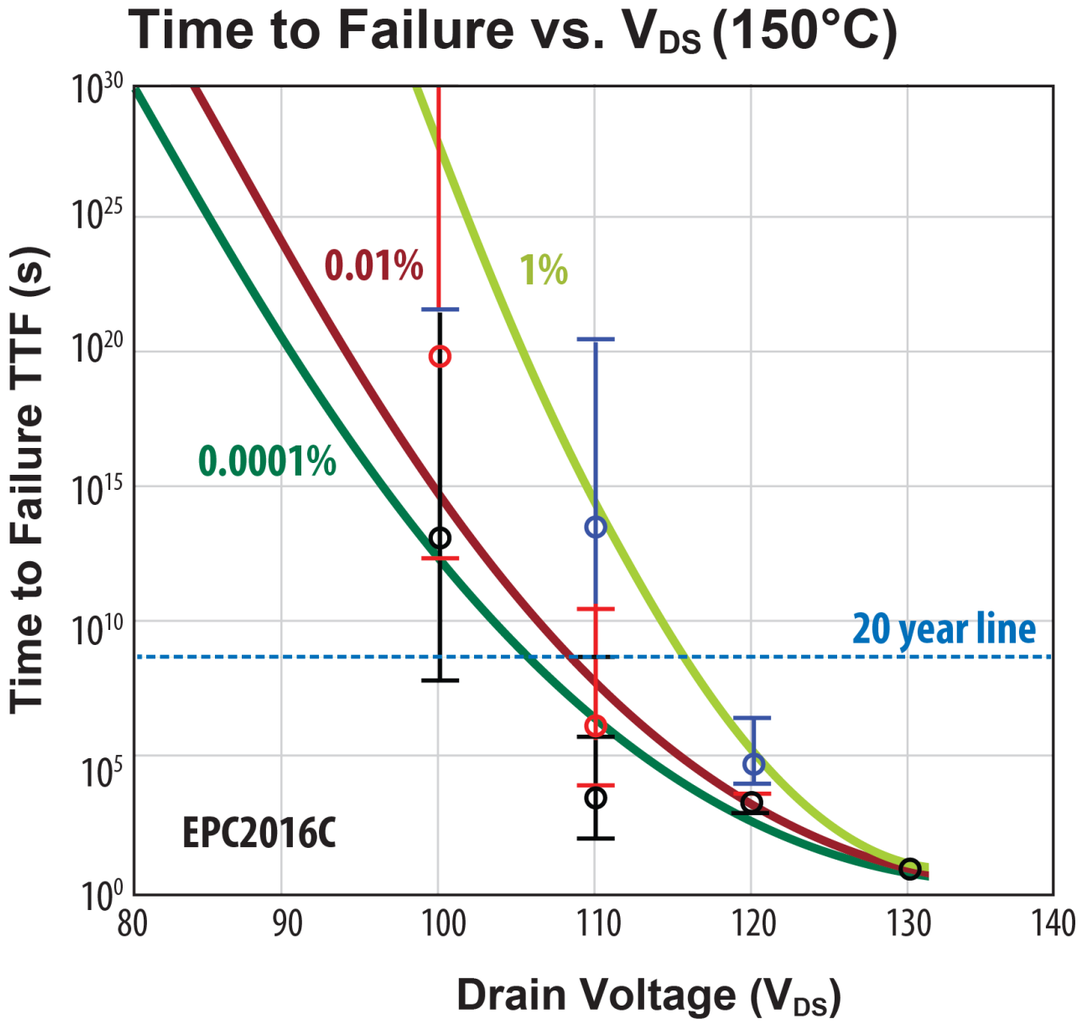


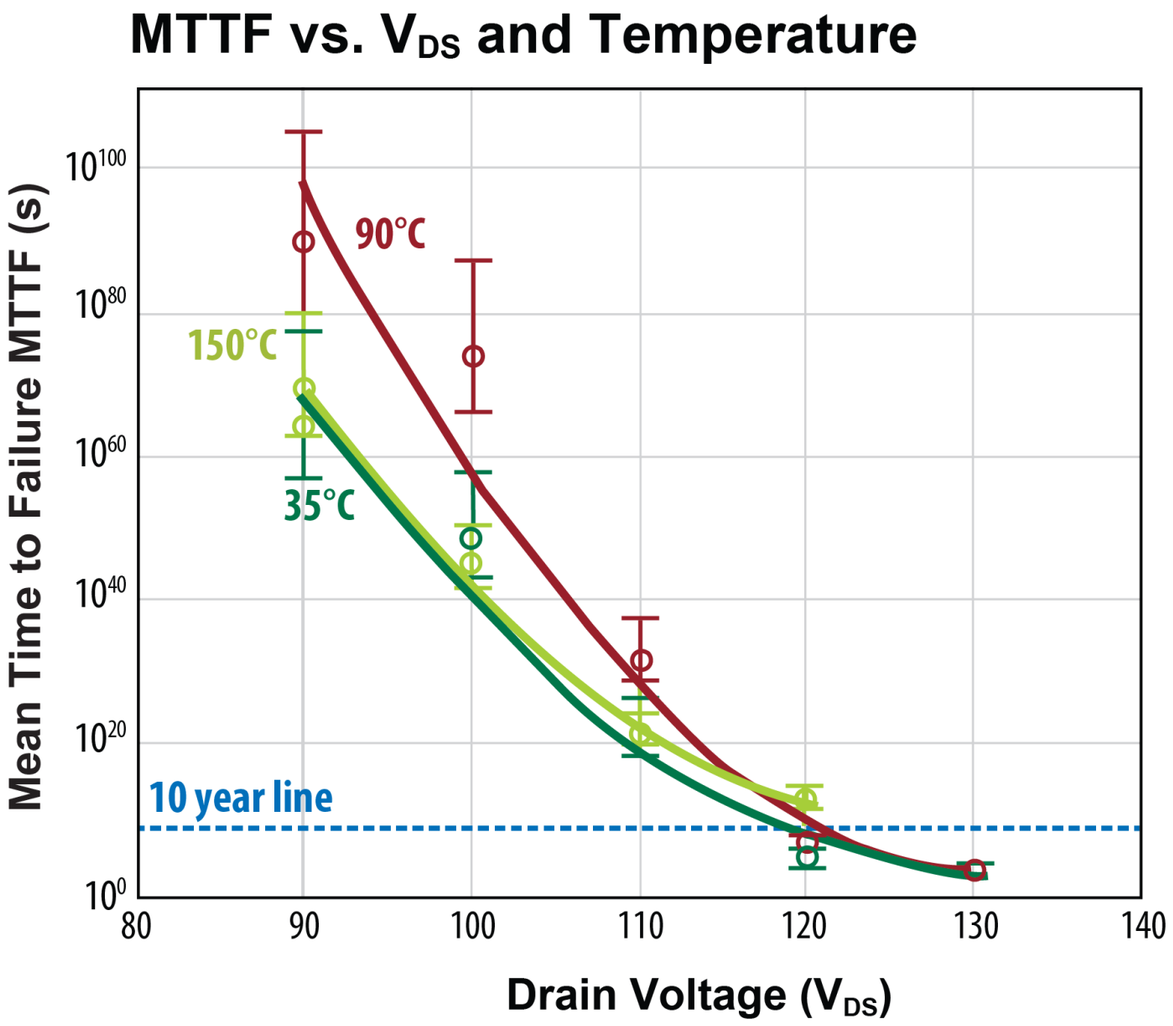
$$R(t) = R_0 (\alpha + \beta \ln[t])$$

Drain Stress Weibull Fits

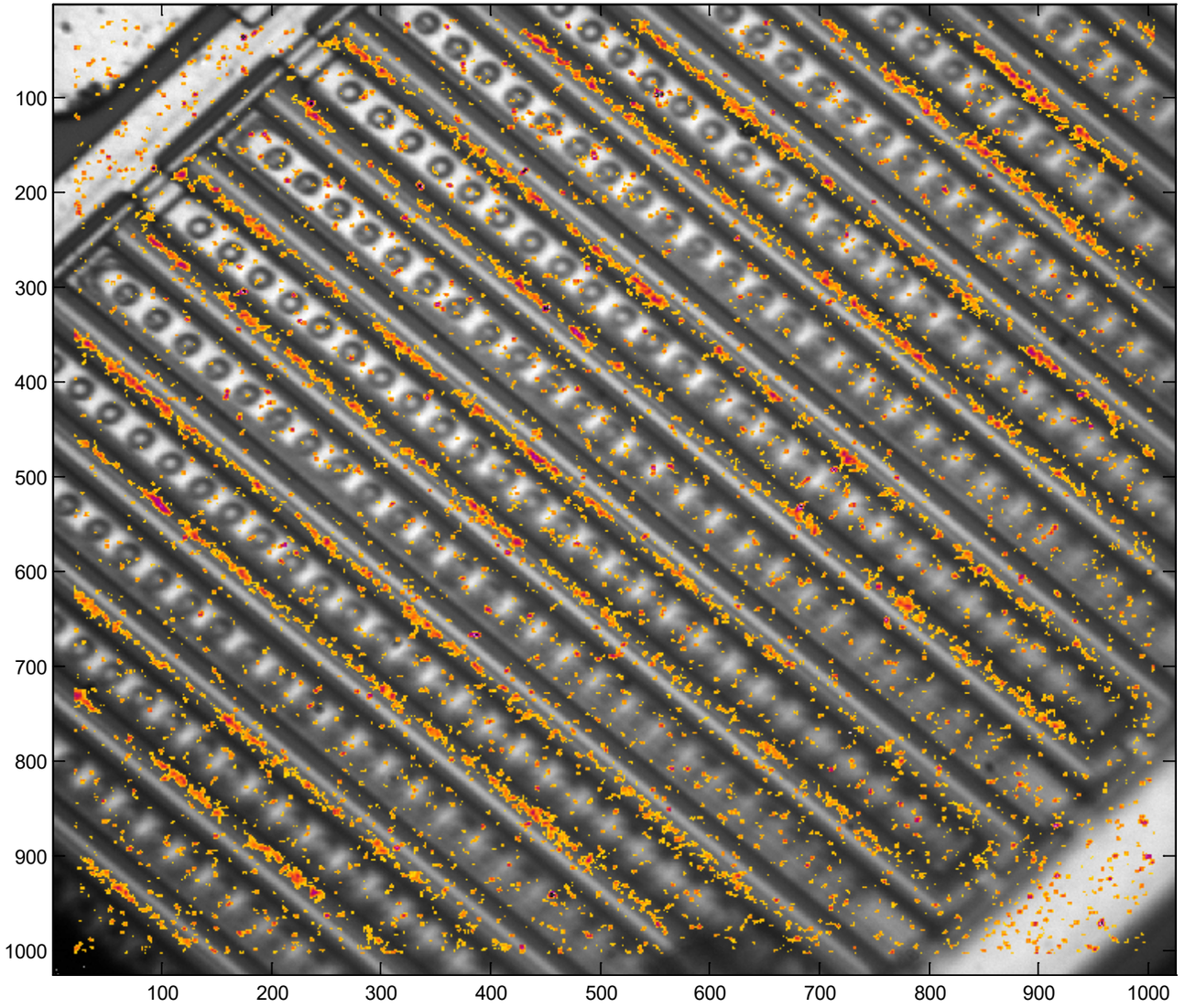


Device Robustness vs. V_{DS}

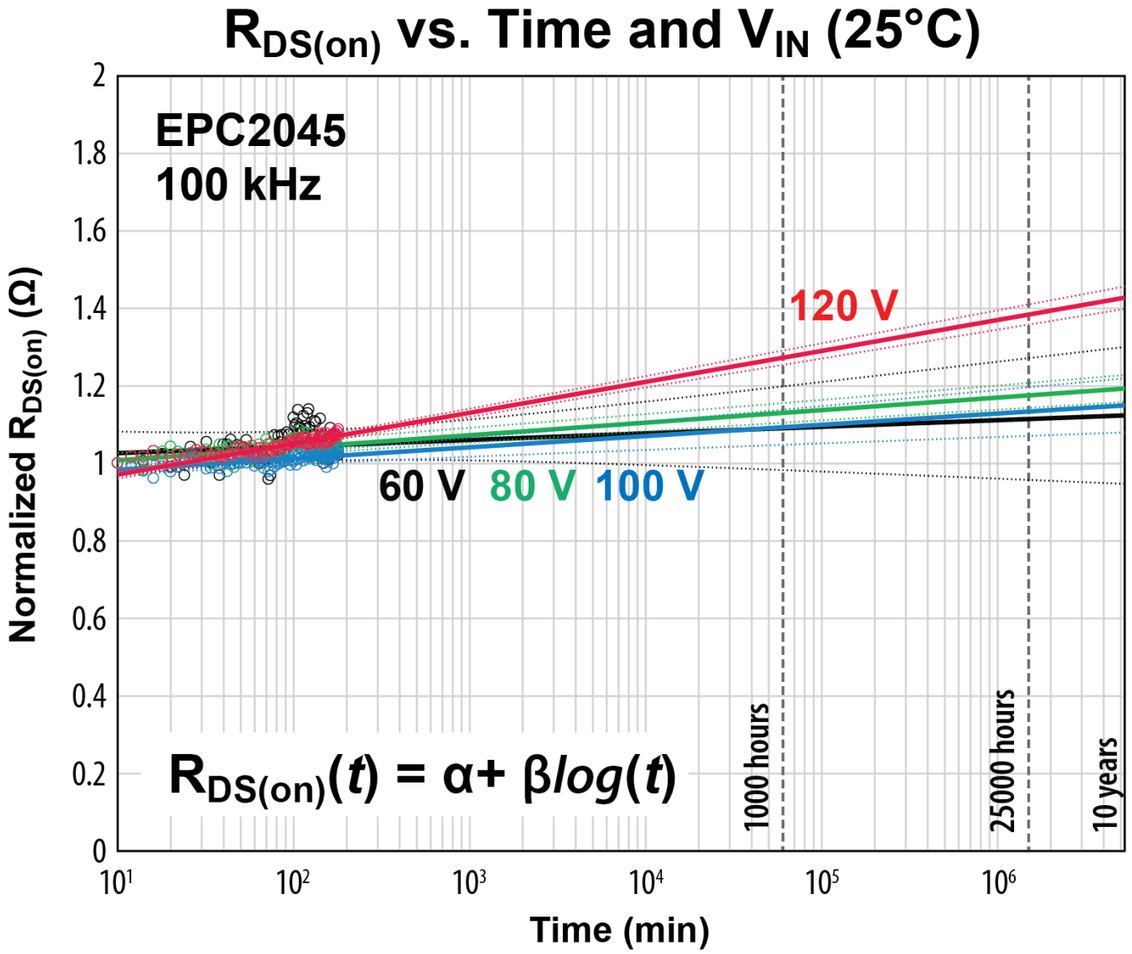


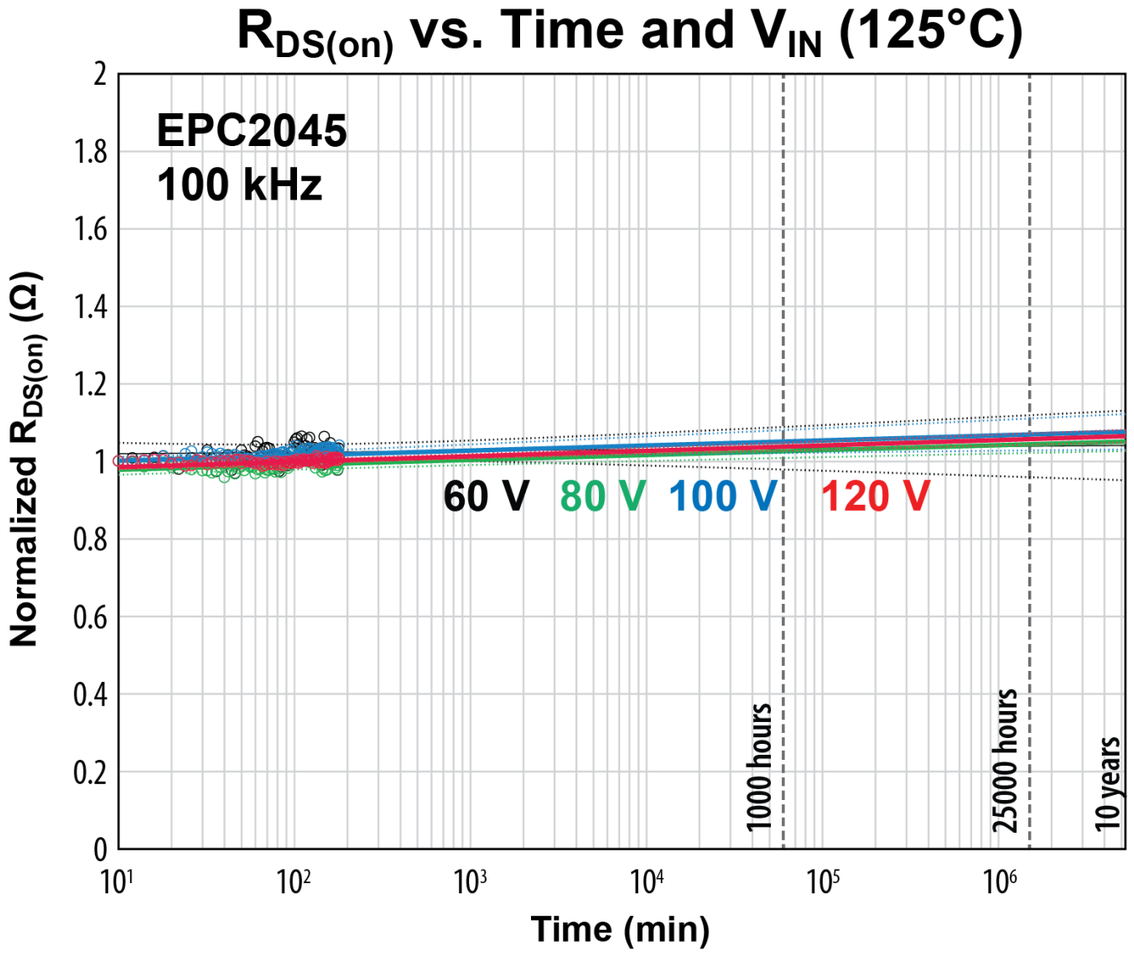


Physics of $R_{DS(on)}$ Shift – Hot Carrier Emission



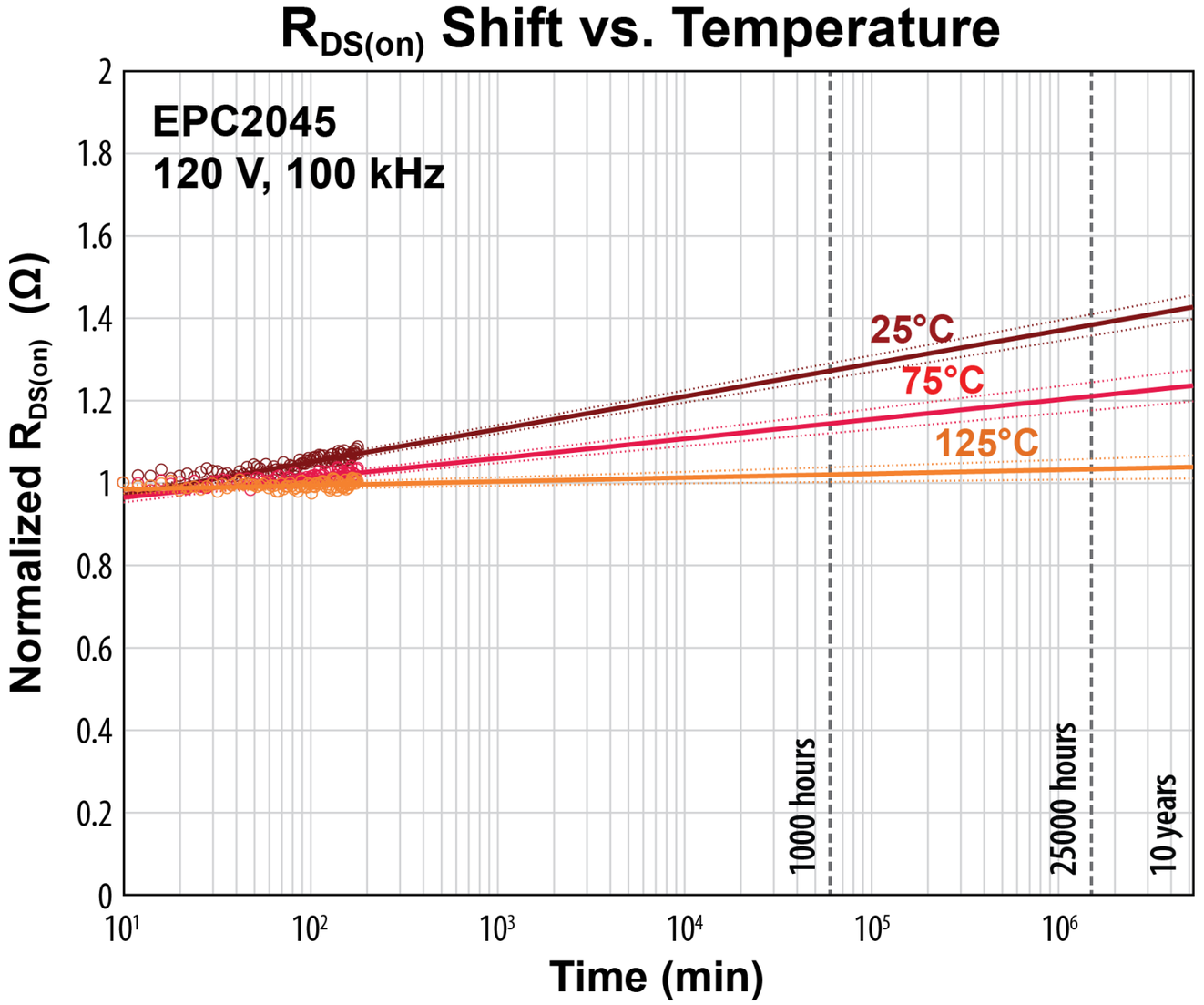
Hard-Switching: Effect of V_{IN} for 100 V Product





Hard-Switching: Effect of Temperature

This negative temperature activation is consistent with hot-electron scattering theory.

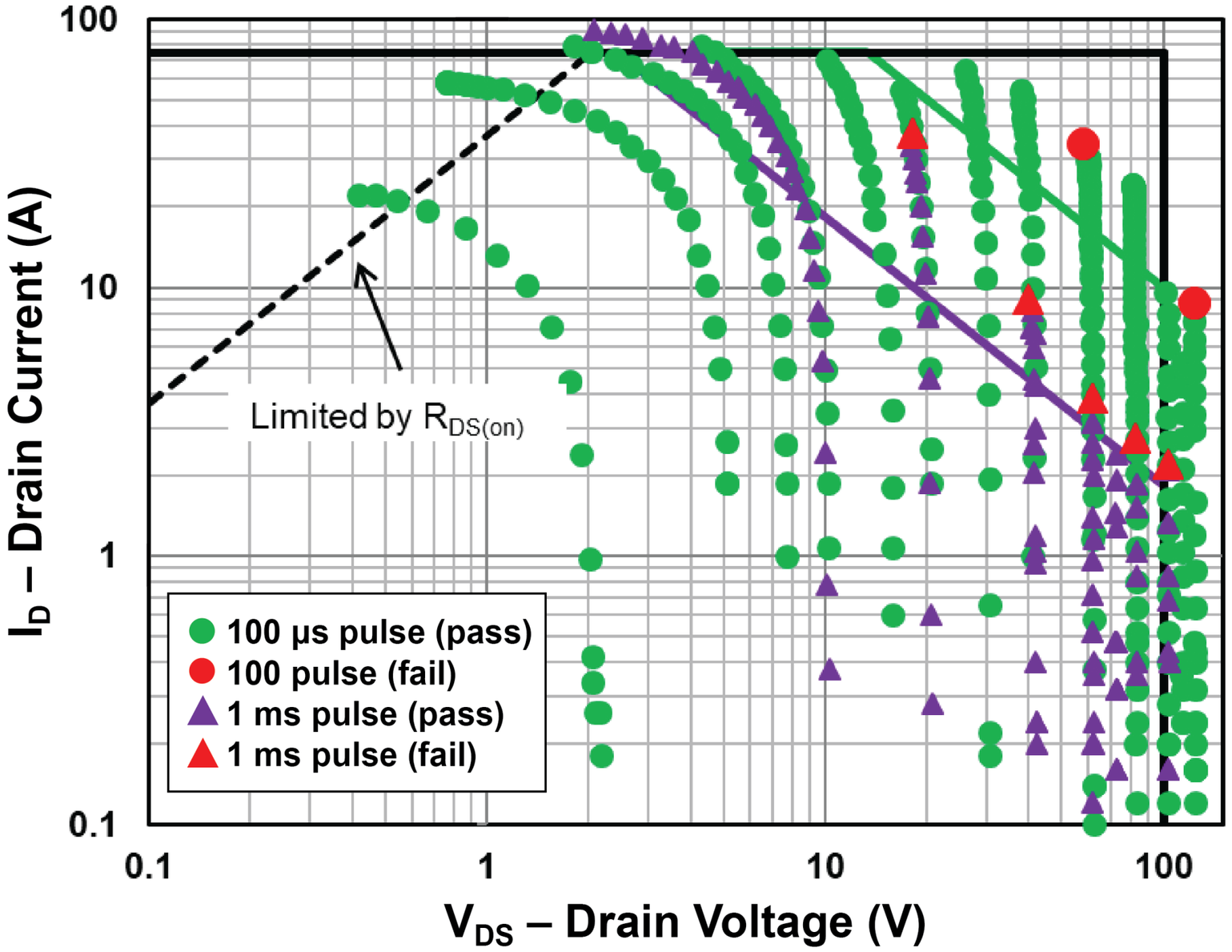


Stress – Current

Safe Operating Area

di/dt

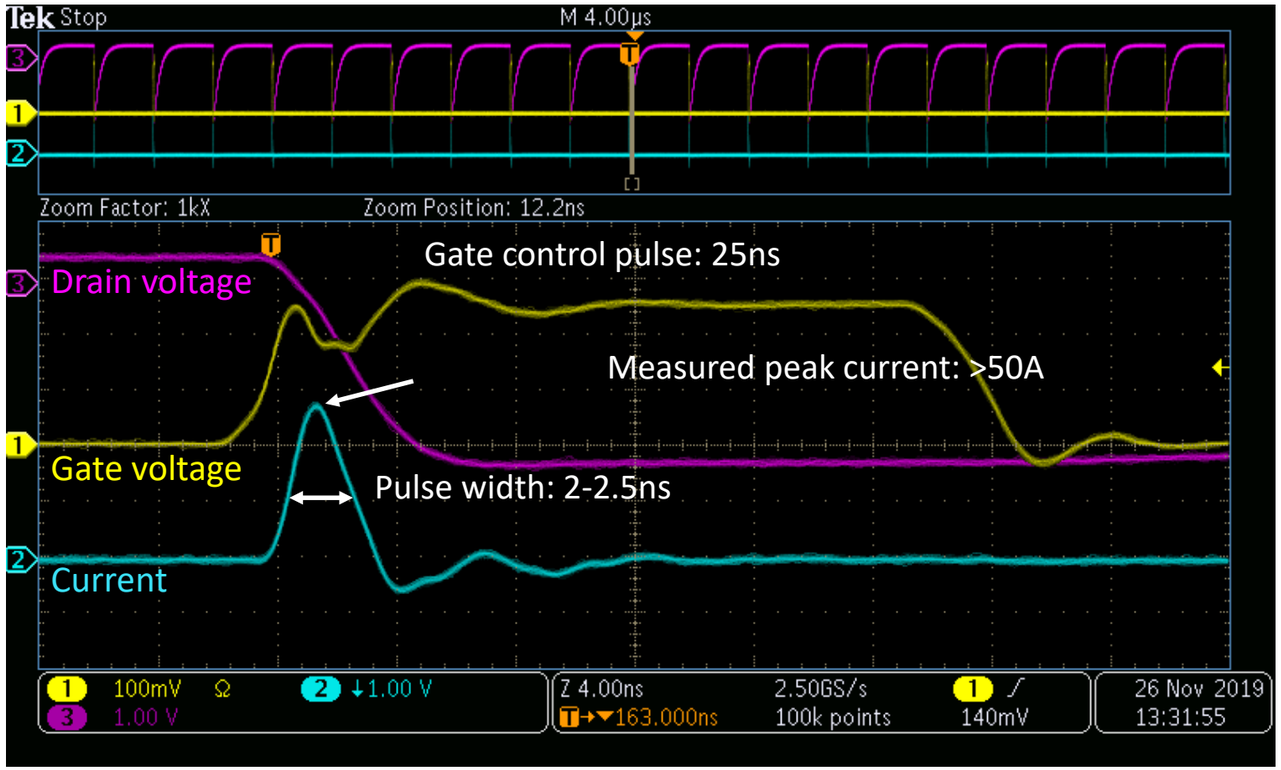
SOA Test Results: EPC2212



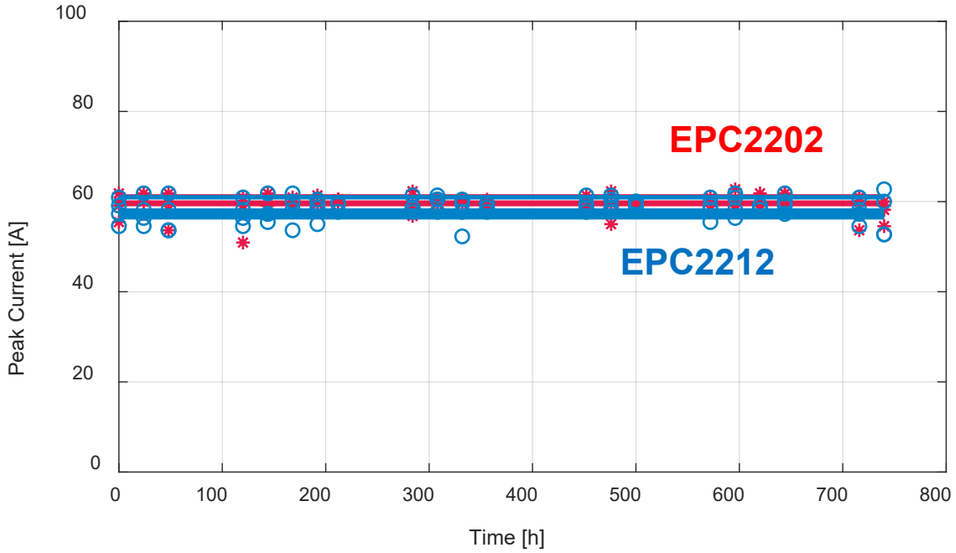
Note:
The "Limited by $R_{DS(on)}$" line is based on data sheet maximum specification for $R_{DS(on)}$ at 150°C.

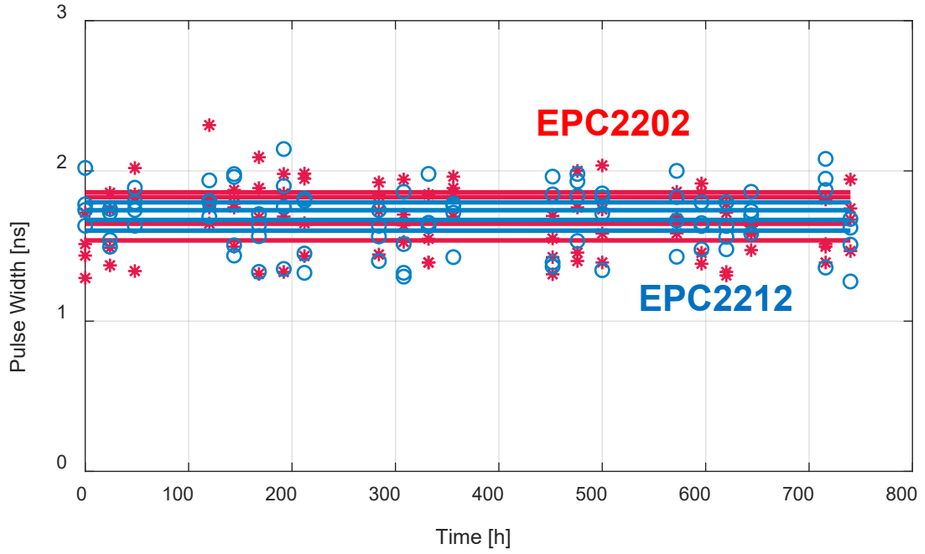
Long-Term Stability Under High Current Pulses

Continuous operation with pulsed current: 80 V, >50 A , 500 kHz



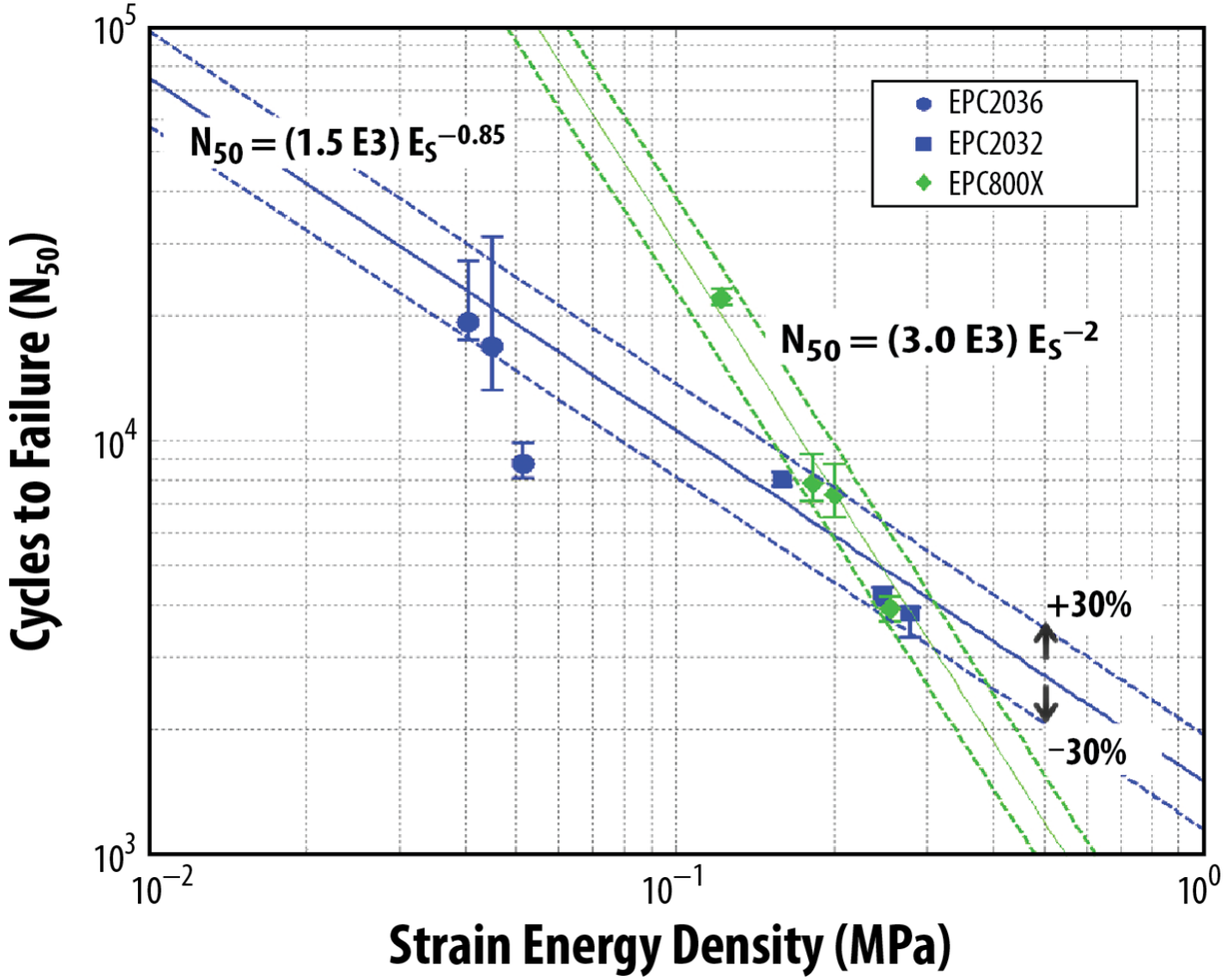
- 8 samples (4xEPC2212, 4xEPC2202)
- Over 5 weeks of operation at 500 kHz (>1 trillion pulses). Test ongoing.
- 300 billion pulses approximates 10-year life

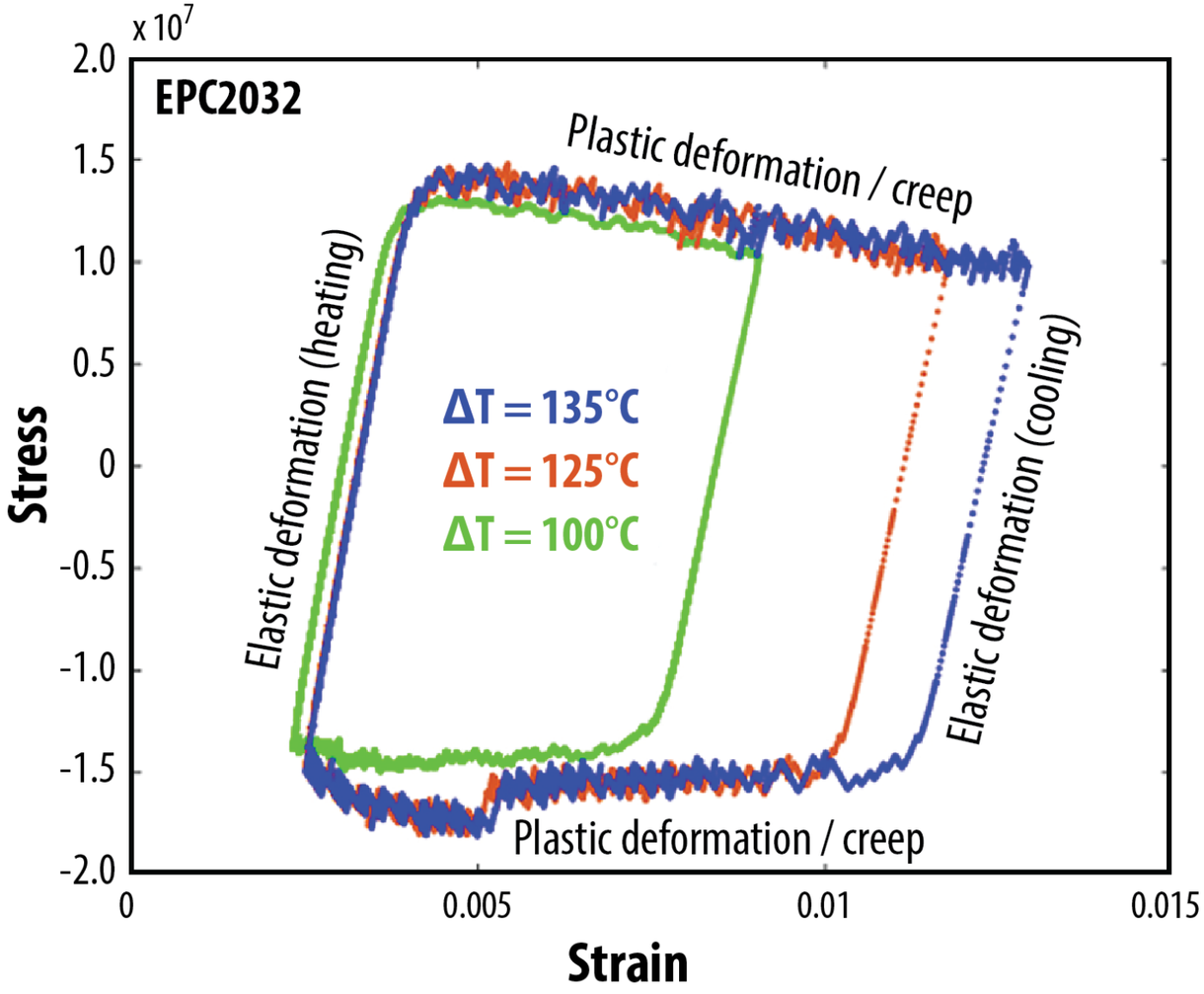




Stress
Thermo-Mechanical

Thermo-mechanical Modeling and Verification





[1] Jean-Paul Clech, "Solder Reliability Solutions: A PC-Based Design-For-Reliability Tool," Proceedings, Surface Mount International, San Jose, CA, Sept 1996.

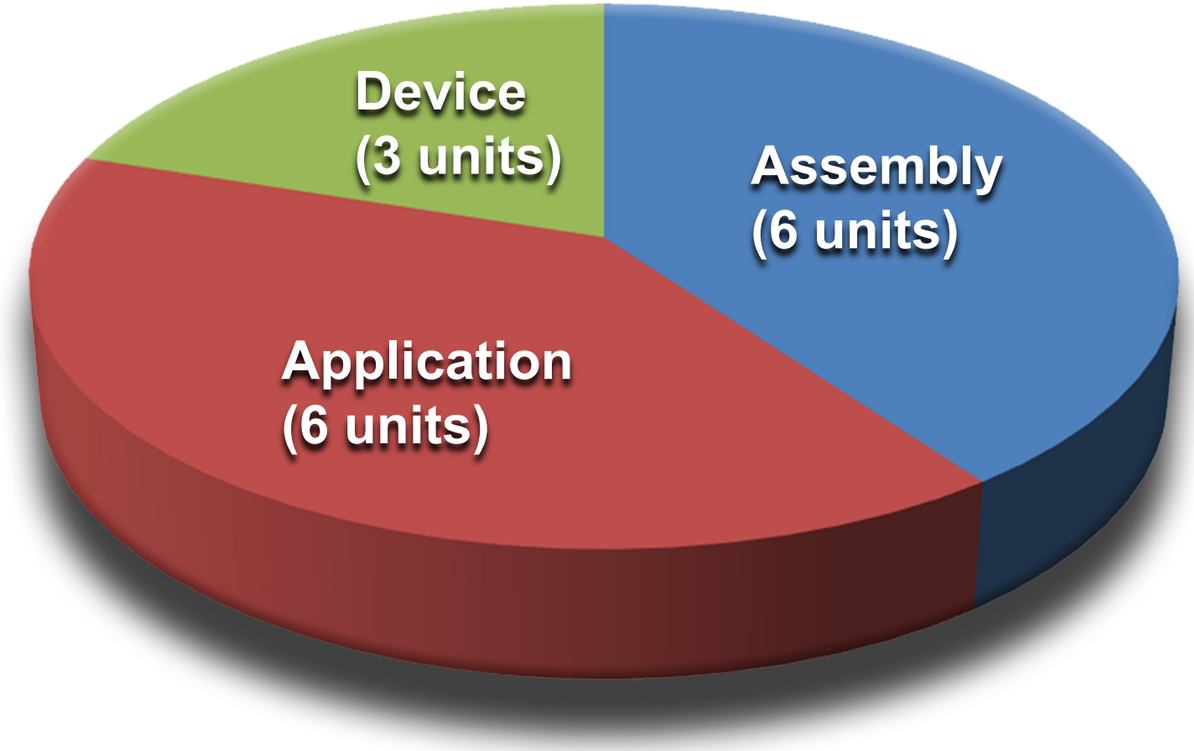
Strain Energy Density Calculation (Area inside stress-strain curve)

Results

GaN FET Reliability

Field Failures by Category

1/1/2017– 6/30/2019



Proven Reliability – 85 billion device hours in the field since January 1, 2017 with only 3 device failures.