Ultra-High Density Double-Sided Half-Bridge Packaging with Organic Laminates

Dr Douglas C Hopkins,
Tzu-Hsuan Cheng

Invited Paper

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Acknowledgements

This material is based upon work supported in part by the U. S. Army Research Laboratory and the U. S. Army Research Office under contract number W911NF1820135 with TPOC Dr. Lauren Boteler

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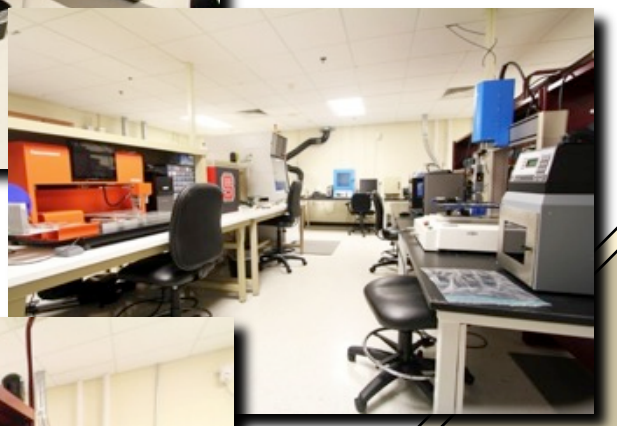
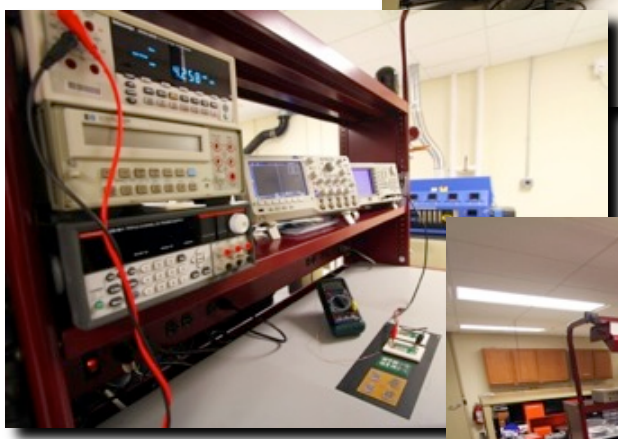
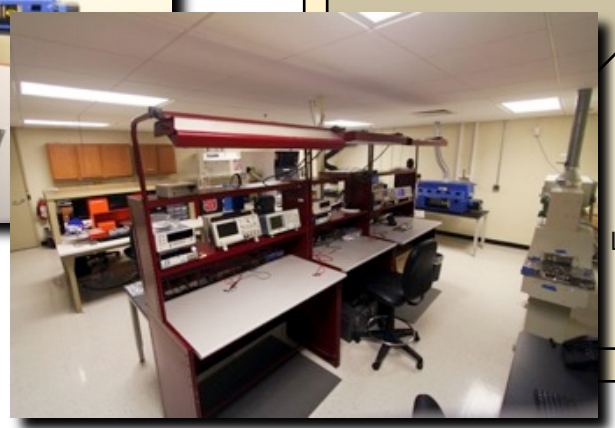
PREES Laboratory Enhancements







LPKF-contac-S4
Reliable Through-hole
Plating in the Lab

LPKF® MultiPress S
Automatic Lamination Press

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circuit board plotters

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TPT-HB05 Manual
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The trend to higher performance power electronic systems has fostered more electrophysical integration including inclusion of more microelectronics packaging and assembly approaches.

This presentation reviews the new trends in kilovolt packaging using organic substrates, and specifically Epoxy Resin Composite Dielectric (ERCD) materials.

An application is to a lower voltage package (<1500V) for the new BiDirectional FET (BiDFET)

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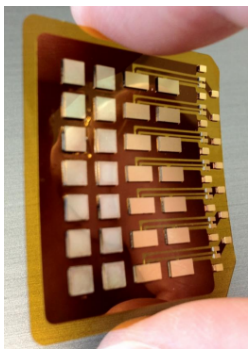
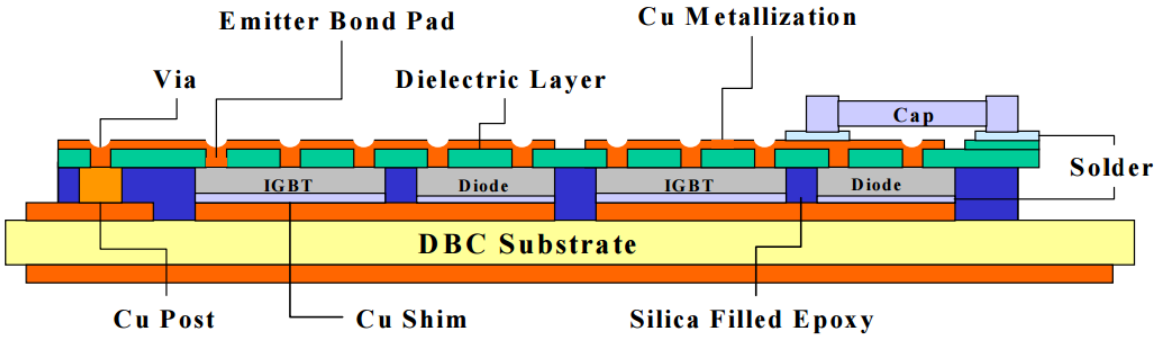
Double-sided power modules- type 1

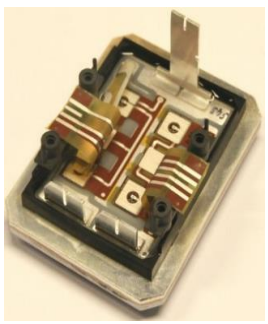
Double-sided electrical contact / Single-sided cooling

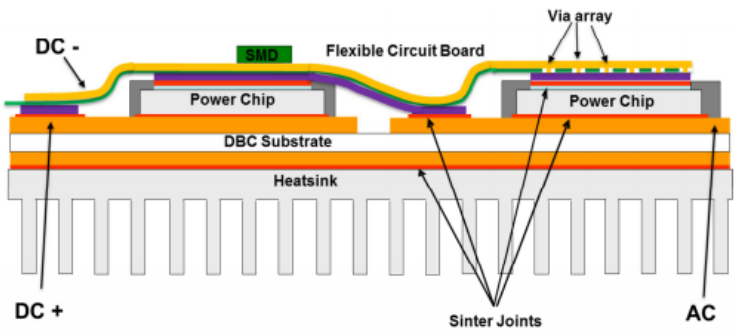


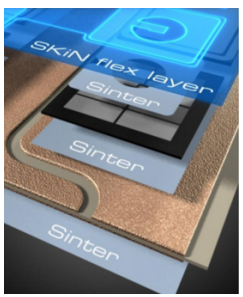
Power Overlay package [1]



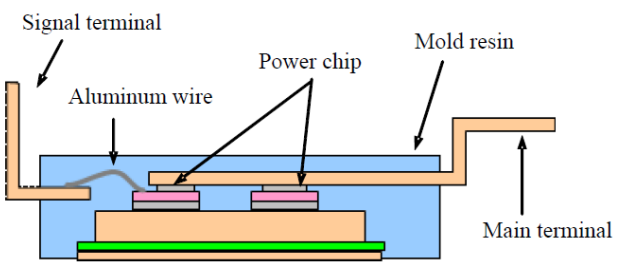
Semikron SKiN module [2]

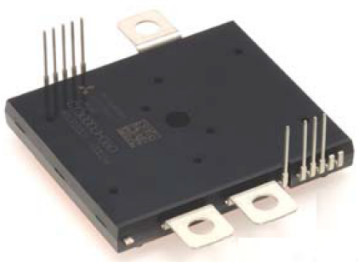






Mitsubishi Direct Lead Bonding (DLB)





[1] Ozmat, B.; Korman, C.S.; McConnelee, P.; Kheraluwala, M.; Delgado, E.; Fillion, R., "A new power module packaging technology for enhanced thermal performance, "Thermal and Thermomechanical Phenomena in Electronic Systems, 2000. ITHERM 2000, vol.2, no., pp.287, 296 2000.
[2] S. Hauser. Direct Pressed Die Technology: Increased Power Density and Reliability in Standard Power Module Packages. APEC 2017, Tampa, FL.

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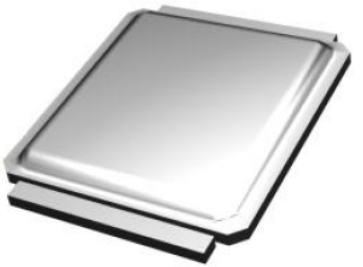
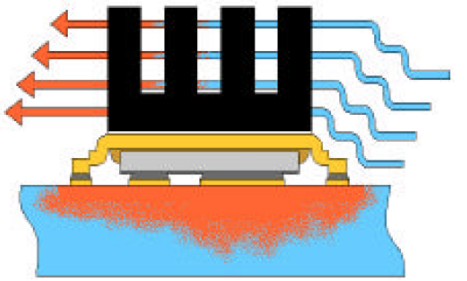
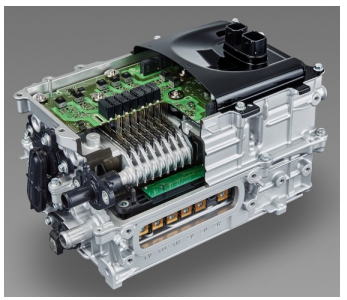
Double-sided power modules- type 2

Double-sided planar electrical contact / Double-sided cooling

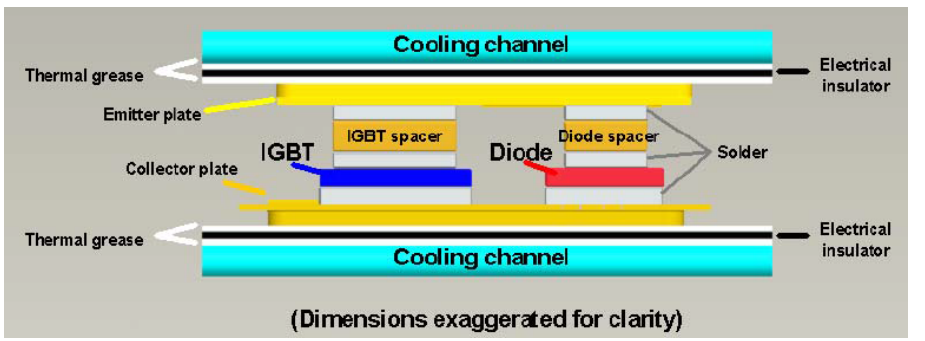
International Rectifier DirectFET

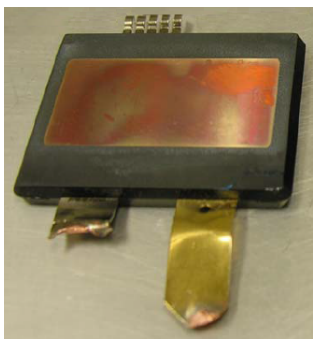




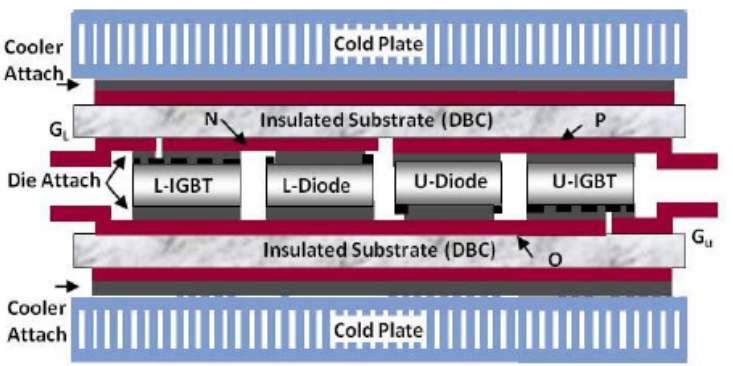


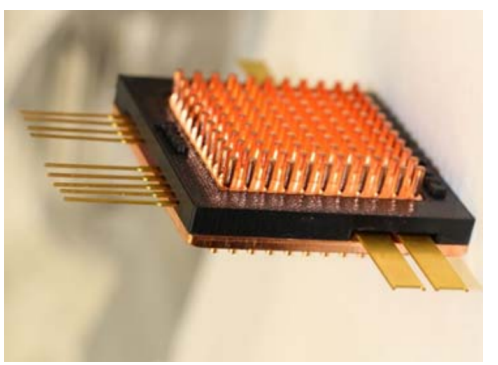
Toyota-Denso Double sided module





Oak Ridge National Lab All planar Module [1]





[1] F. Yang, et al. Design of a Low Parasitic Inductance SiC Power Module with Double-sided Cooling. APEC 2017, Tampa, FL.

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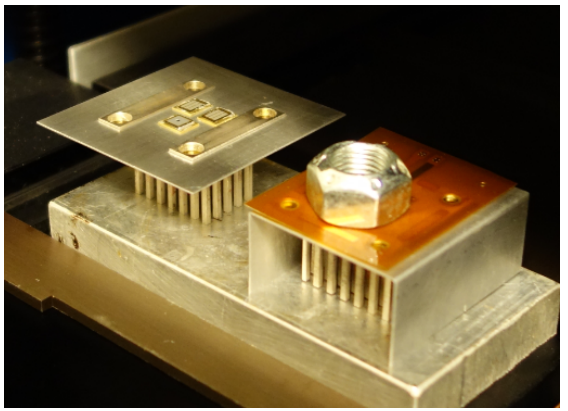
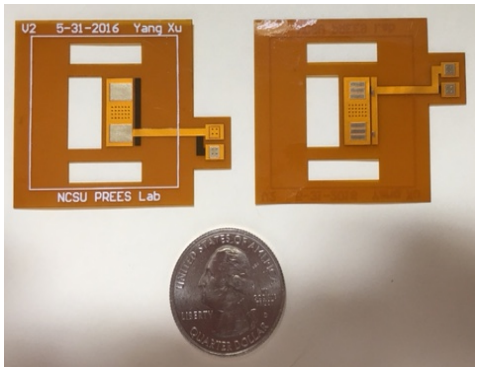
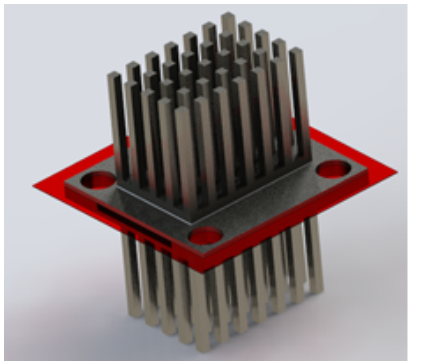
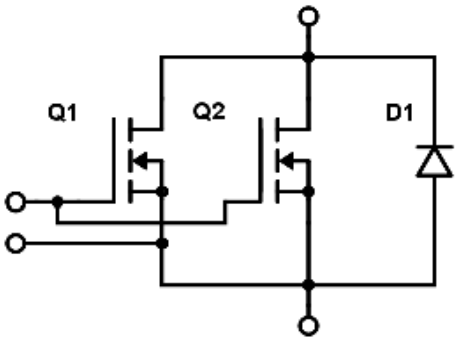
R_{th} Benchmark for Power Chip on Bus (PCoB)





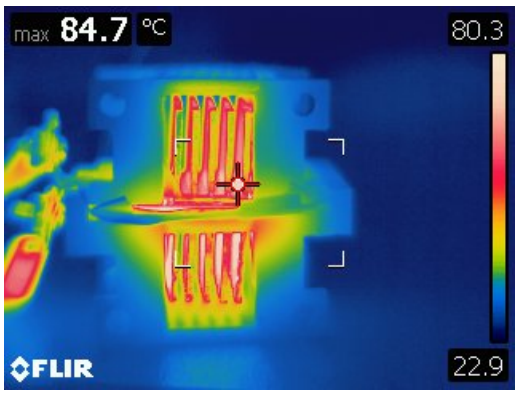




$40\times40\times40mm^3$ & ~60 grams

The module is designed for 1200V and 100A.

Two 1200V, 50A SiC MOSFETs (CPM2-1200-0025B) and one 1200V 50A anti-parallel SiC Schottky diode (CPW5-1200-Z050B) bare dies are chosen for each module.



Test condition: No encapsulation, single-fan air cooled, SiC Schottky diode heating, ambient at 25˚C. Die size of 4.9 x 4.9 mm

Tested $\boldsymbol{R_{th_ja}}$ =0.53C/W (about 15CFM flow Rate)

Thermal capability: *100W dissipation, 50 ˚C increase, air-cooled power module density: >60 kW/ L.*

Equivalent to liquid cooled DBC structures

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New Thin Organic Dielectrics for Low Cost Modules

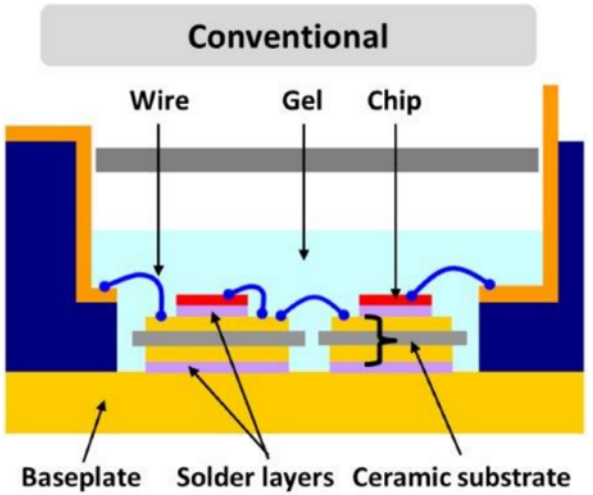
Epoxy Resin Composite Dielectrics – ERCDs

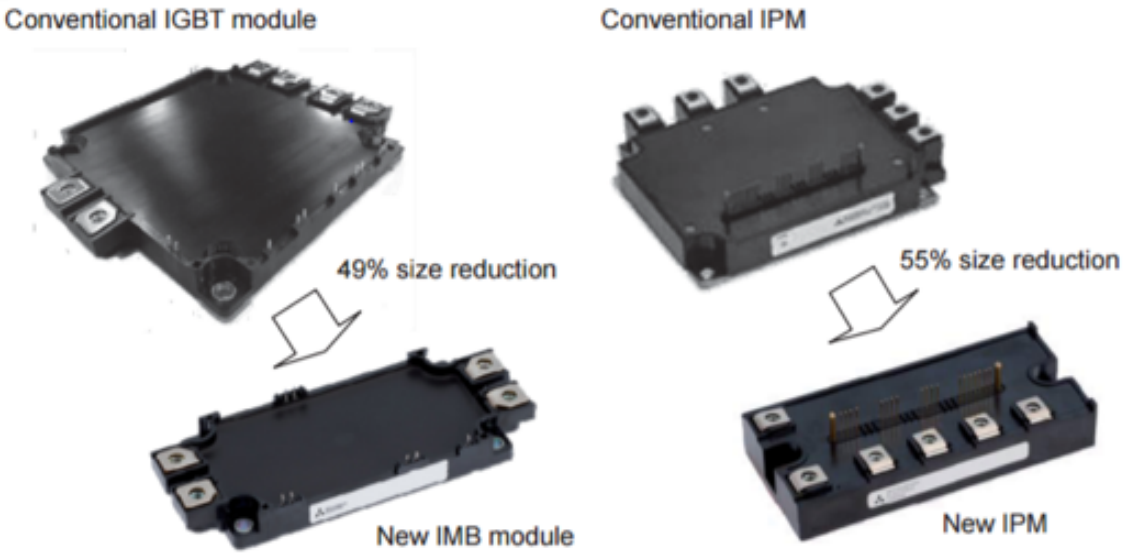
These provide and opportunity to look at very low cost modules with *embedded* components.

"Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao[1], Yifan Jiang[1], Bo Gao[1], Kenji Nishiguchi[2], Yoshi Fukawa[3], D. C. Hopkins[1]

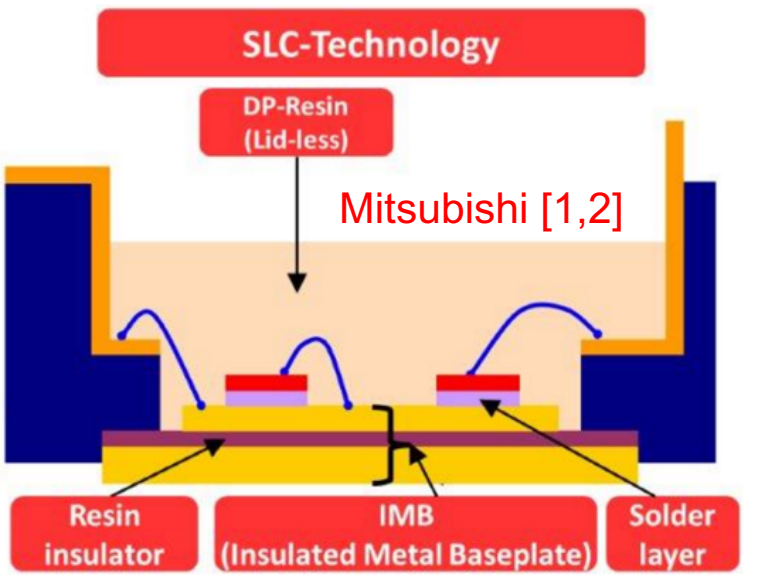
[1]North Carolina State University, [2]Risho Kogyo Co., LTD, [3]TOYOTech LLC

Development of WBG power module w/ Resin Insulator





- CTE of insulating resin layer ~17ppm, close to Copper, with better mechanical stress management
- 35% thermal impedance reduction from development of resin
- Fewer interconnection layers for lower profile, up to 55% size reduction from traditional DBC based module
- Better thermal cycling reliability with less cracks during cycling
  - Depends heavily on the resin interface material



[1] Y. Kaji, et al. Novel IGBT Modules with Epoxy Resin Encapsulation and Insulating Metal Baseplate. ISPSD'16.

[2] T. Takahashi, et al. A 1700V-IGBT module and IPM with new insulated metal baseplate (IMB) featuring enhanced isolation properties and thermal conductivity. PCIM Europe 2016.

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High Thermal Conductivity Materials

RISHO

AD-7006
0.3W/mK

Low resin flow Bonding sheet

CS-3945
1.3W/mK
CCL

CS-3295, ES-3245
3W/mK
CCL, Prepreg

Glass epoxy laminate, Prepreg

[1] Low modulus
CC: Cu Clad
CCL: Cu Clad Laminate
AC: Aluminum Clad
ACL: Aluminum Clad Laminate
CS: Woven Glass cloth
ES: B-Stage w/ Woven Glass cloth

Liquid Molding Compound
(One-pack type)
(1～4W/mK)

Liquid Molding Compound
(Two-pack type)
(1～7W/mK)

AC-7900
1W/mK
Al base CCL

[1] AC-7303
3W/mK
Al base CCL

AC-7200TY
5W/mK
Al base CCL

AC-7208
8W/mK
Al base CCL

AC-7210
10W/mK

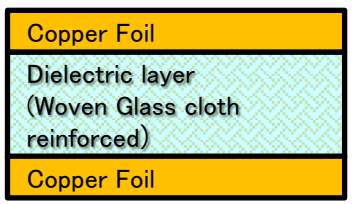
[1] CC-7303
AD-7303
CD-7303
3W/mK

CC-7200TY
AD-7200TY
CD-7200TY
5W/mK

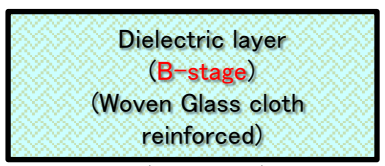
AD-7208
CD-7208
8W/mK

AD-7210
CD-7210
CC-7210
10W/mK

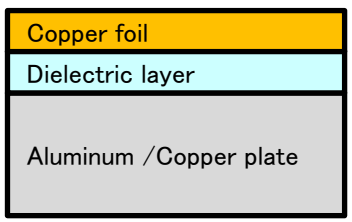
Bonding sheet, RCC, Copper-base CCL without glass fabric



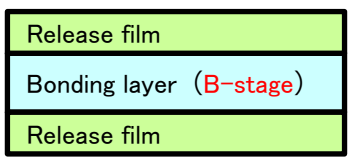
CCL: Cu Clad Laminate
(CS-XXXX) Woven Cloth



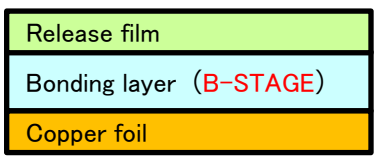
Prepreg (ES-XXXX)



CCL: Cu Clad Laminate
with metal base (AC-XXXX)



Bonding sheet (AD-XXXX)



RCC (CD-XXXX)

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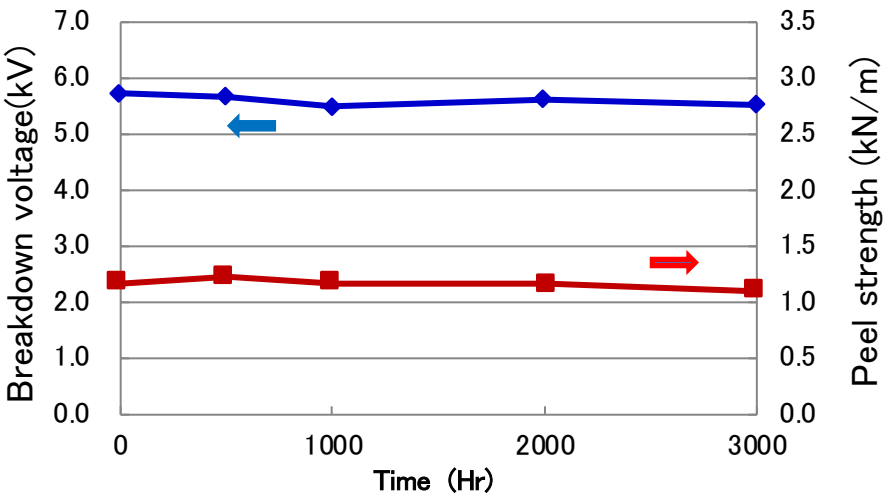
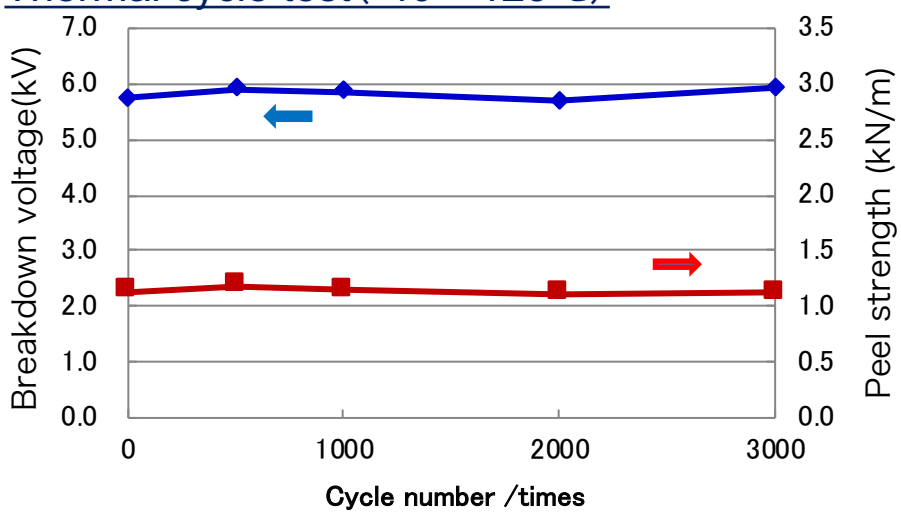
High thermal conductivity mat'ls: AC-7208 (8W/mK)

Product number	AC-7208	
Dielectric layer thickness	120μm	
Thermal conductivity (W/mK)	**8**	Laser flash
Tg (℃)	**270**	DMA method
Peel strength (kN/m)	1.2	1 oz copper
Solder limit (sec)	Over60	260℃
CTE (ppm/℃)	9/22	α_1/α_2
Breakdown V (kV)	**> 5**	JIS C2110
CTI	over600	IEC method
Flammability	V-0equiv.	UL94

High temperature long term test (@175℃)



Thermal cycle test (-40⇔125℃)



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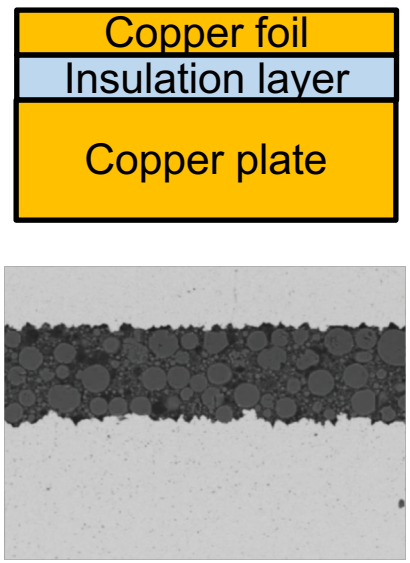
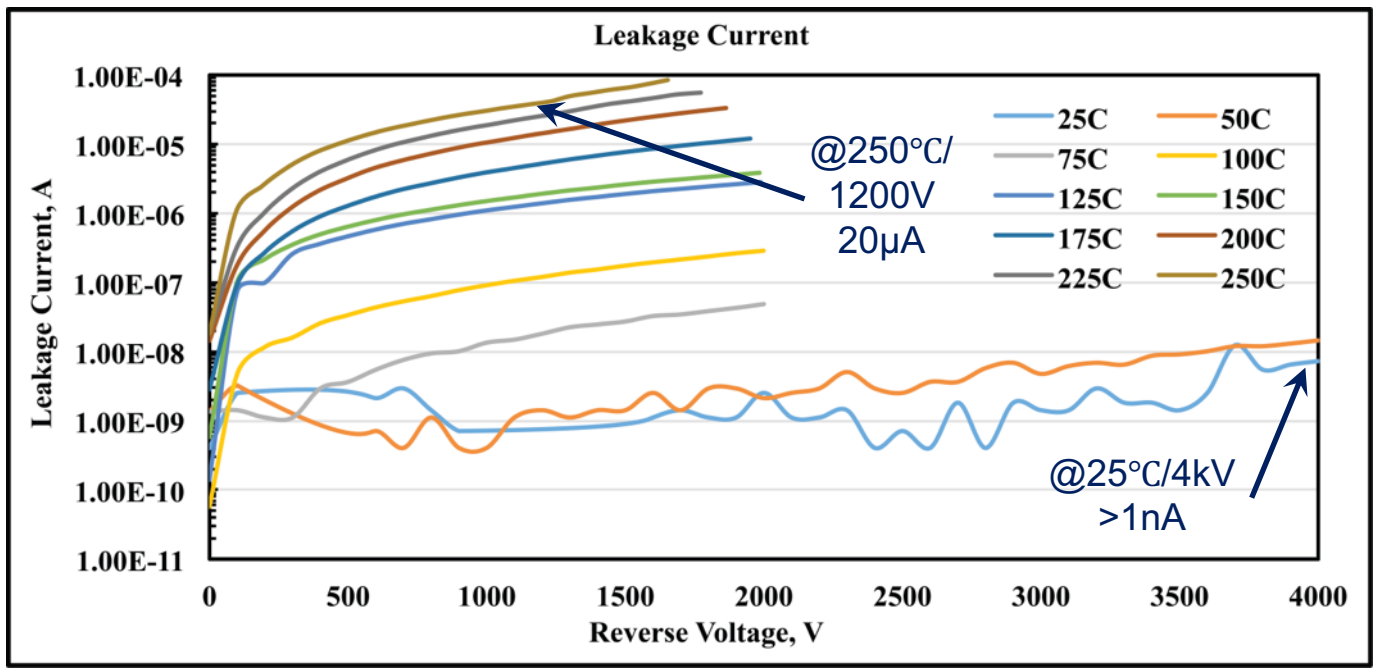
High voltage capability: CC-7208 (8W/mK)

"Novel Polymer Substrate-Based 1.2kV / 40A Double-Sided Intelligent Power Module," Xin Zhao, et.al., IEEE 67th ECTC –Orlando, FL, USA

Characterization of Leakage Current v. Temperature





Limited leakage current is measured on the 80 μm sample with copper bonded on both sides

- 20 μA leakage even at 250°C with 1200 V voltage applied
- 1 nA leakage at room temperature with > 4kV voltage applied

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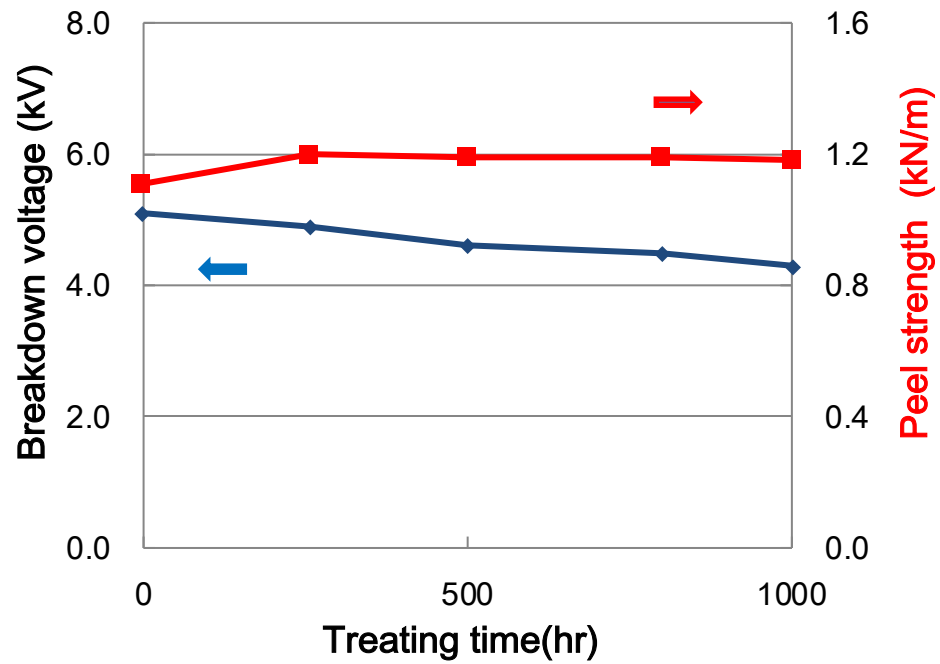
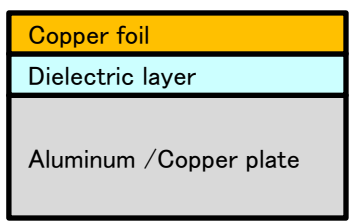
High thermal conductivity mat'ls: AC-7210 (10W/mK)

PROPERTIES

Product number	AC−7210	
Dielectric layer thickness	120 μ m	
Thermal conductivity (W/mK)	10	Laser flush method
Tg (℃)	270	DMA method
Peel strength (kN/m)	1.2	1 oz copper
Solder limit (sec)	60＜	260℃
CTE (ppm/℃) α1	14/14/14	X/Y/Z
Breakdown V (kV)	>5	JIS C2110
CTI	>600	IEC method
Flammability	V−0 equivalent	UL94

High temperature long term reliability(175℃)





CCL: Cu Clad Laminate with metal base (AC-XXXX)

RISHO

APEC®

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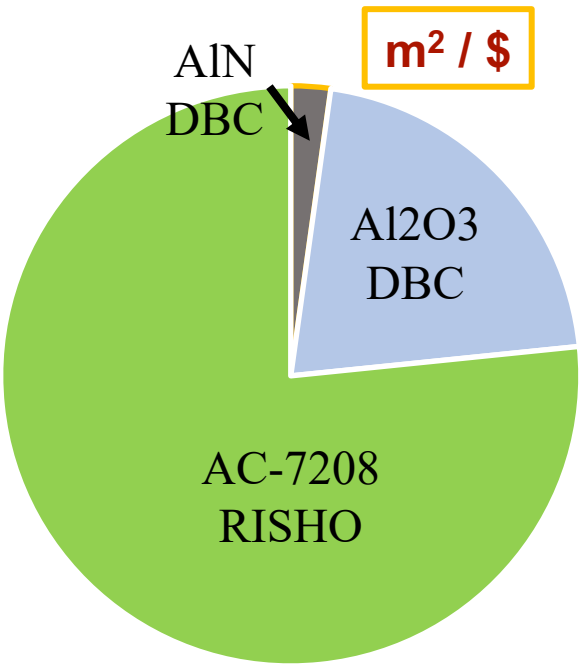
$$$ Cost (Material by RISHO KOGYO Co. Ltd.)

Products	Manufacturer	Price (circa 2018):
AC-7200TY	Risho	\$154 / m^2 1oz Cu and 1mm Al
AC-7208	Risho	\$170 / m^2 1oz Cu and 1mm Al
CS-3295	Risho	\$175 / m^2 0.5oz Cu and 0.4mm Al

AC-7208 (Risho)	\$170 / m^2	1oz Cu and 1mm Al
Al_2O_3 DBC	\$1628 / m^2	0.3mm Cu with 0.635mm Al_2O_3
AlN DBC	\$5892 / m^2	0.3mm Cu with 0.635mm AlN



Parts	Thickness/ µm	Thermal Conductivity W/m·K	Unit Thermal Conductance W/m²·°C	Cost Estimate \$/m²
Al_2O_3	254	23	0.09E6	1628
AlN	254	170	0.67E6	5892
Epoxy-resin*	**80**	**8**	**0.1E6**	**170**

RISHO Company Profile
Founded: October, 1921 (~100 yrs)
Annual Revenue: 170M USD
Number of Employee: 740

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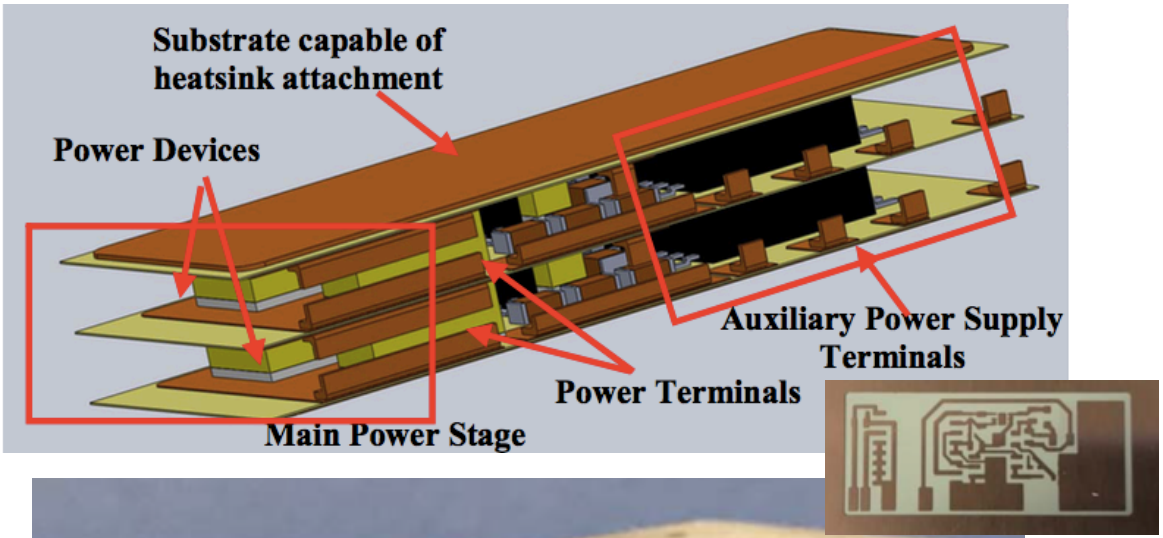
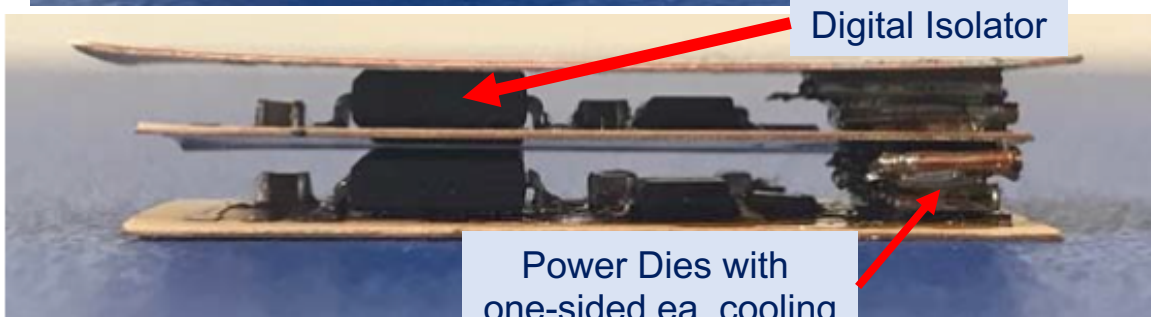
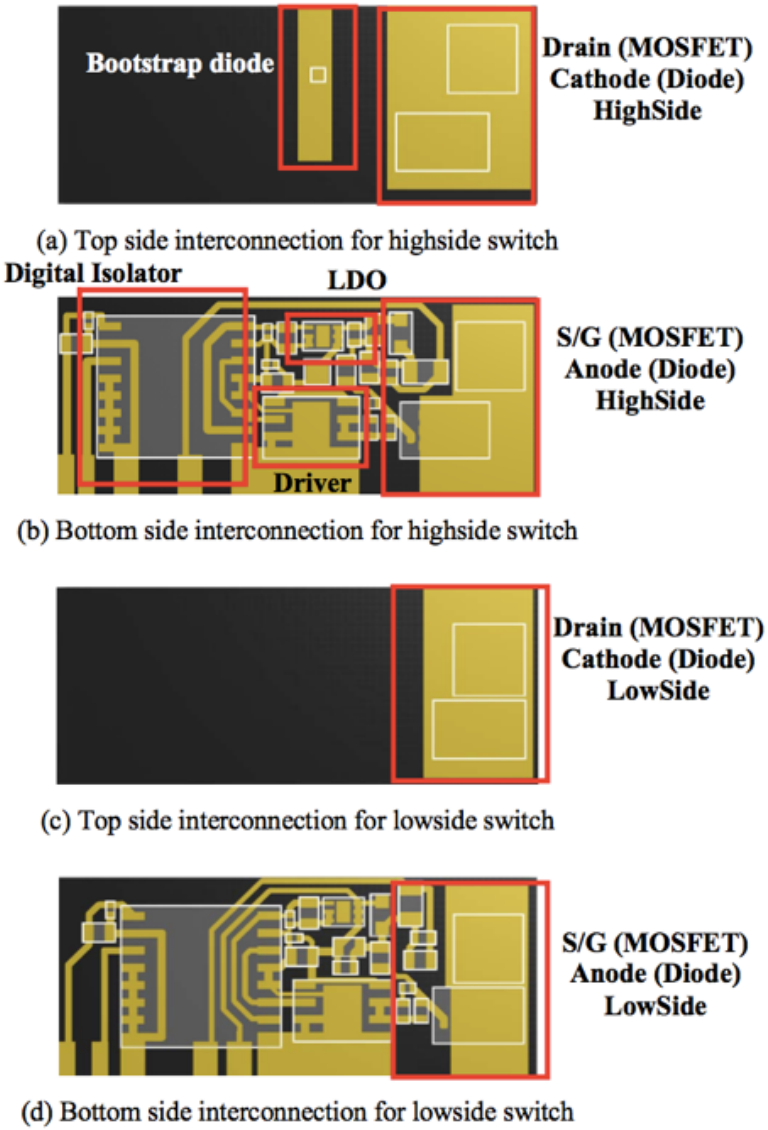
Stacked Power Dies, Driver & Isolator w/ ERCD







(a) Top side interconnection for highside switch

(b) Bottom side interconnection for highside switch

(c) Top side interconnection for lowside switch

(d) Bottom side interconnection for lowside switch

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Monolithically Integrated SiC-Based Four Quadrant Power Switch

"PV Inverter Systems Enabled by Monolithically Integrated SiC based Four Quadrant Power Switch (4-QPS),"
Principal Investigator: Subhashish Bhattacharya; (co-PIs): Jayant Baliga, Douglas Hopkins
Other Contributors (PhD students): Kijeong Han, Aditi Agarwal, Ajit Kanale, Tzu-Hsuan Cheng
Other Contributors (Post-Doc scholars): Bo Gao, Suvendu Samanta

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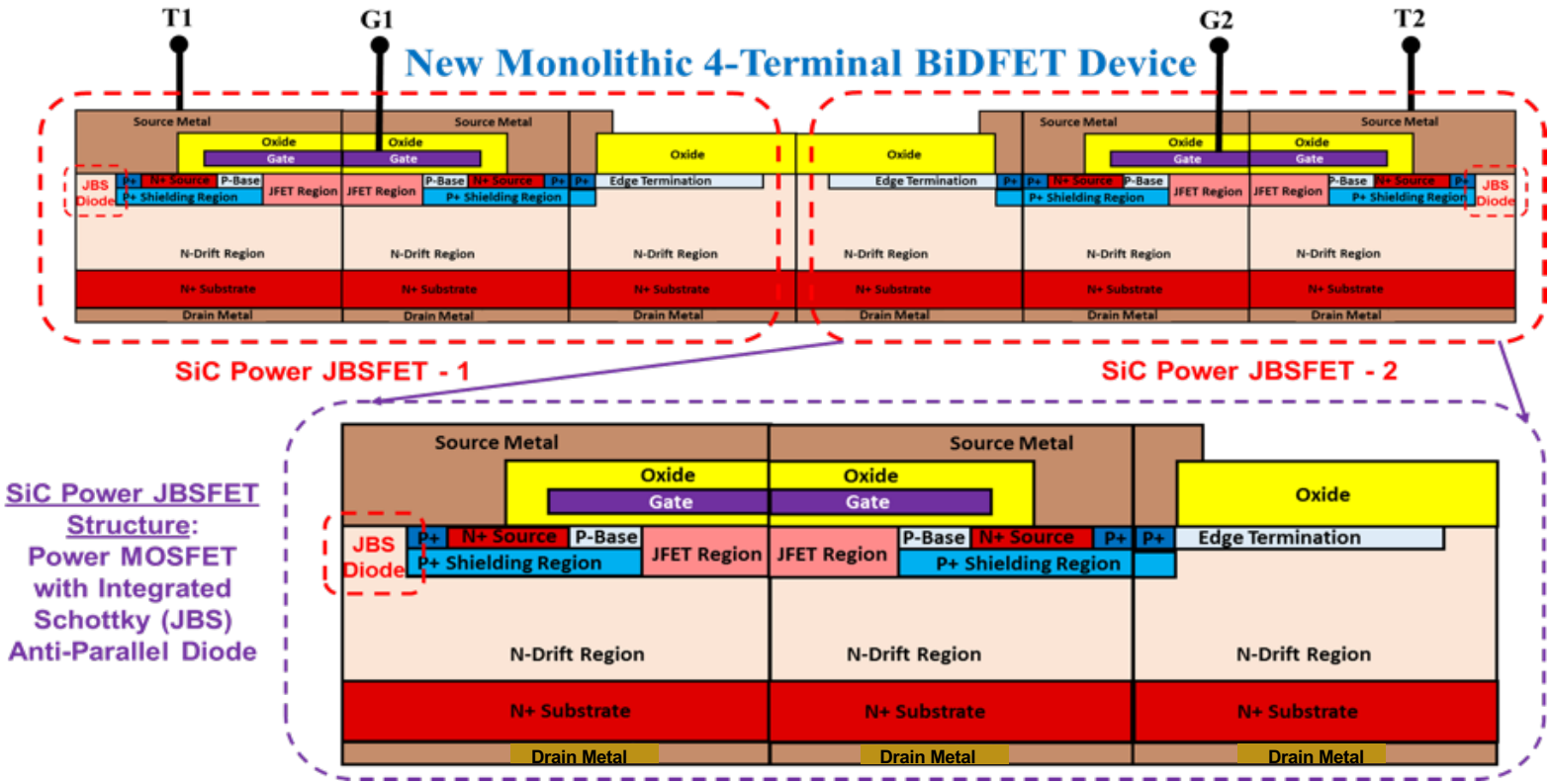
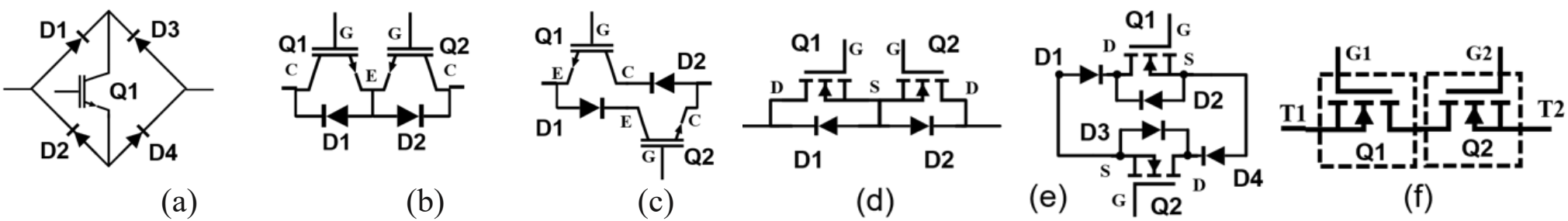
SiC BiDirectional FET– BiDFET





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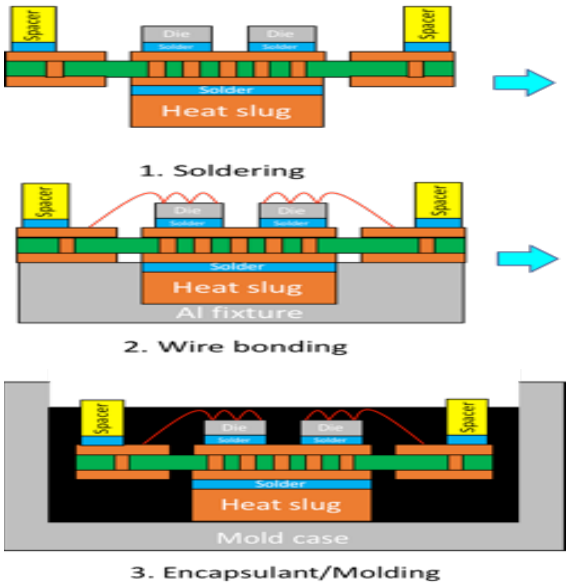
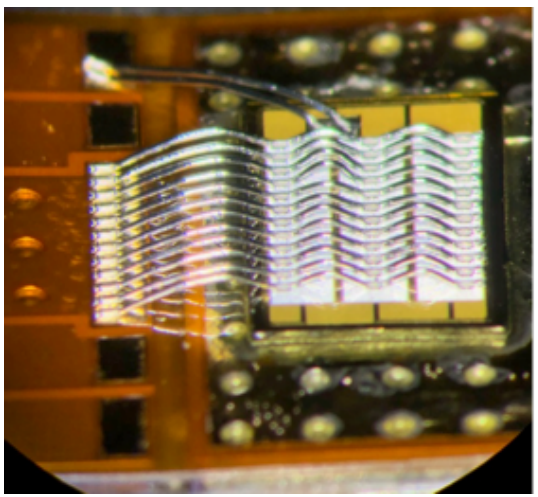
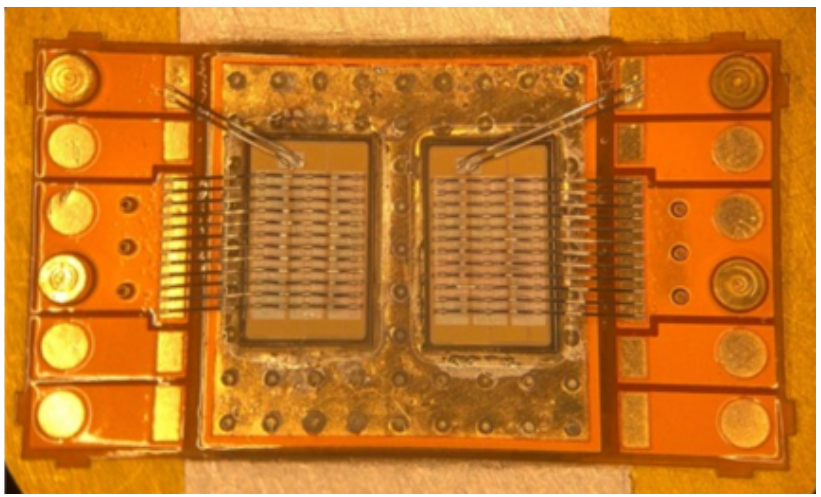
Low Cost Flex in a Low R&L Structure

- For high power applications a low thermal resistance is required to support very high density & lower material costs
- The innovative *Early Stage Package* achieves top-side cooling through an exposed heat slug on the top surface for mounting a heat sink.
- The substrate includes thermal vias and heat slug to minimize thermal resistance of the main thermal path.
- To reduce parasitic package R & L, a twelve 5-mil wire array is bonded to each device with stitch bonding.
- Cu posts are used for thermal and electrical terminals to create an SMD package.







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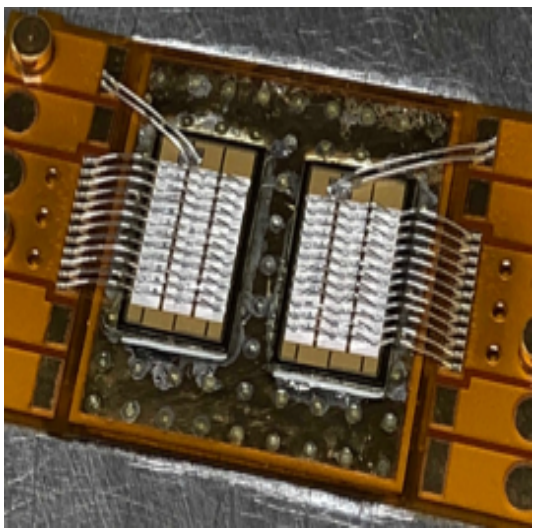
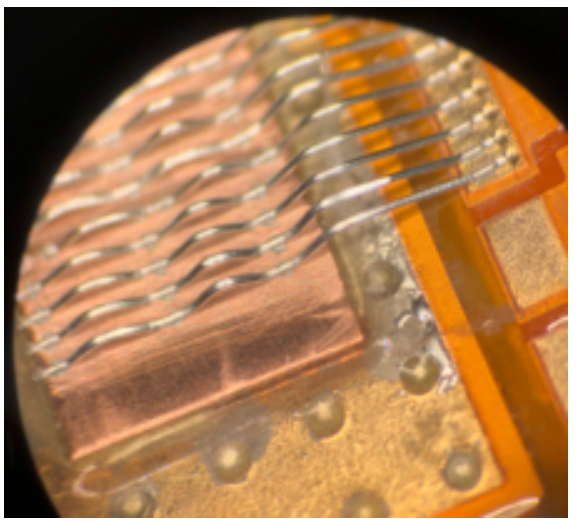
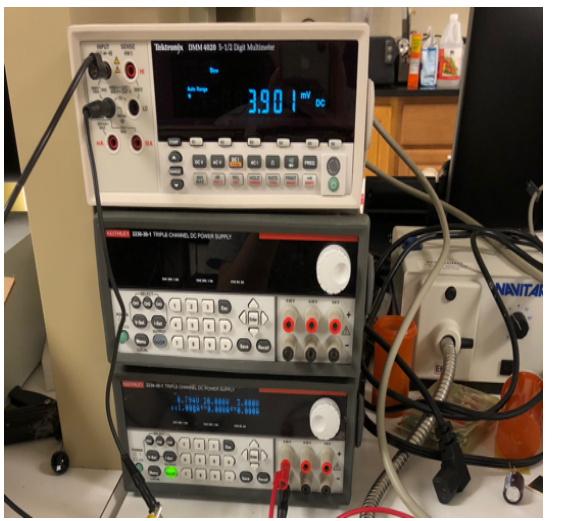
Package Resistance Characterization

- The BiDFET die will have very low internal resistance. Hence, the packaging must be designed and verified to not significantly contribute to final packaged switch resistance
- One resistive element that dominants, is the bonding wires. Layout and asymmetry are also detractors from performance. For R measurement a Cu block replaces devices. <u>The resistance is measurement at 3.9mΩ.</u>



The distributed resistance of packaged devices is 57.5mΩ.





A Cu block replaces the devices and package-only resistance is measurement at 3.9mΩ.

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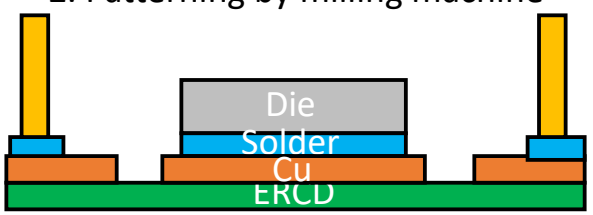
Three Processes for Organic (ERCD) Packages

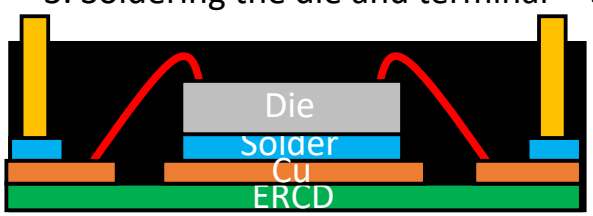
SMD – Insulated Backside

1. Lamination of ERCD based single-layer substrate

2. Patterning by milling machine



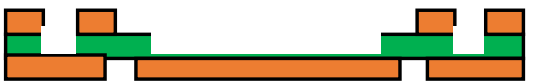
3. Soldering the die and terminal



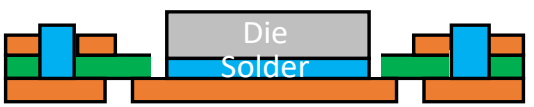
4. Wire bonding and Molding

SMD – Conductive Backside

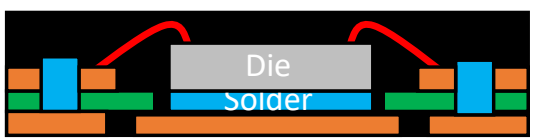
1. Lamination of ERCD based double-layer substrate



2. Patterning by milling machine



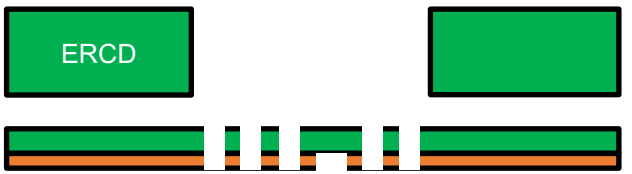
3. Soldering the die and via structure



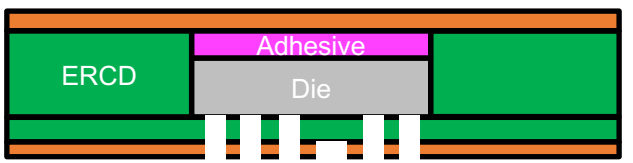
4. Wire bonding and Molding

Bondless Double-Sided High Performance Package

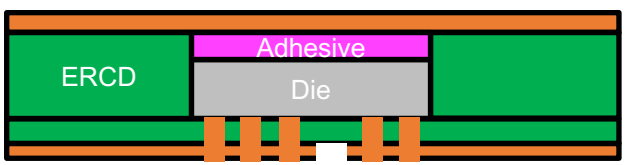
1. Die bonding



2. Formation of ERCD layers



3. Lamination



4. Via plating

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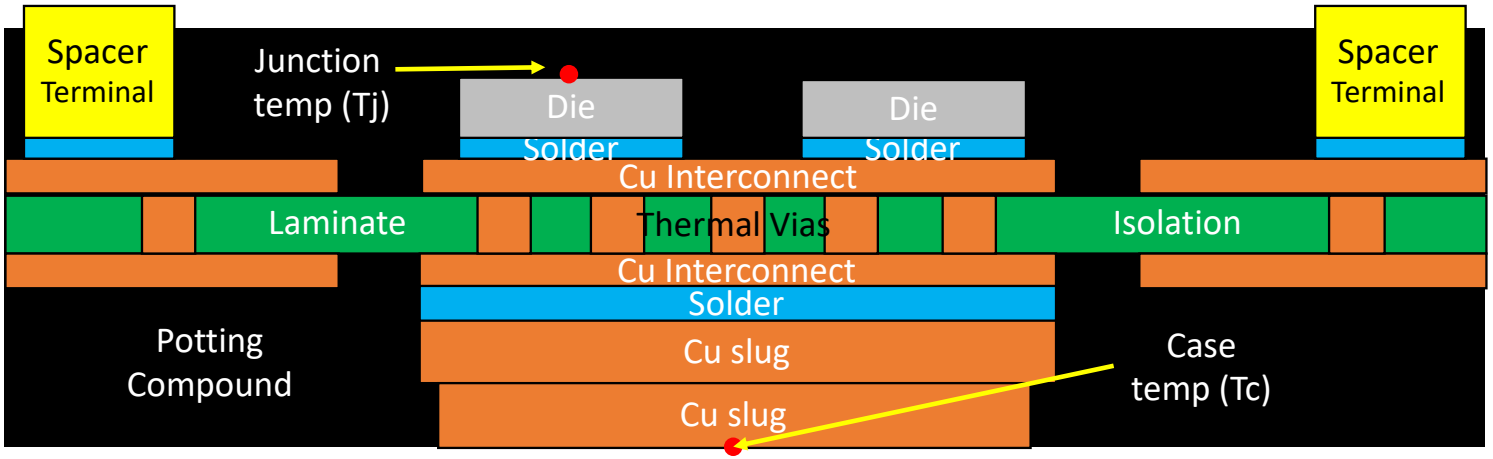
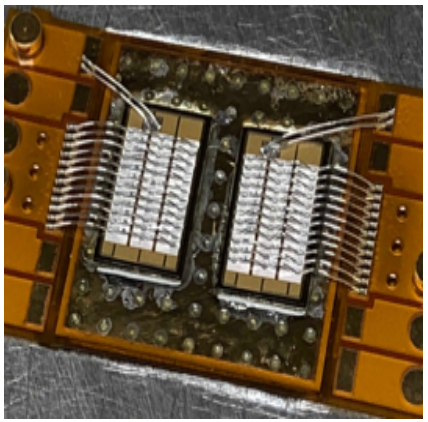
Thermal Analysis of Packaged Dual Die

A dual-die package emulates the monolithic BiDFET packaging approach, and is analyzed for thermal performance and suitability for full power testing. (wire bond connections are not shown).





Organic embedded component package for thermal simulation

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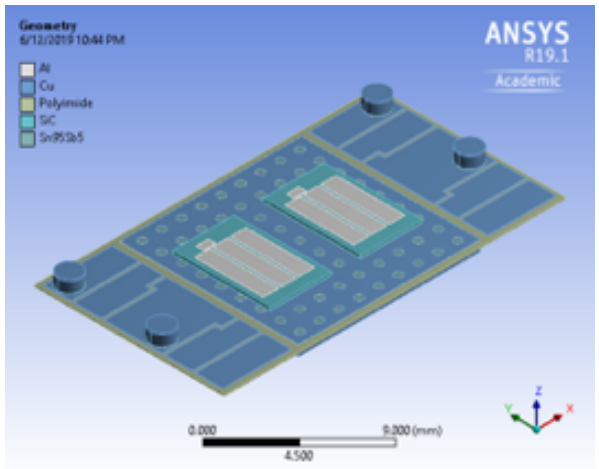
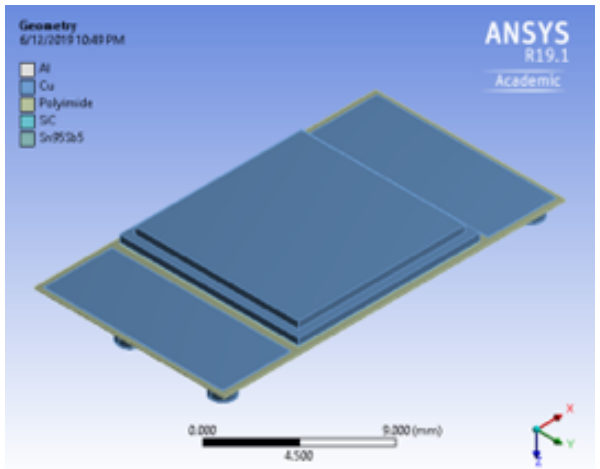
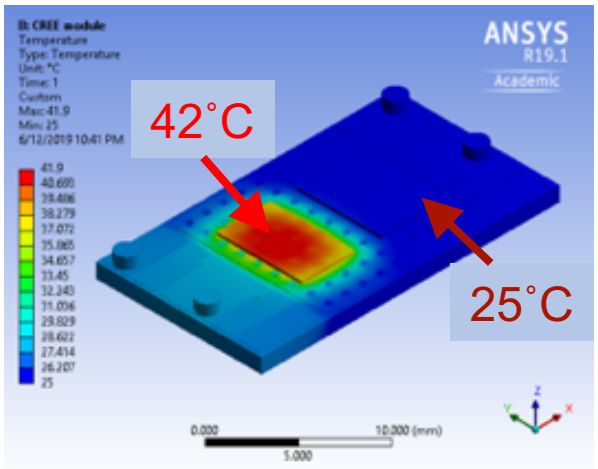
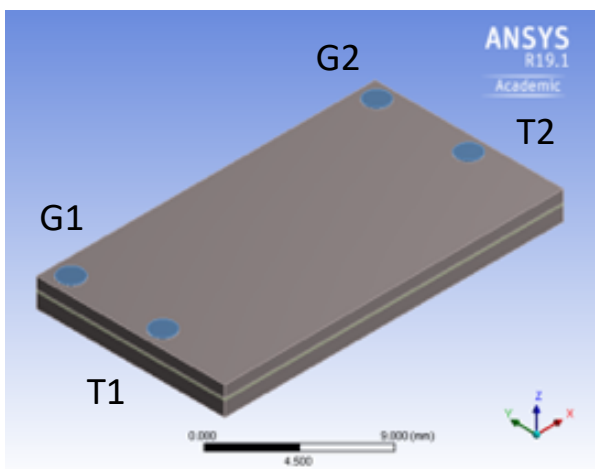
ANSYS Thermal Analysis of Dual Die Package

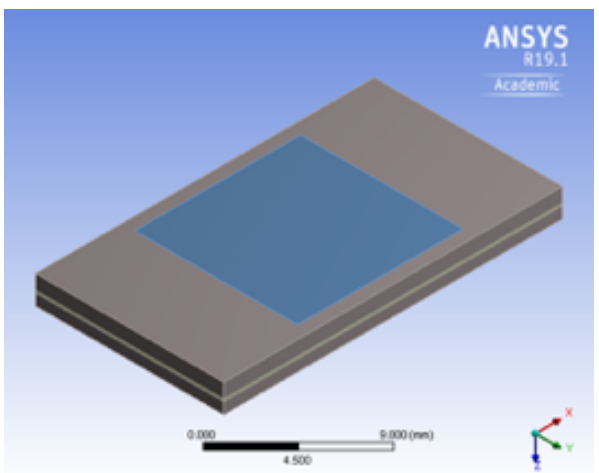
One die is heated at 10W/die with case at 25˚C. Result is Delta 17˚C or 1.7˚C/W

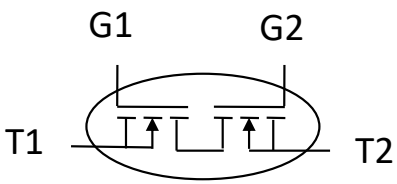












Boundary conditions:

- Steady state thermal analysis
- Input power is 10 Watt on one die
- Case temperature (Tc) is fixed at 25˚C

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Thermal Analysis of Near-Term Package-Dual Die

The results show the thermal resistance and max allowed current.

The thermal resistance junction-to-case is:

$R_{jc} = \frac{T_j - Tc}{P} = \frac{41.9-25}{10} = 1.69\ K/W$

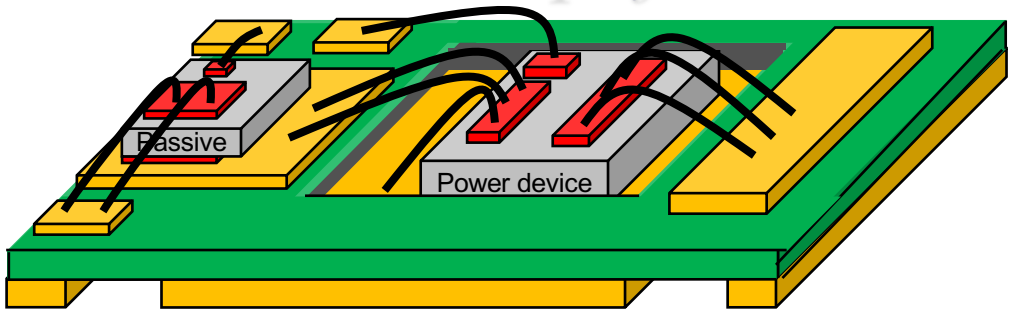
The maximum allowed power dissipation at 25 ˚ C is:

$P_{tot} = \frac{T_j - Tc}{R_{jc}} = \frac{175-25}{1.69} = 88.76\ W$

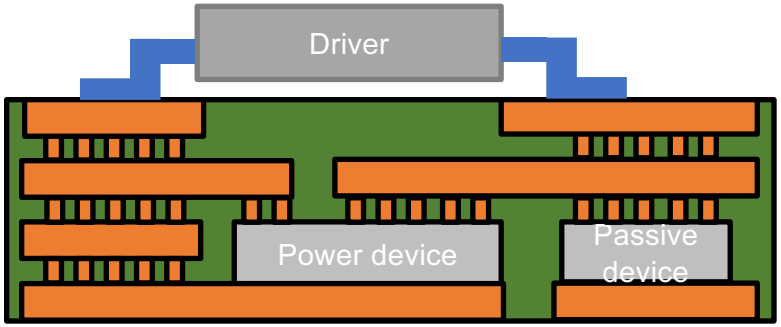
The maximum continuous drain current from data sheet (CPM2-1200-0025B) at 175˚ C is:

$I_D = \sqrt{\frac{T_{j,max} - Tc}{R_{jc} * Rds_{,on}\,(@\,Tj_{,max})}} = \sqrt{\frac{175-25}{1.69 * 0.052}} = 41.31\ A$

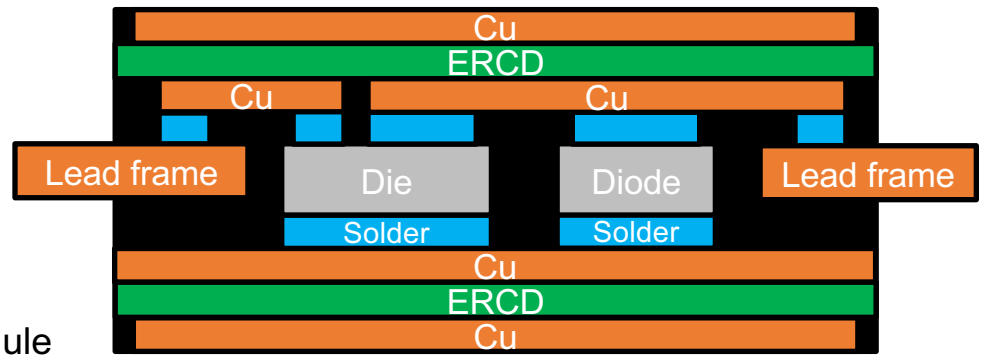
Advanced Concept for Double Sided Cooling



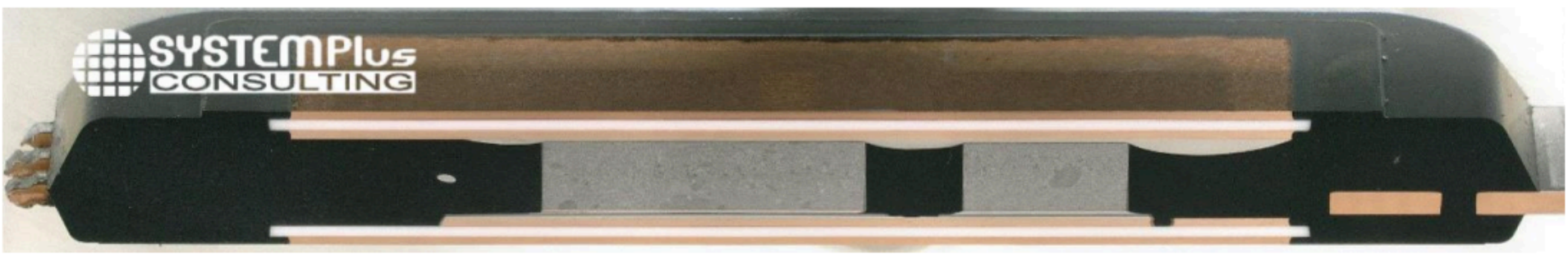
Wire bond version



Wire bond-less version



Infineon FF400R07A01E3 Double Side Cooled IGBT Module
(Infineon's first double sided cooling power module for automotive)



Ref: https://www.autonomousvehicletech.com/articles/1497-infineons-dual-sided-power-module-for-electric-vehicle-systems

Ref: https://www.systemplus.fr/wp-content/uploads/2018/01/SP18375_Infineon_double_side_cooling_IGBT_flyer.pdf

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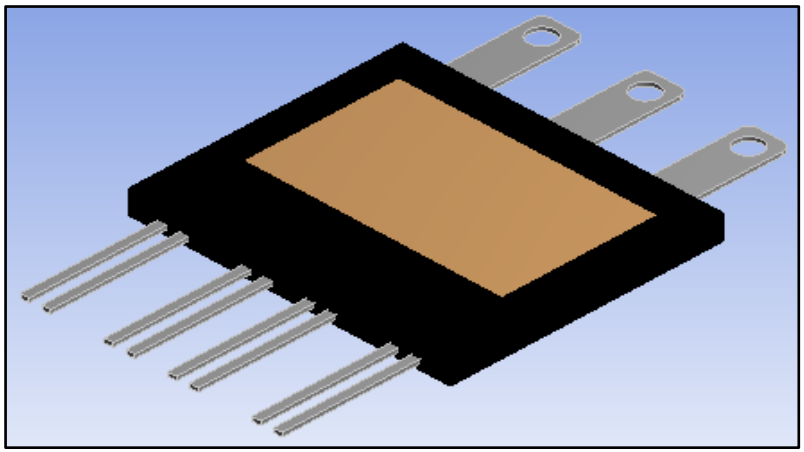
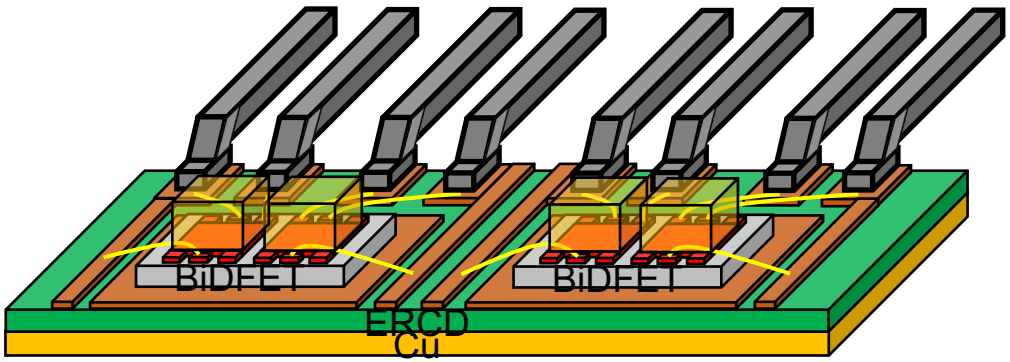
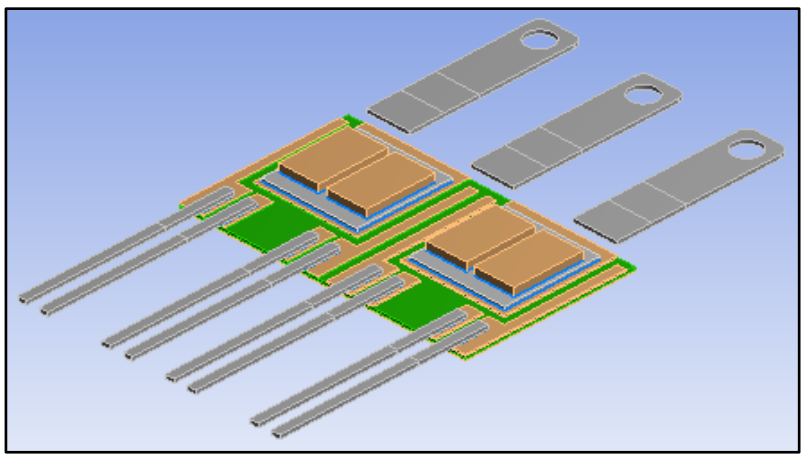
Initial Half-Bridge Design

Module Details:

- Half-bridge power module
- Kelvin source connections
- Double sided cooling THD PKG
- Dual 10 W/mK 120um ERCD substrates
- 3 power terminals and 8 gate terminals
- BiDFET – BiDirectional FET







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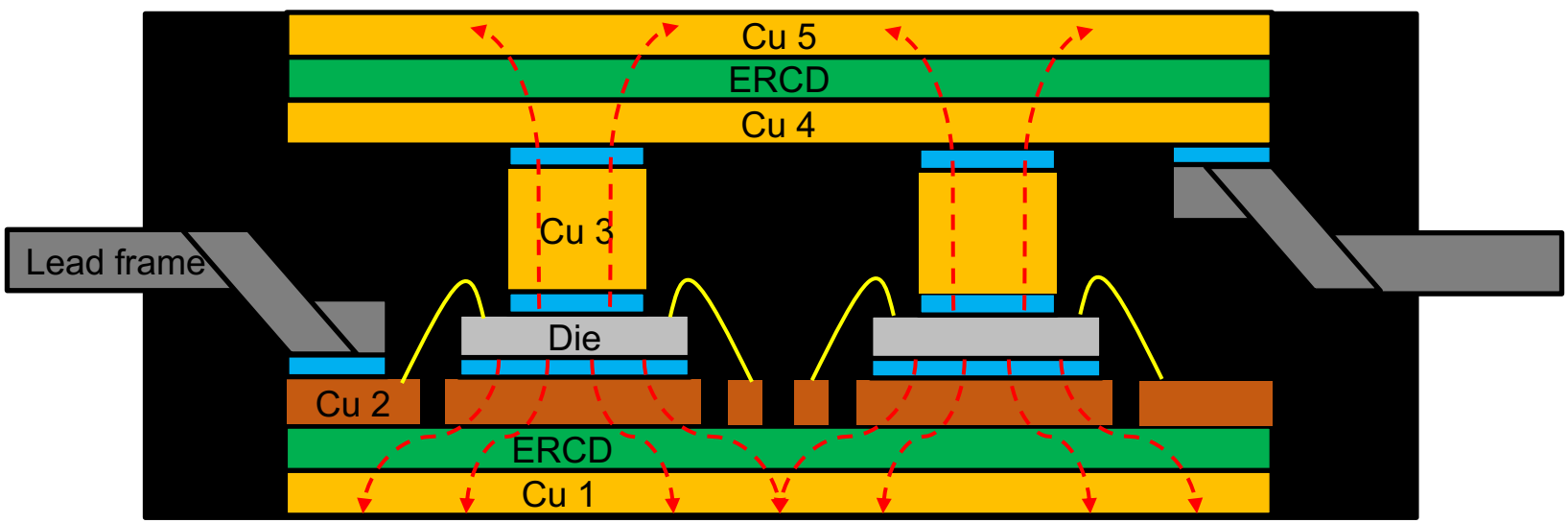
Optimization of Material Selection

Thermal cycling test:

- Infinite heat transfer on top and bottom exposed Cu pads
- Heat sources on die surface

Thermal resistance:

$$R_{jc} = \frac{T_{j,max} - T_c}{P}$$



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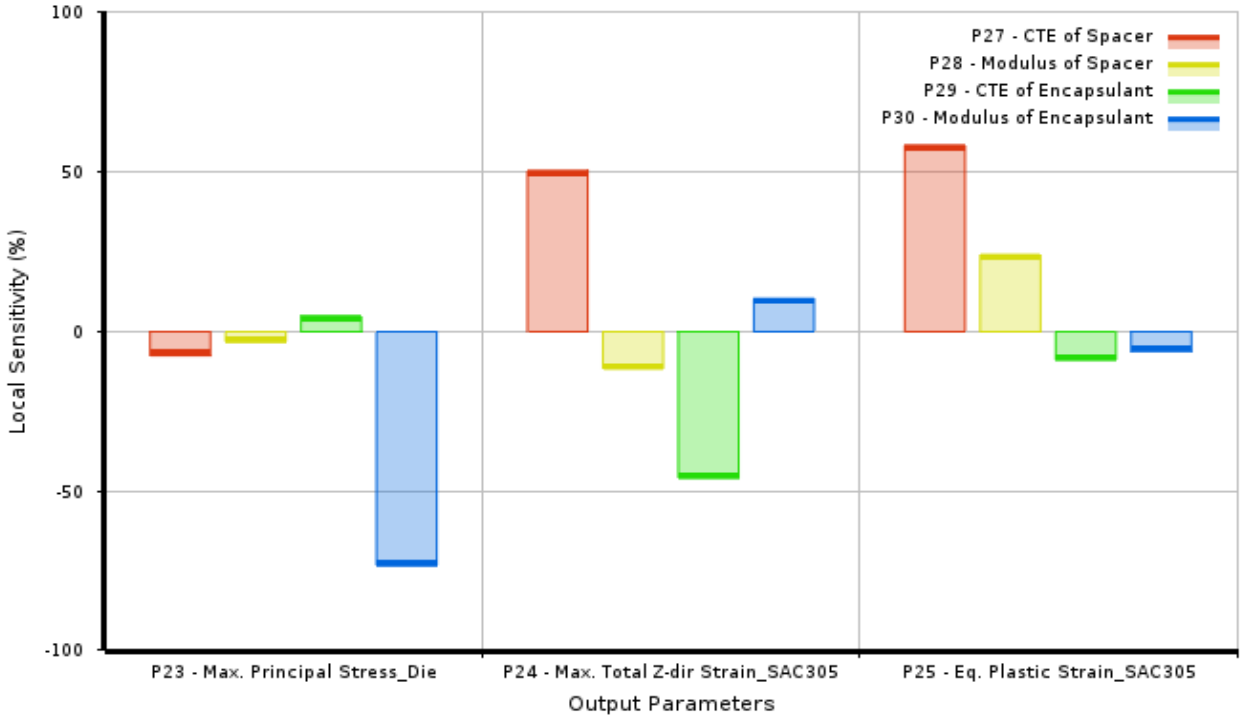
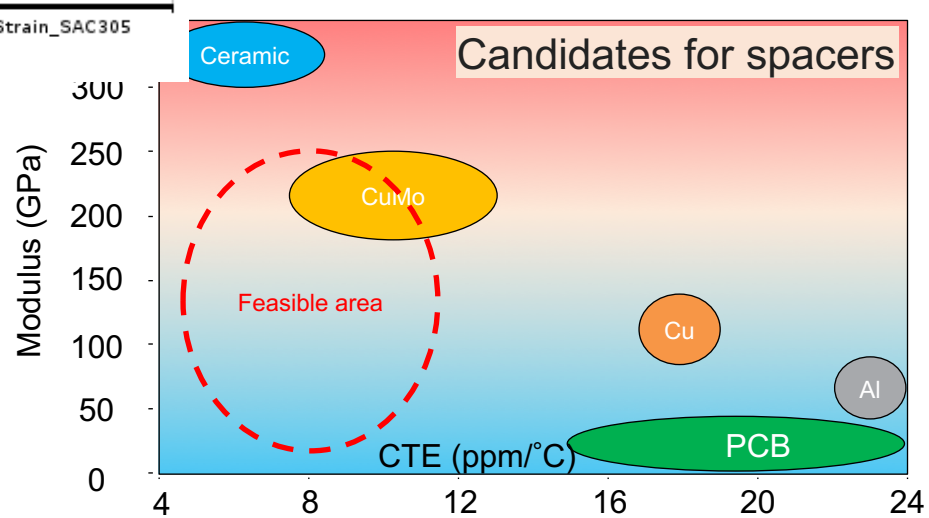
PACKAGING RESEARCH IN ELECTRONIC ENERGY SYSTEMS

Optimization of Material Selection



- The best candidate for a spacer is characterized by the optimization of material selection.
- In geometric optimization, the thickness of spacer is the most sensitive factor for both mechanical and thermal performance.



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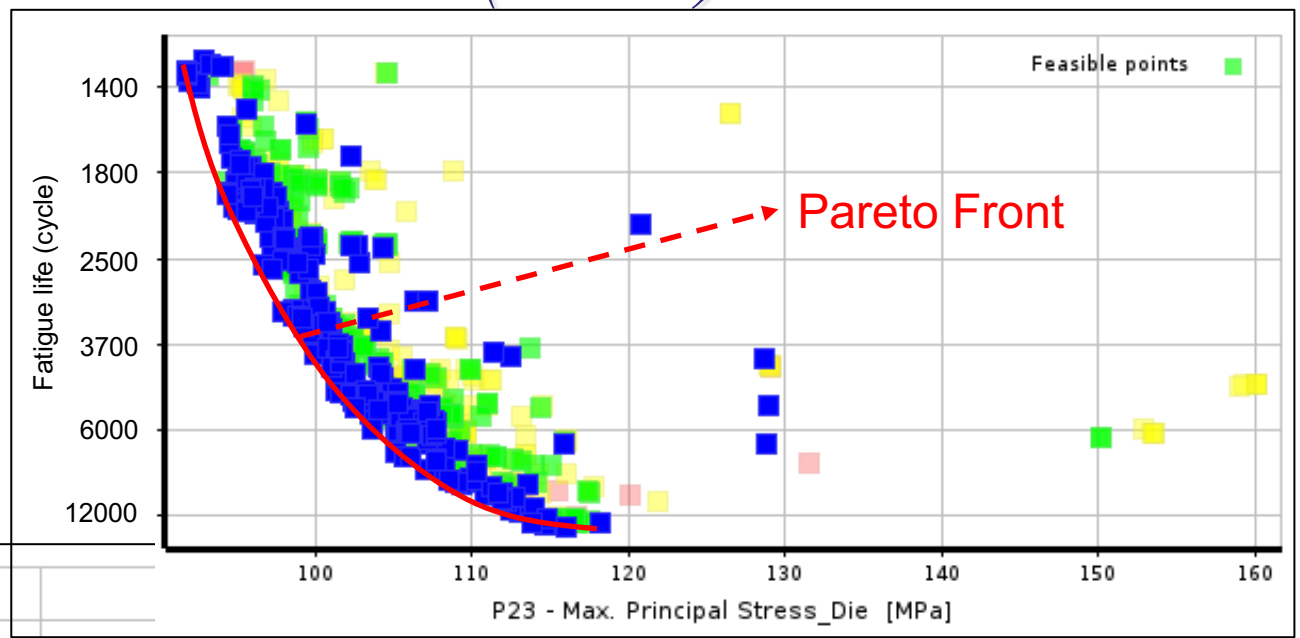
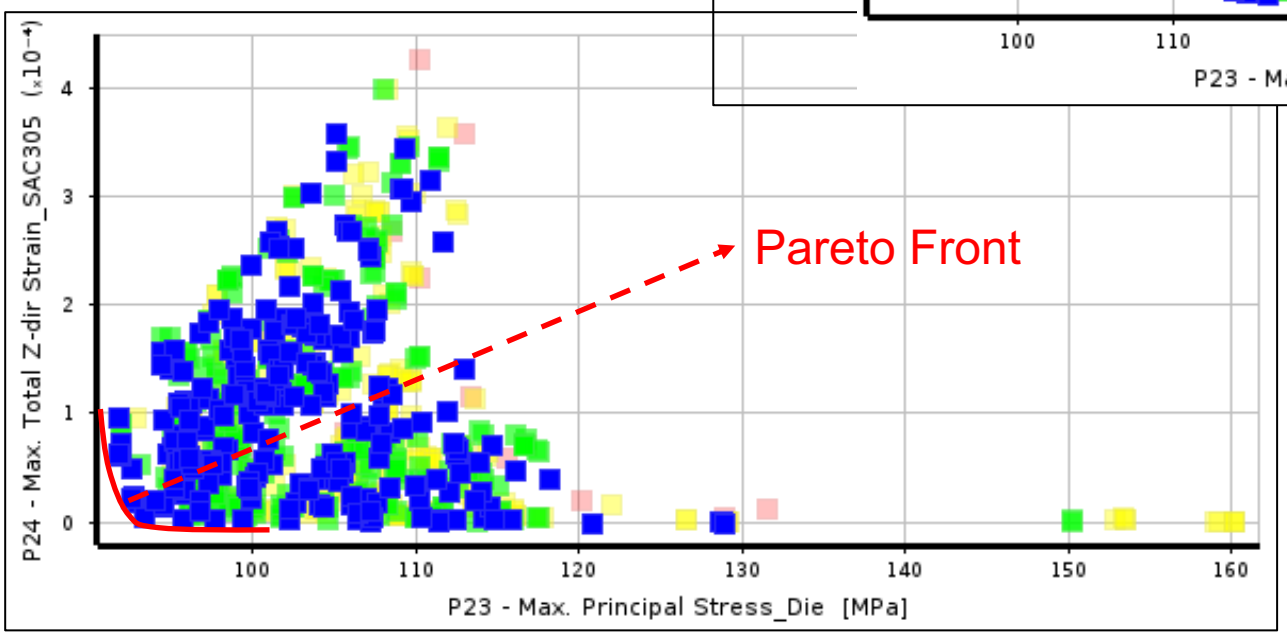
Optimization of Material Selection (con'd)





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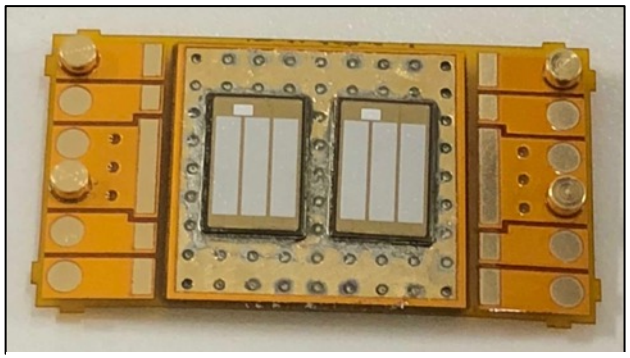
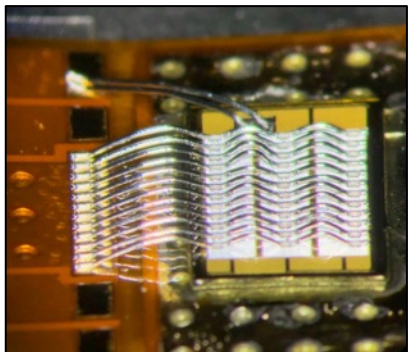
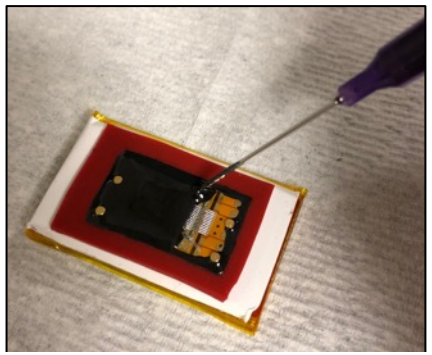
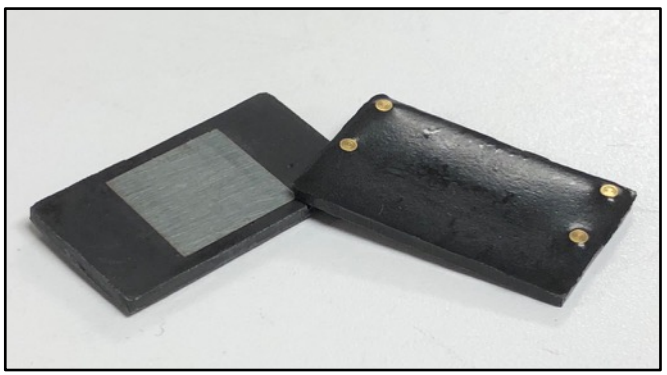
Results with Discrete Die

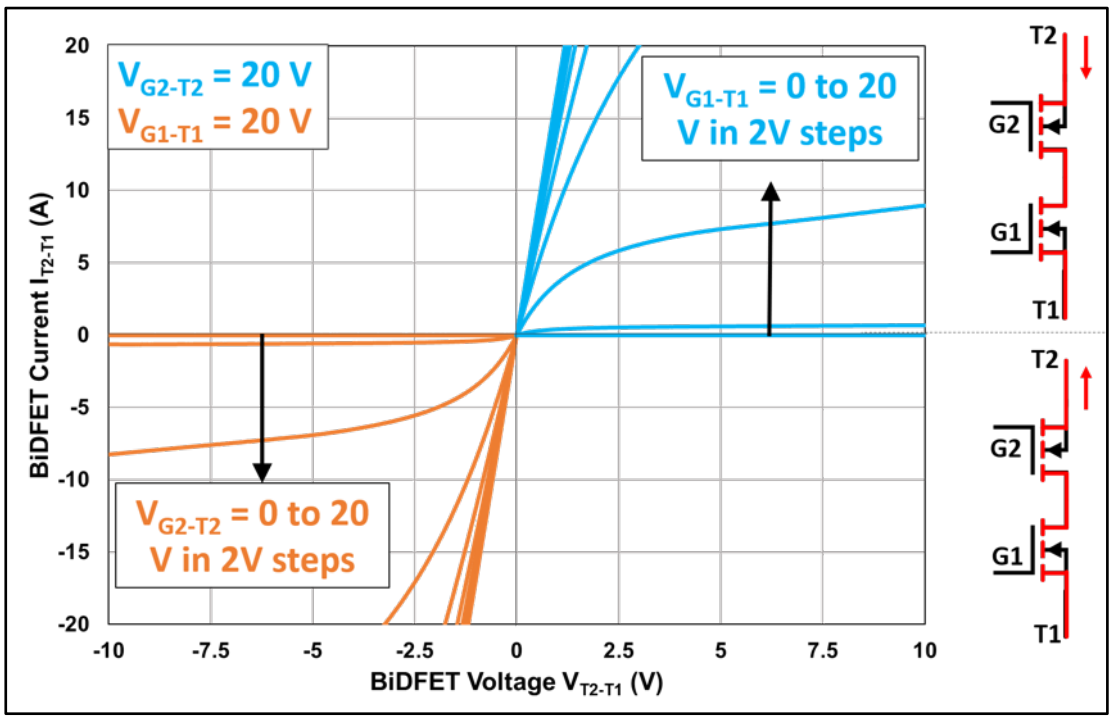








- **Module Details:**
- ✓ Two bare die SiC Power MOSFET chips used (CREE CPM2-1200-0025B – 1.2kV, 25 mΩ)
- ✓ Top sided cooling SMD PKG
- ✓ Package encapsulated to create a 4-terminal module
- ✓ Two high-voltage terminals (T1 and T2) and two control terminals (G1 and G2)



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THANK YOU

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Acknowledgements

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PowerAmerica

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