PSMA

Au cœur de l'efficacité énergétique

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Full 3D advanced packaging concepts for Wide Bandgap Power Electronics

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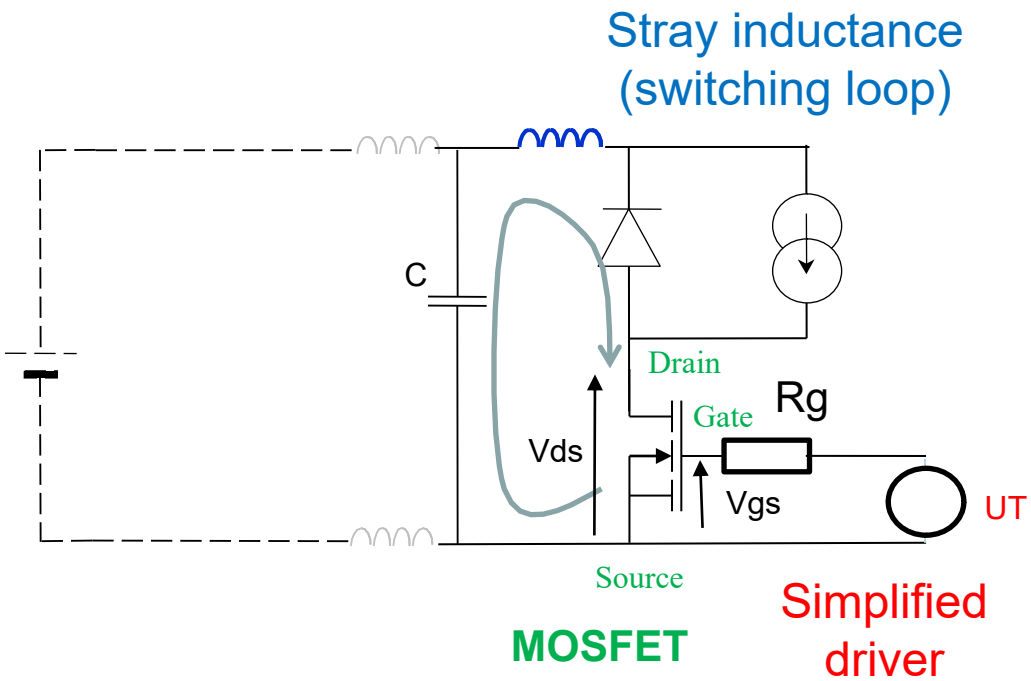
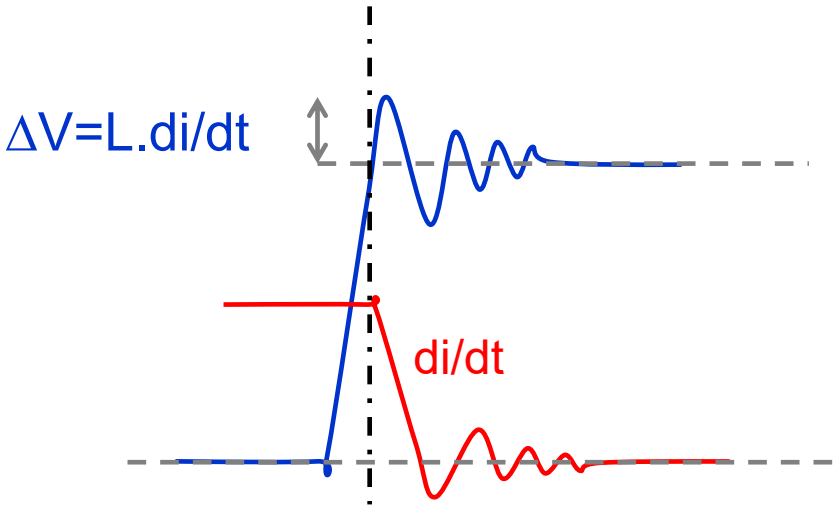
Outline

1. **Electromagnetic limitations of packaging for high speed devices**
2. **Power Chip on Chip concept (PCoC)**
   - Principle
   - Application to SiC
   - Application to GaN
3. **compacT and modulAr Power modules with IntegRated cooling (TAPIR)**

1. EM limitations of packaging

Voltage overshoot

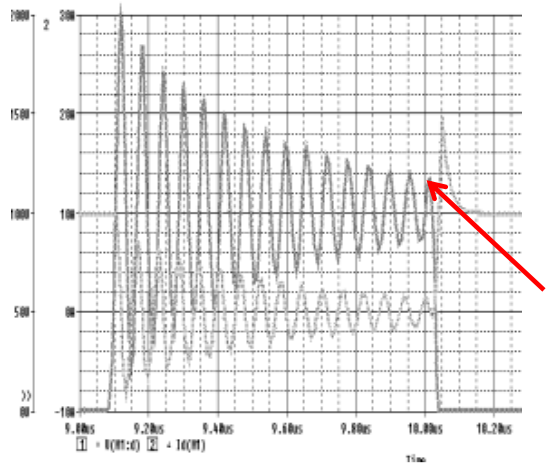




Nano- or Subnano-henry requirements

1. EM limitations of packaging

Power ringing: Lstray+Coss

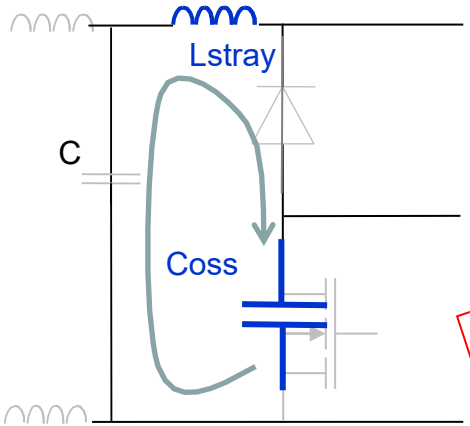


Impact on EMC (localized peak)

May change initial voltage/current thus losses, especially in DCM

Damping factor:

$$z = {}^{R}/_{2} \cdot \sqrt{{}^{Coss}/_{L_{stray}}}$$

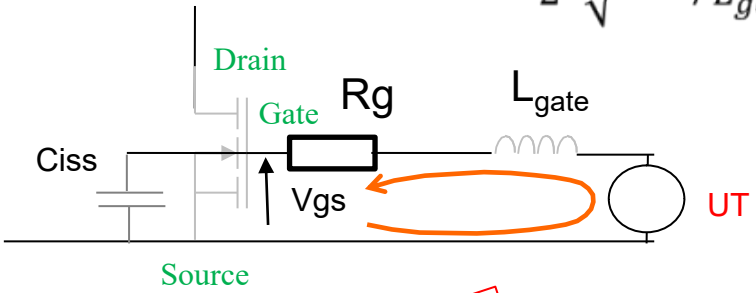


Reducing power loop stray inductance

Gate ringing: Lgate + Ciss

- Generates current oscillations
- Induces shoot through currents in phase leg configurations (false turn off)
- Damage the device (GaN HEMT gate oxide very fragile)

Damping factor: $z = {}^{Rg}/_{2} \cdot \sqrt{{}^{Ciss}/_{L_{gate}}}$



MOSFET

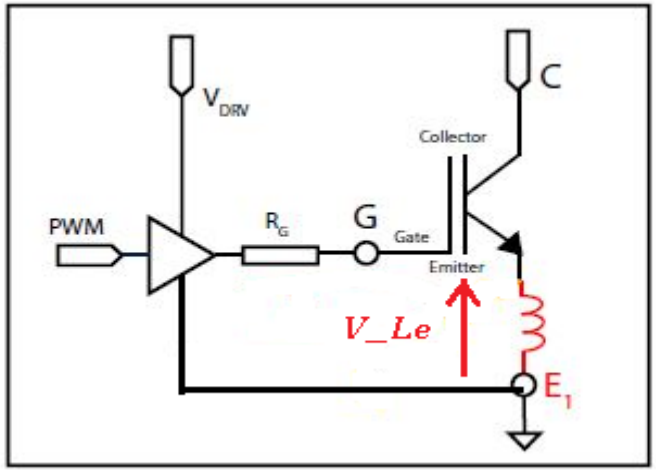
Simplified driver

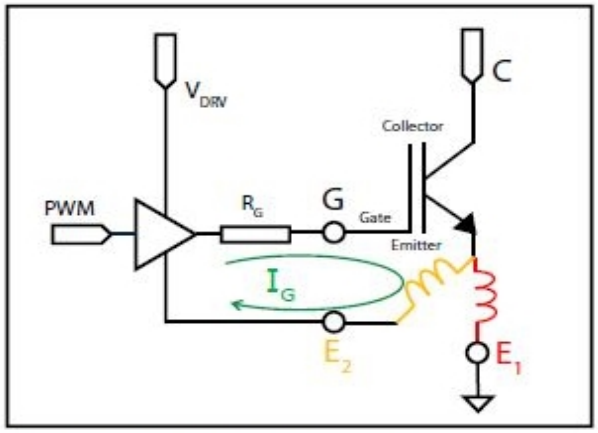
Nano-henry Requirement for gate circuit with small Rg

1. EM limitations of packaging

Gate circuit disturbance – Common impedance

- Induced voltage in the gate circuit → reduces Gate to Source voltage, thus commutation speed.
- Usual solution: Kelvin connection – Does not prevent mutual inductance effect between power loop and gate circuit



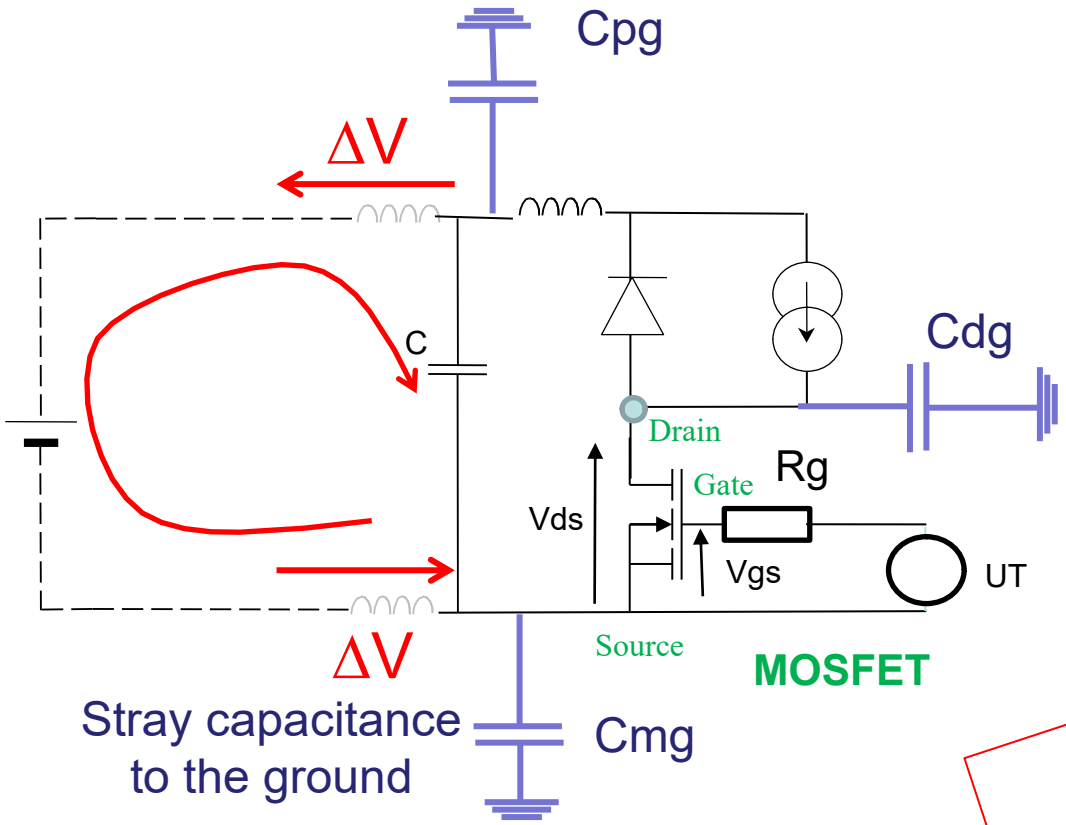


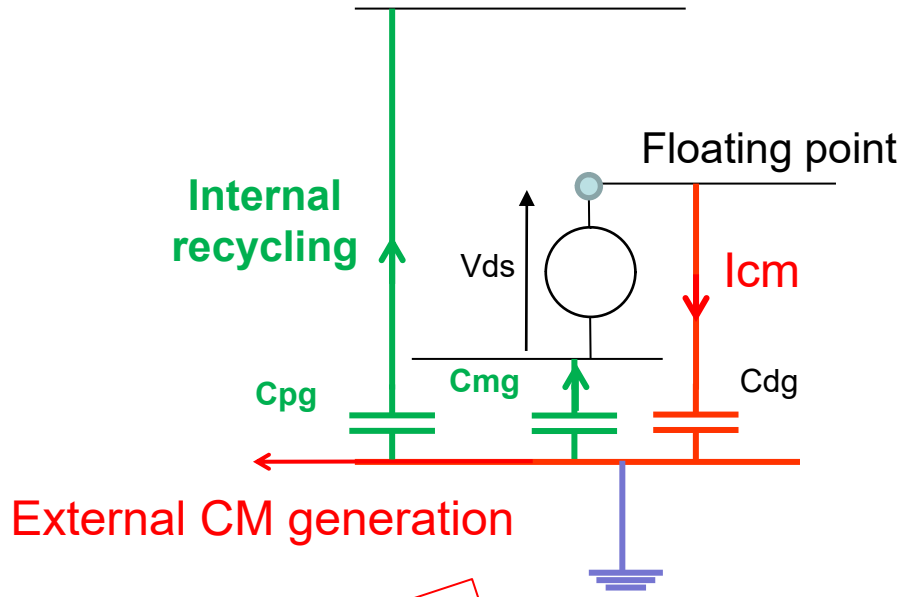
IGBT connection in Kelvin emitter configuration

Separate uncoupled circuits

1. EM limitations of packaging

- **Effect of dV/dt on CM generation (ground currents)**





Reduce Cdg, increase Cpg, Cmg

Keep symmetry (mode coupling)

1. EM limitations of packaging

Summary

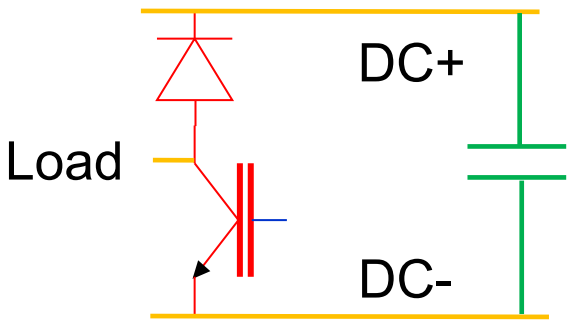
- Do not put a F1 on a forest track !

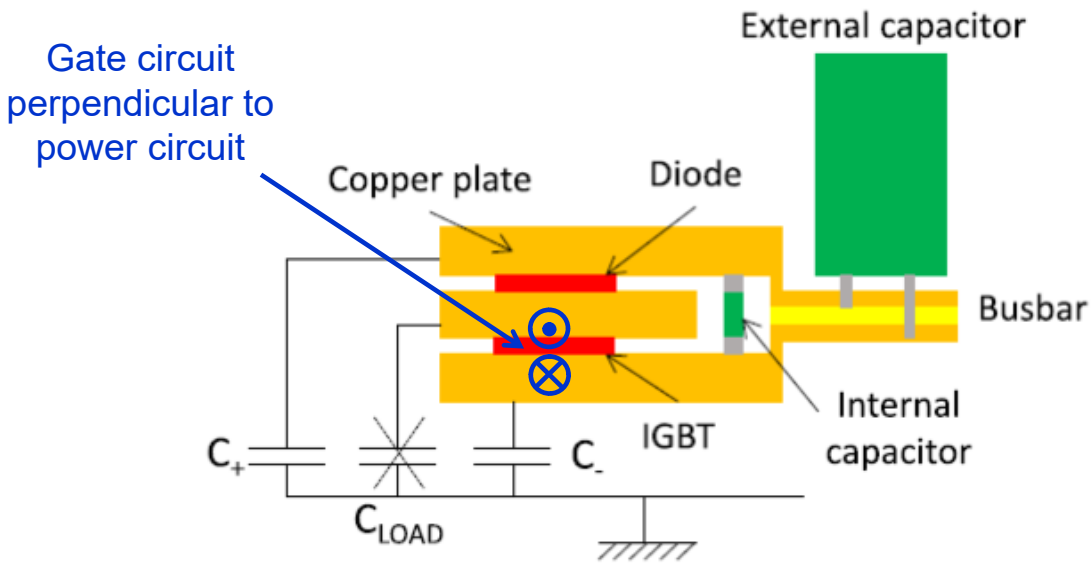
Parameter	Effect	Action
Lstray	Voltage overshoot dI/dt reduction ringing with Coss	Lstray to be reduced: less overshoot, more damping during the ringing
Lgate	Gate ringing with Ciss	Lgate to be reduced: more damping
Ls (and mutual inductances)	Power drive interaction: dI/dt reduction (increased losses) dynamic current imbalance	Reduce Ls and mutual effects
Cpg, Cmg	Common mode current	Should be increased. Keep symmetry to avoid mode conversion
Cdg	Common mode current	Should be reduced

2. Power Chip on Chip Concept

Principle

- 3D integration of the converter for vertical components
- reduction of the stray inductance and of the common mode stray capacitance

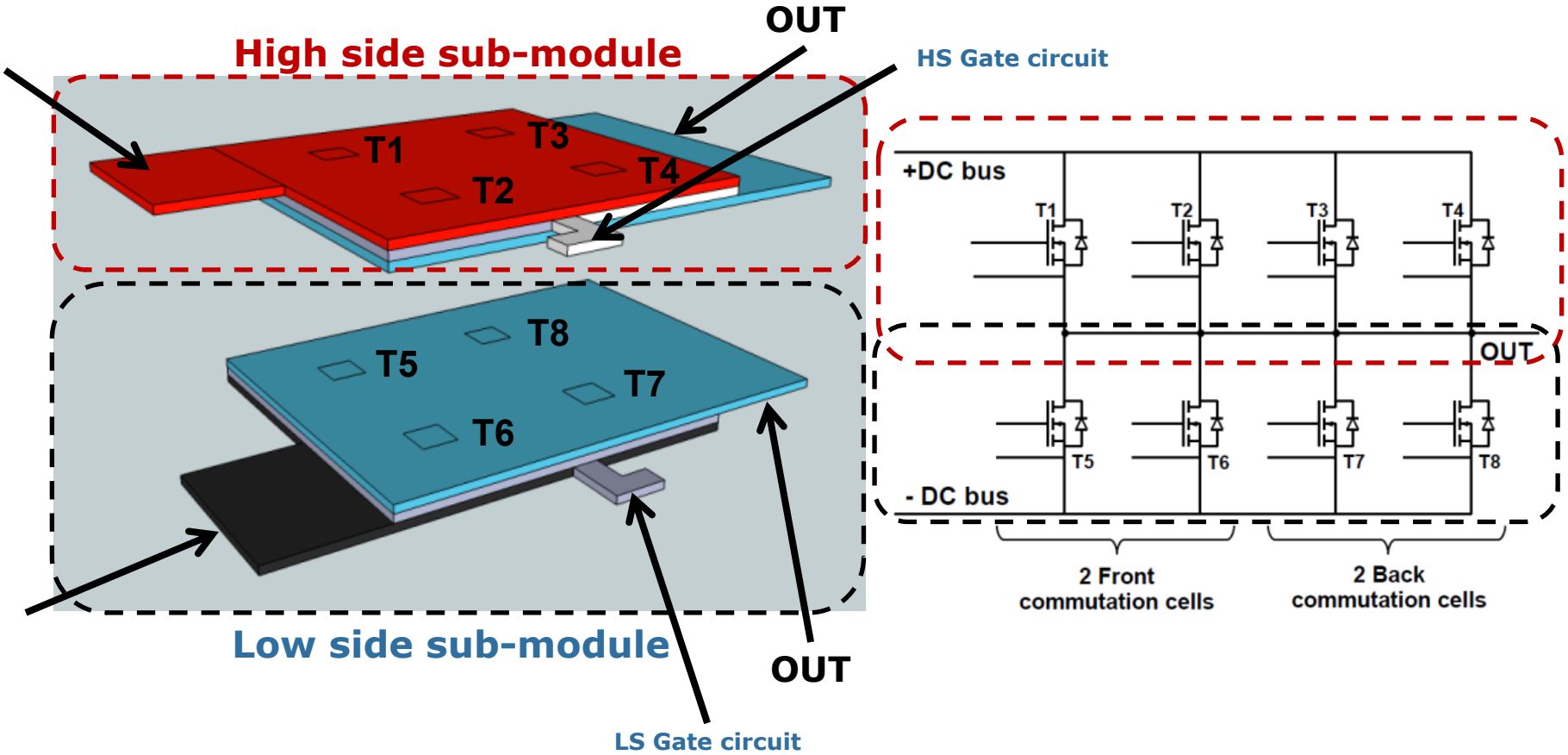




The stray inductance is minimized due to the global integration as part of the busbar itself

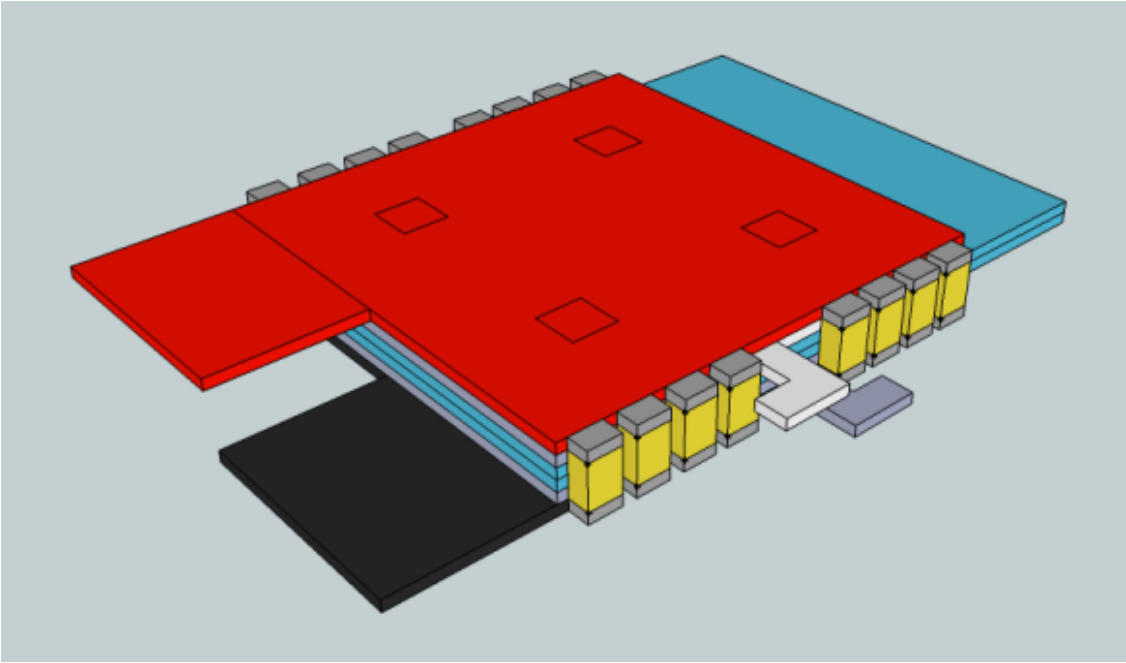
2. SiC Power Chip on Chip

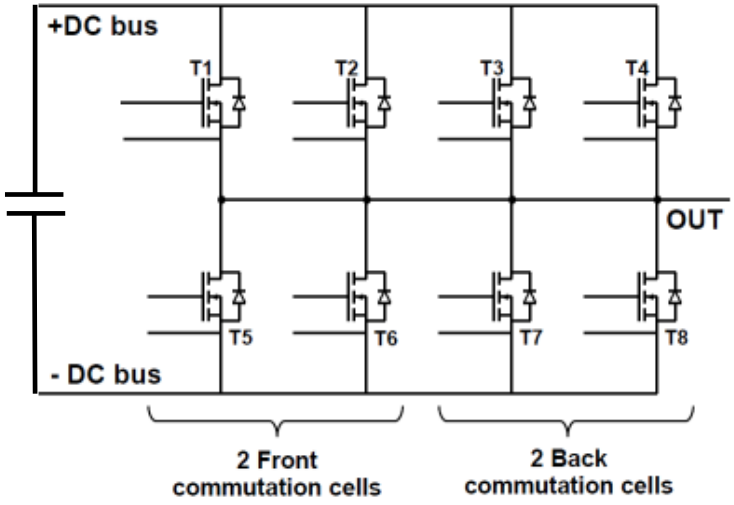
SiC Prototype overview: embedded die process



2. SiC Power Chip on Chip

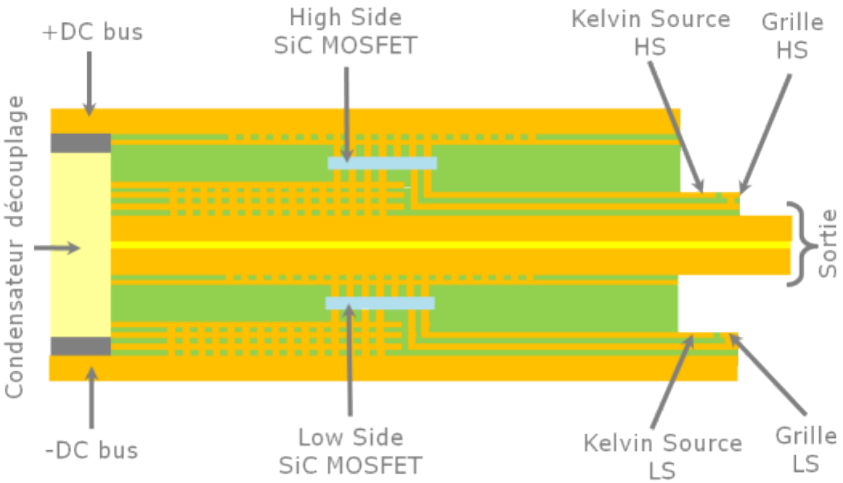
- **SiC Prototype overview: decoupling capacitors**

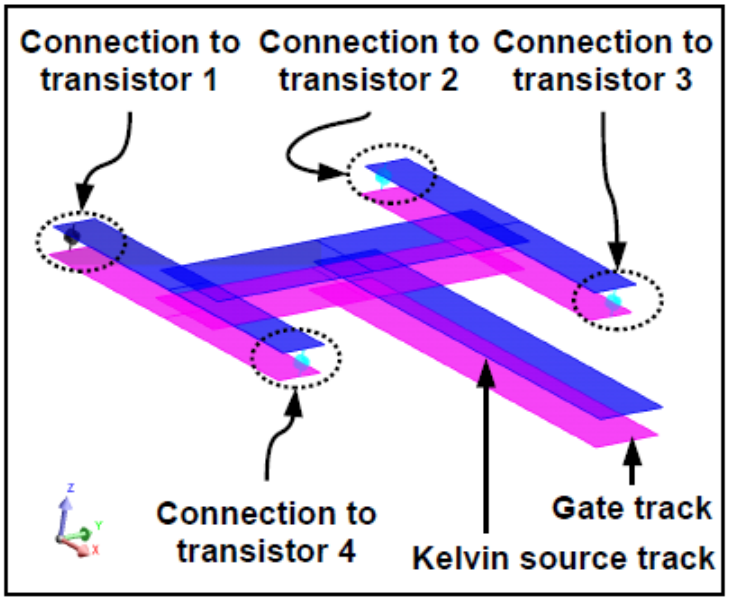




2. SiC Power Chip on Chip

SiC Prototype overview: gate circuit





Source connection:

Kelvin source connection => Common source inductance negligible

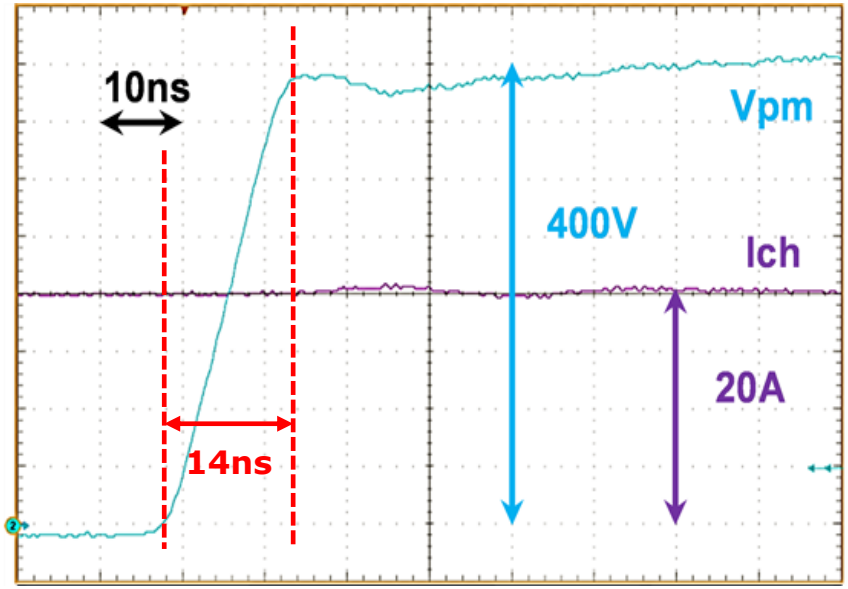
Gate circuit = Bus-bar layout :

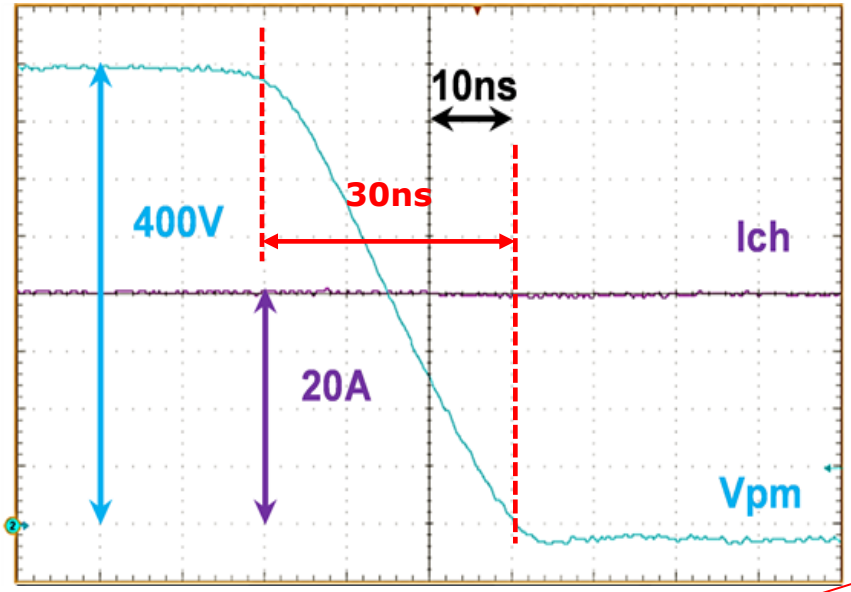
Low value of stray inductance

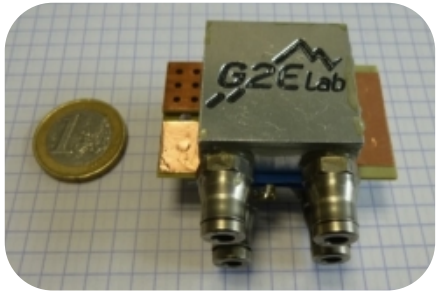
Very low mutual coupling between gate circuit and power circuit

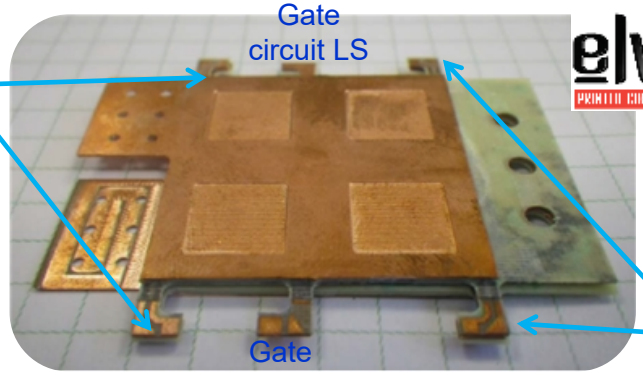
2. SiC Power Chip on Chip

SiC Prototype overview: experimental results





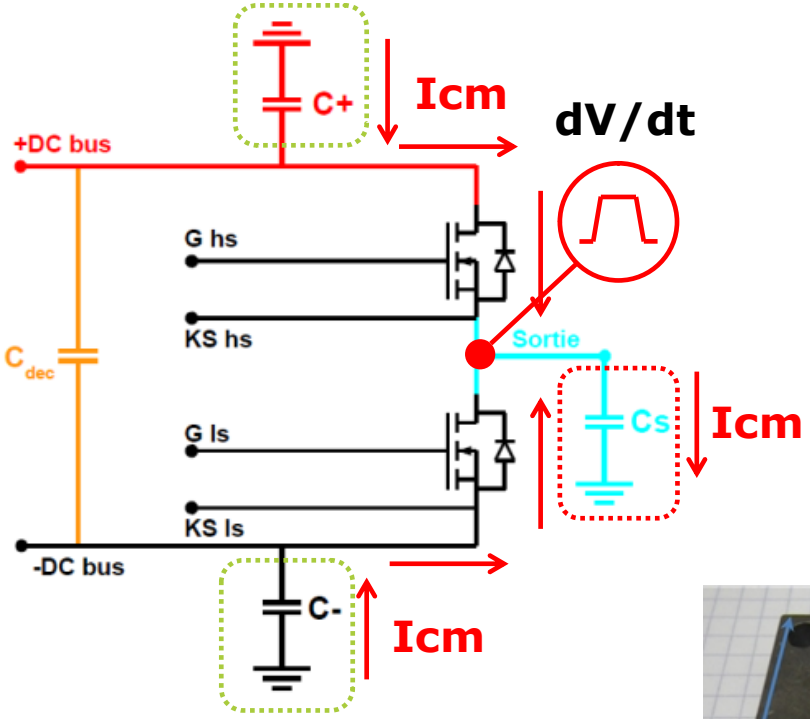




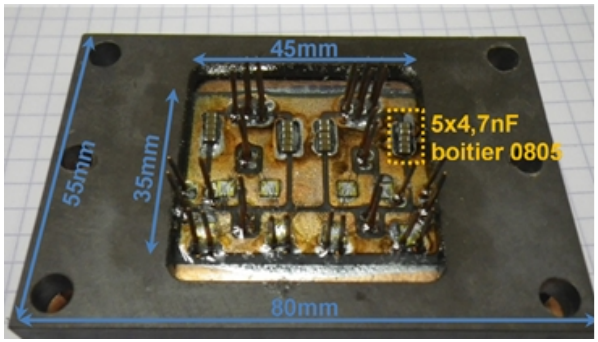
Clean output voltage, no oscillations

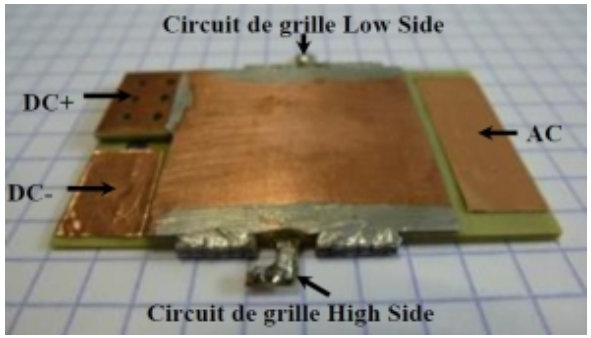
2. SiC Power Chip on Chip

EMC behavior: comparison with a custom 2D module



	2D Module	3D Module
dielectric material	AlN	SILPAD 1500ST
Relative permittivity (1MHz)	9	6,1
Width (mm)	1	0,203
C+ area (mm²)	400,5	900
C+ (pF)	31,9	239
C- area (mm²)	329	900
C- (pF)	26,2	239
Cs area (mm)	239,5	0
Cs (pF)	19,1	Very low

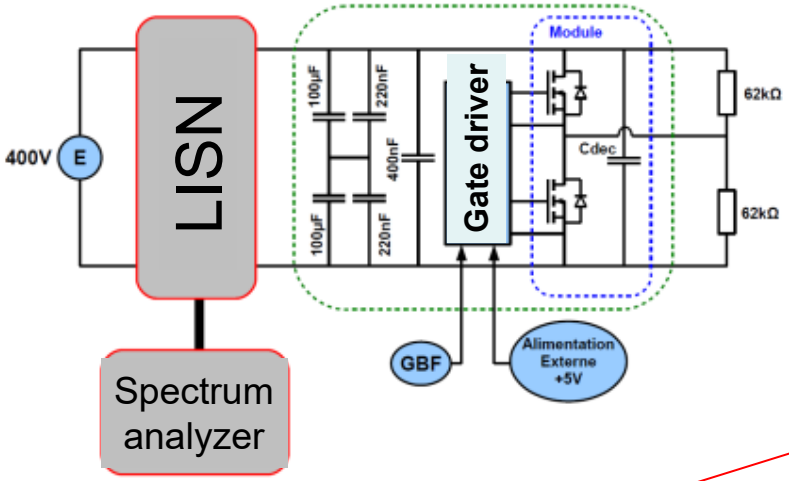




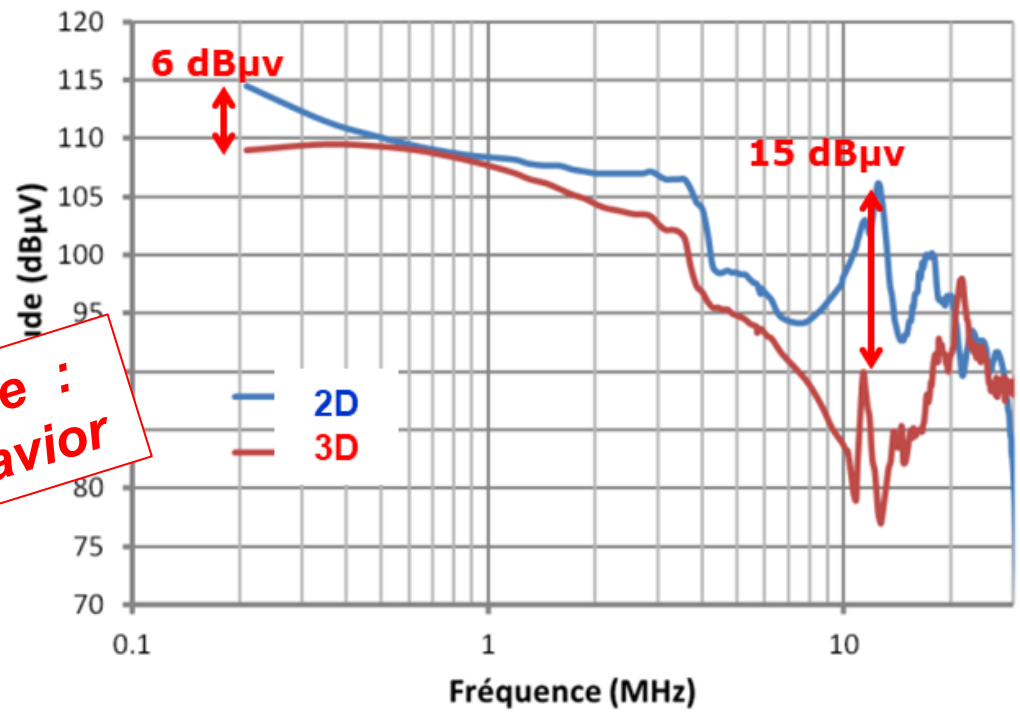
2. SiC Power Chip on Chip

EMC behavior: comparison with a custom 2D module

Interconnection board



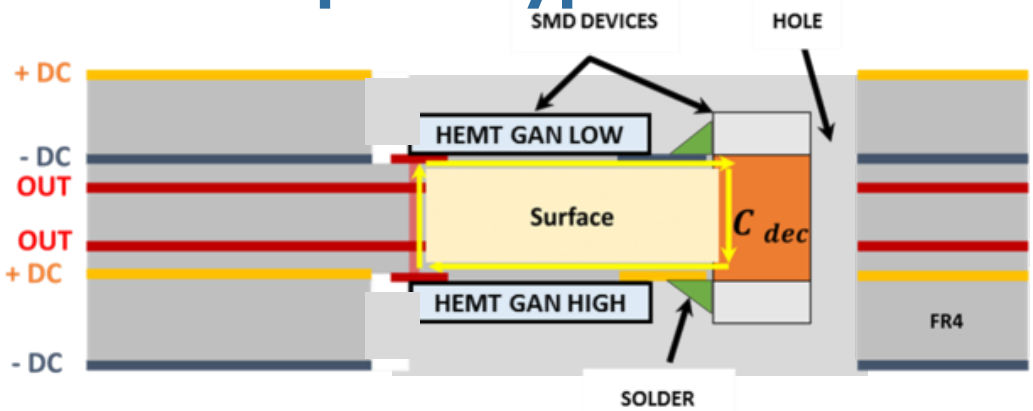
- Symmetrical load with 62kΩ resistor
  - Purpose, to characterize only the power module
- E=400V, switching frequency = 70kHz
- Identical gate driver
- Common mode voltage measurement (150kHz-30MHz)

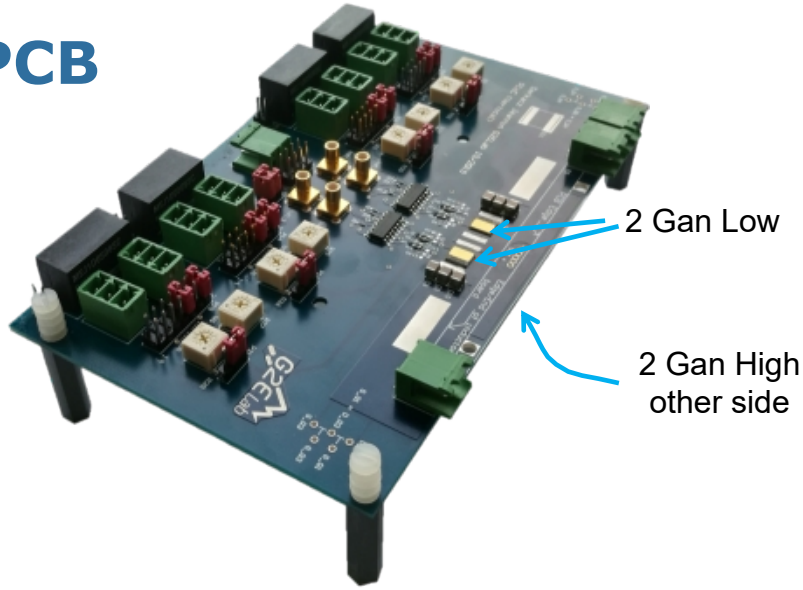


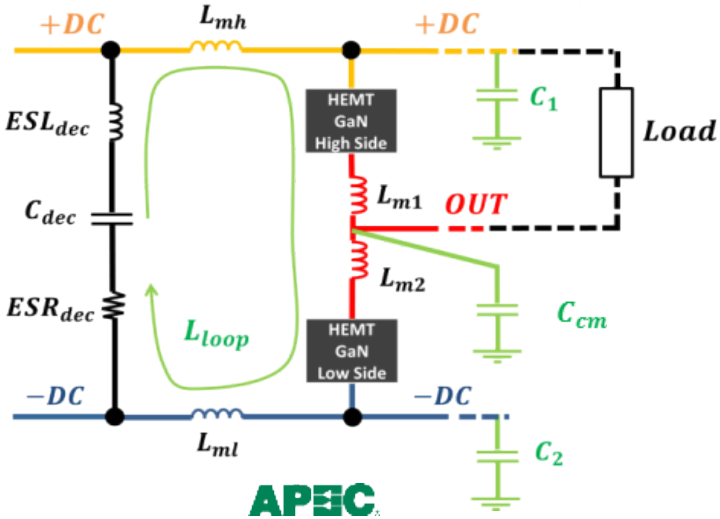
3D PCoC Module : better Emc behavior

2. GaN Power Chip on Chip

First prototype with multilayer PCB



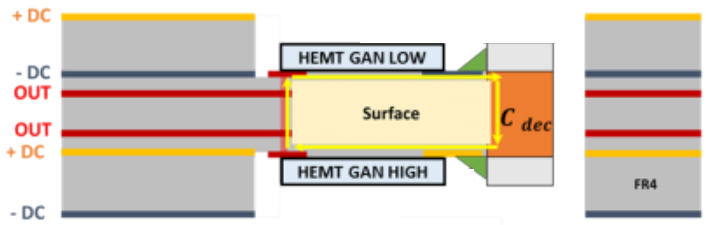




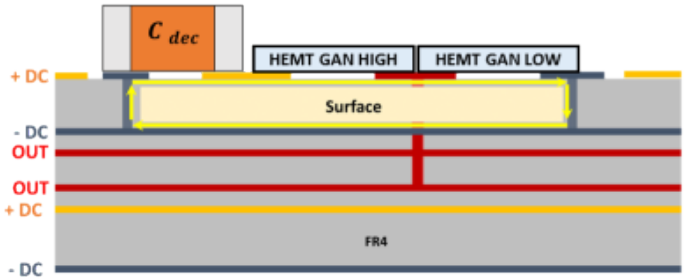
- GaN components are soldered on both sides of the PCB, on the inner layers
- Decoupling capacitances are placed vertically as close as possible of the GaN devices
- **Very low L_{loop} value**
- **Fully symmetrical layout (no CM/DM conversion)**

2. GaN Power Chip on Chip

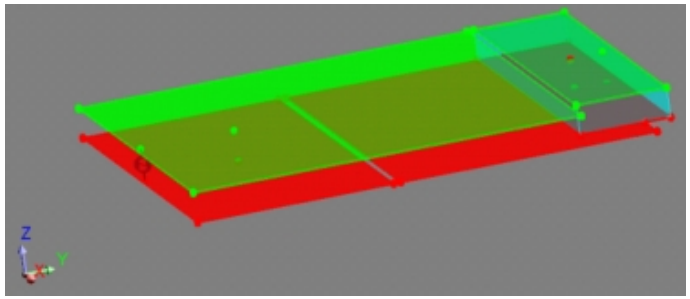
3D power loop design



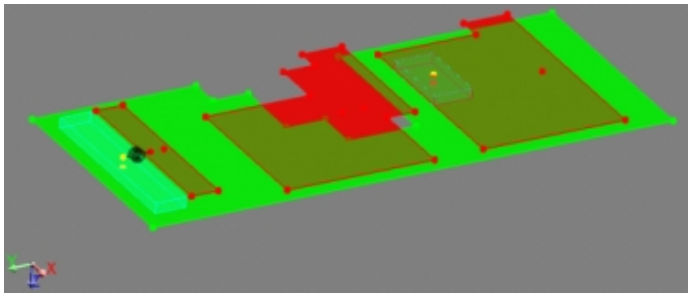
2D power loop design



PEEC modelling (FluxPEEC^{TM})



$L_{loop} \approx 1,46\ nH$



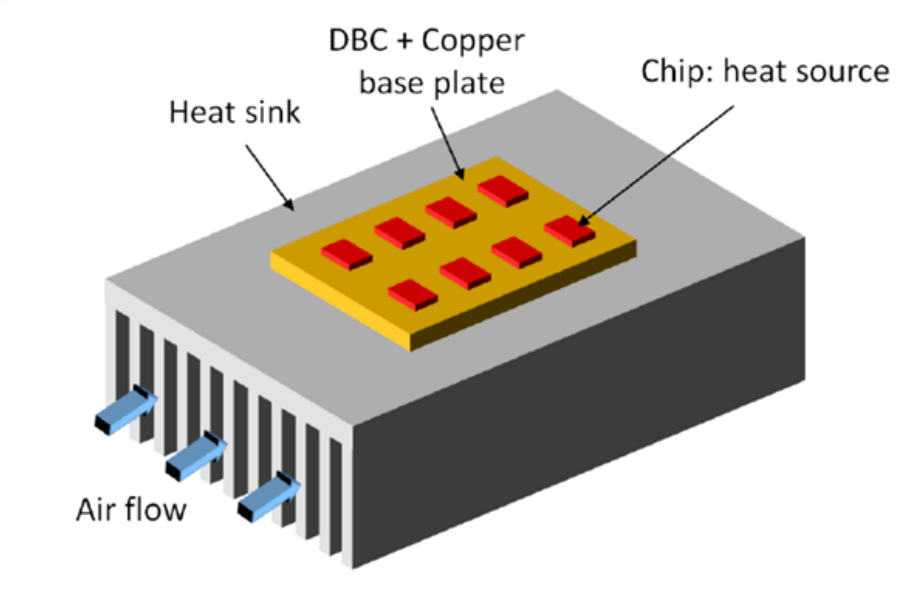
$L_{loop} \approx 5,82\ nH$

3. A new concept of integrated converter: TAPIR

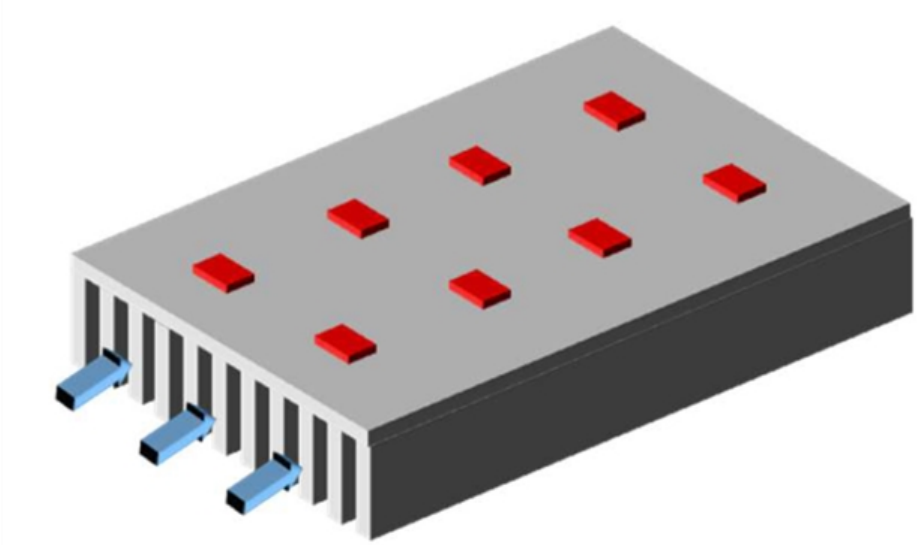
- **TAPIR - compacT and modulAr Power modules with IntegRated cooling**
  - Conventional Power Module:

  → bad use of Heasink

  (dies concentrated, thermal interfaces)

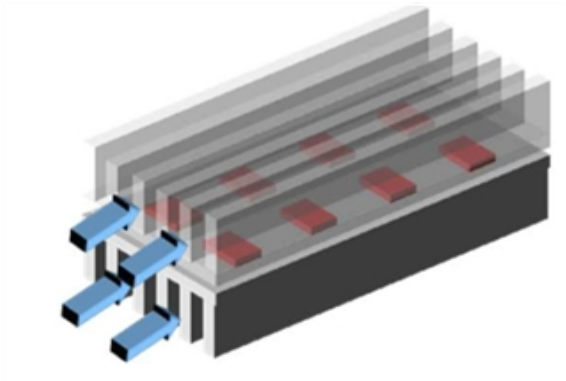


  - Equispaced dies directly on the heatsink: better use

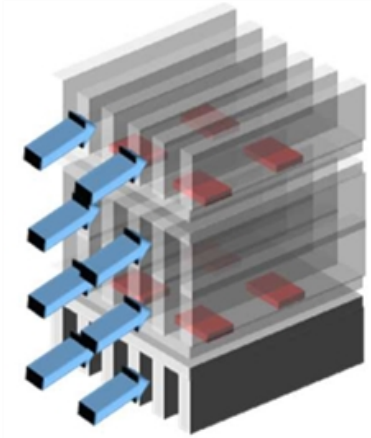


3. A new concept of integrated converter: TAPIR

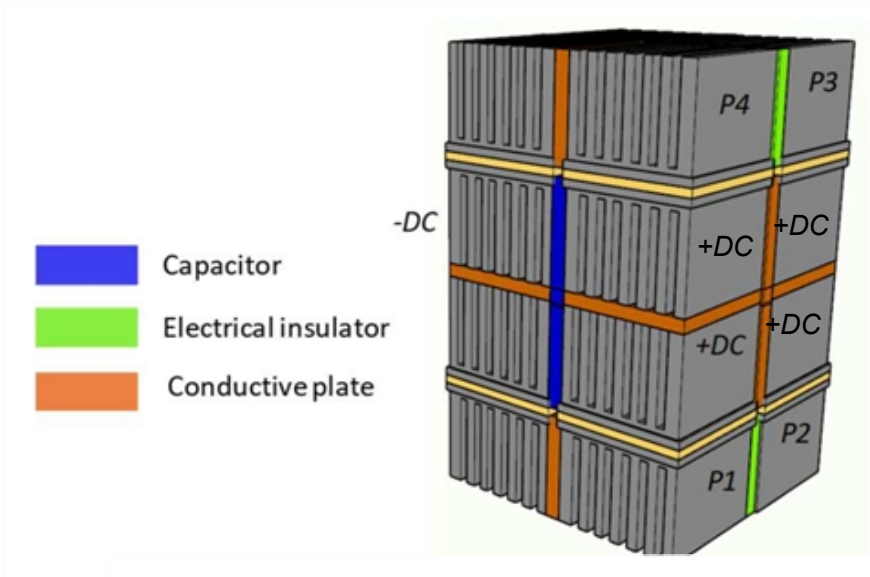
- Double side cooling



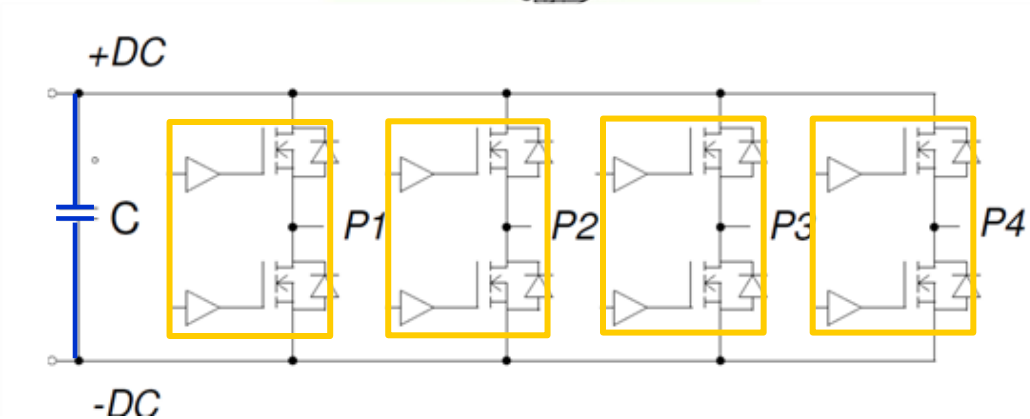
- Full 3D Integration: reduced pressure drop



- Converter realization: heatsink used as electrical connections

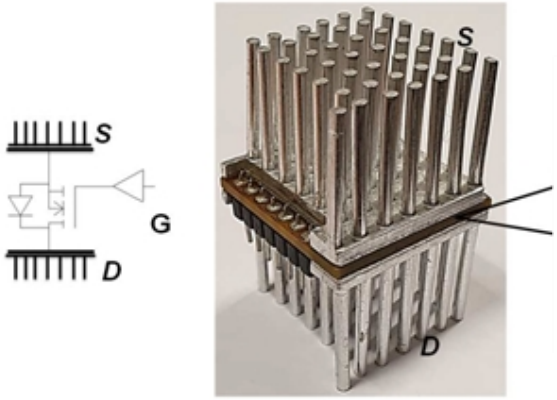


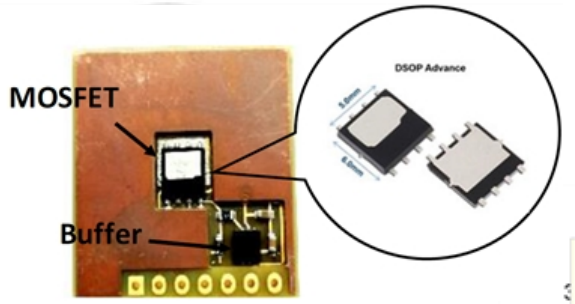
Dies and decoupling capacitor embedded inside an aluminum structure
→ aluminum use optimized
→ number of thermal interfaces reduced



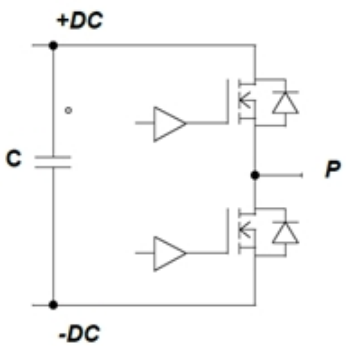
3. A new concept of integrated converter: TAPIR

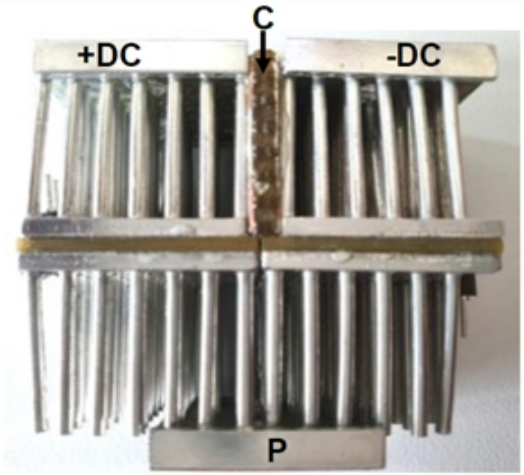
- Low voltage elementary module: first realization with packaged dies

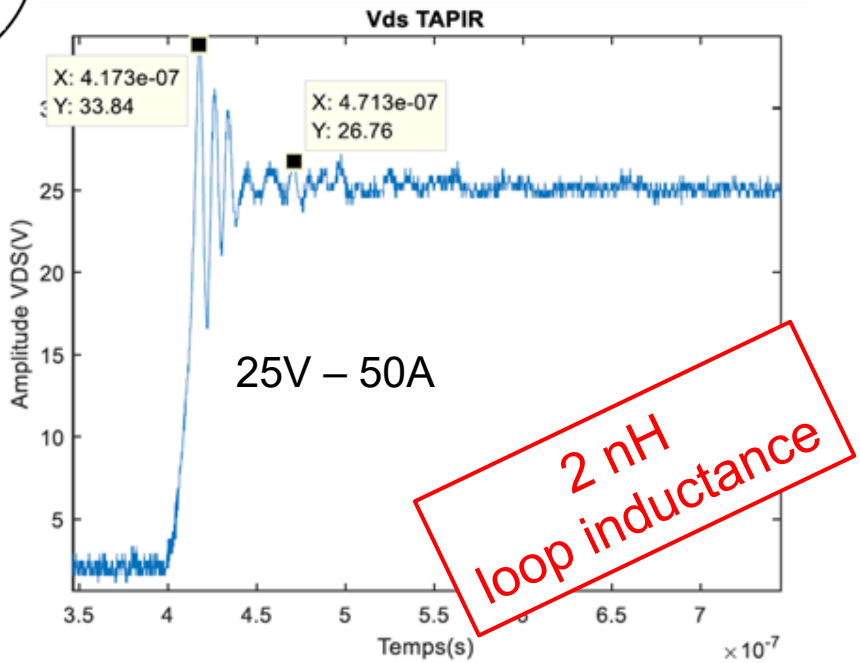




- TAPIR Switching Cell

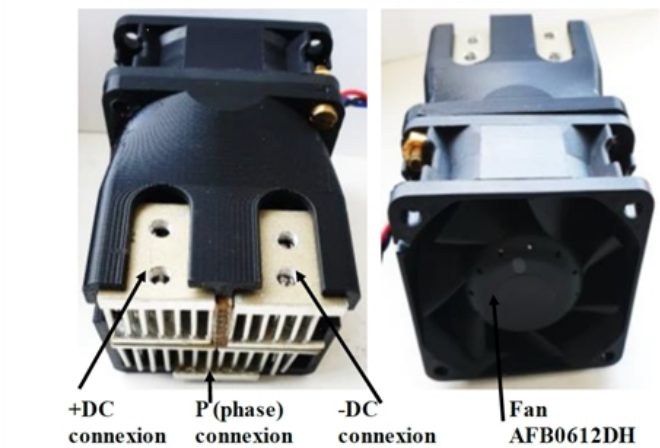




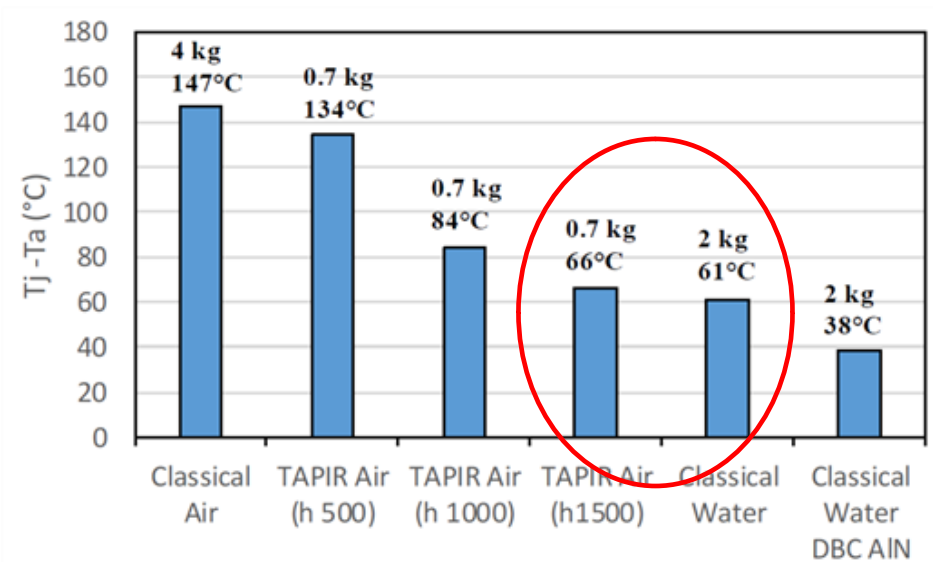


3. A new concept of integrated converter: TAPIR

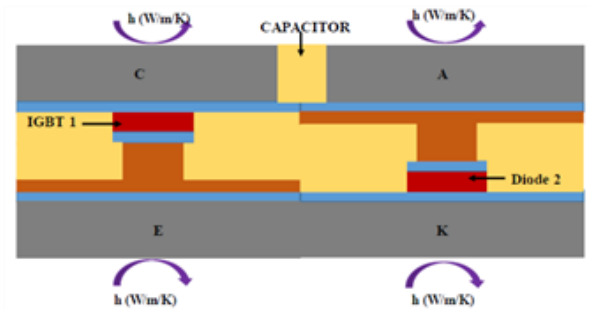
- Thermal Characterization



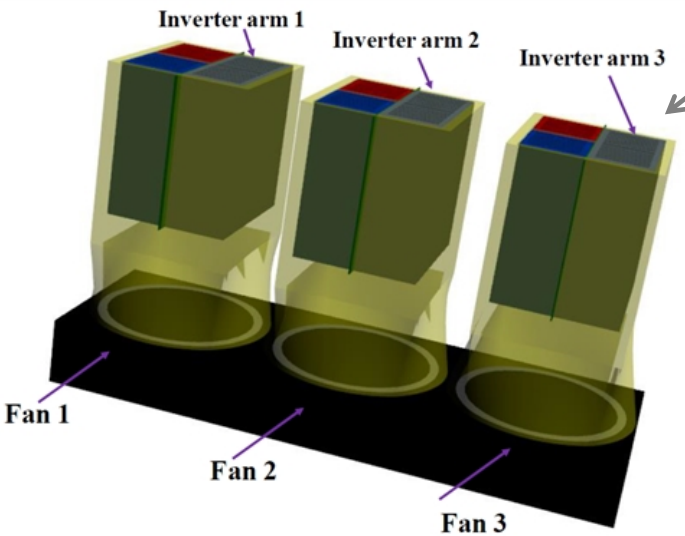
Rthj-a: 1,3 K/W
(1K/W with bare dies)



- Estimation of 3 phases inverter performances (simulation)



h fitted from measurement



Conclusion

- **Electromagnetic behavior of package limits switching performances**
- **3D integration shows outstanding EM performances → PCoC concept**
  - ***Sub nH, uncoupled power and gate circuits, low EMI***
  - Validated with SiC devices
  - Ongoing work on GaN, at converter level
- **New integration concept with high thermal performances: TAPIR**
  - 3D association of elementary cells via electro-thermal interfaces
  - Better use of cooling elements
  - High potentiality (CIPS 2020)