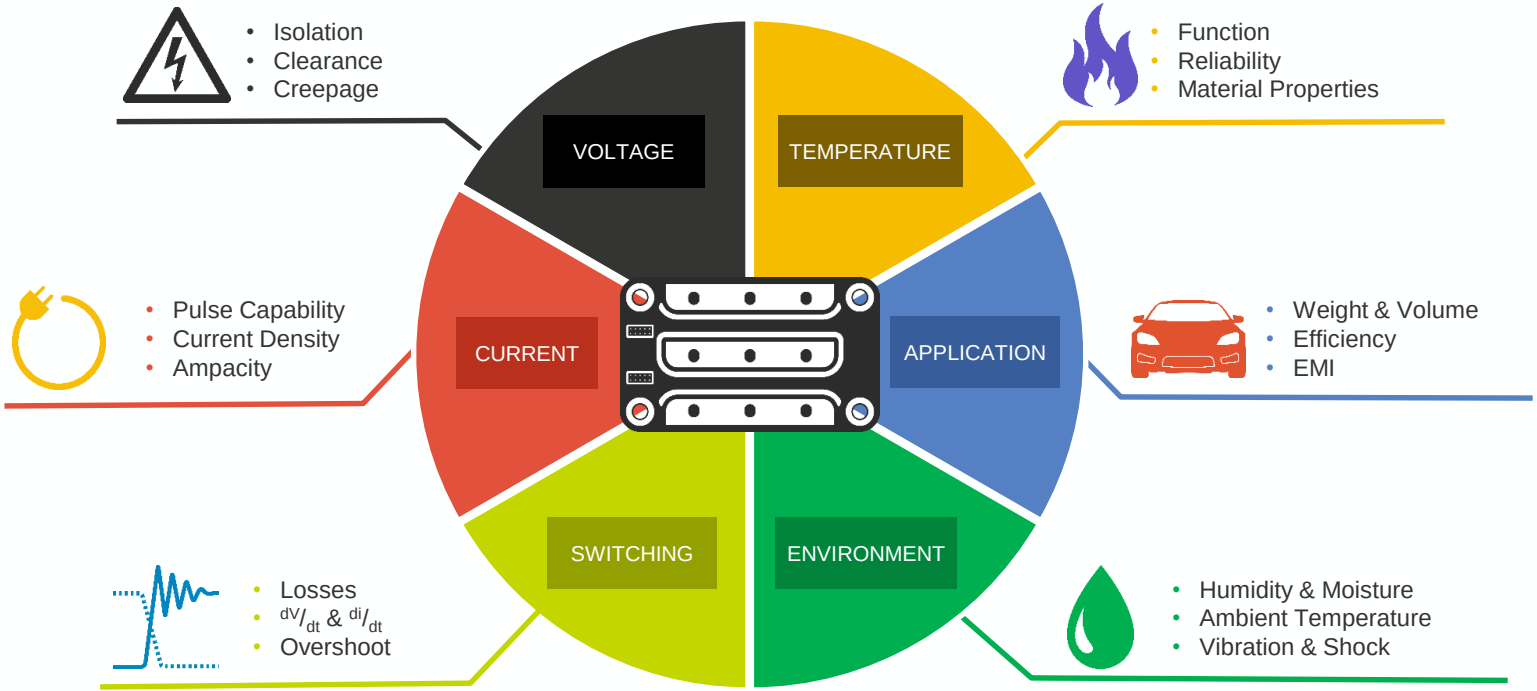
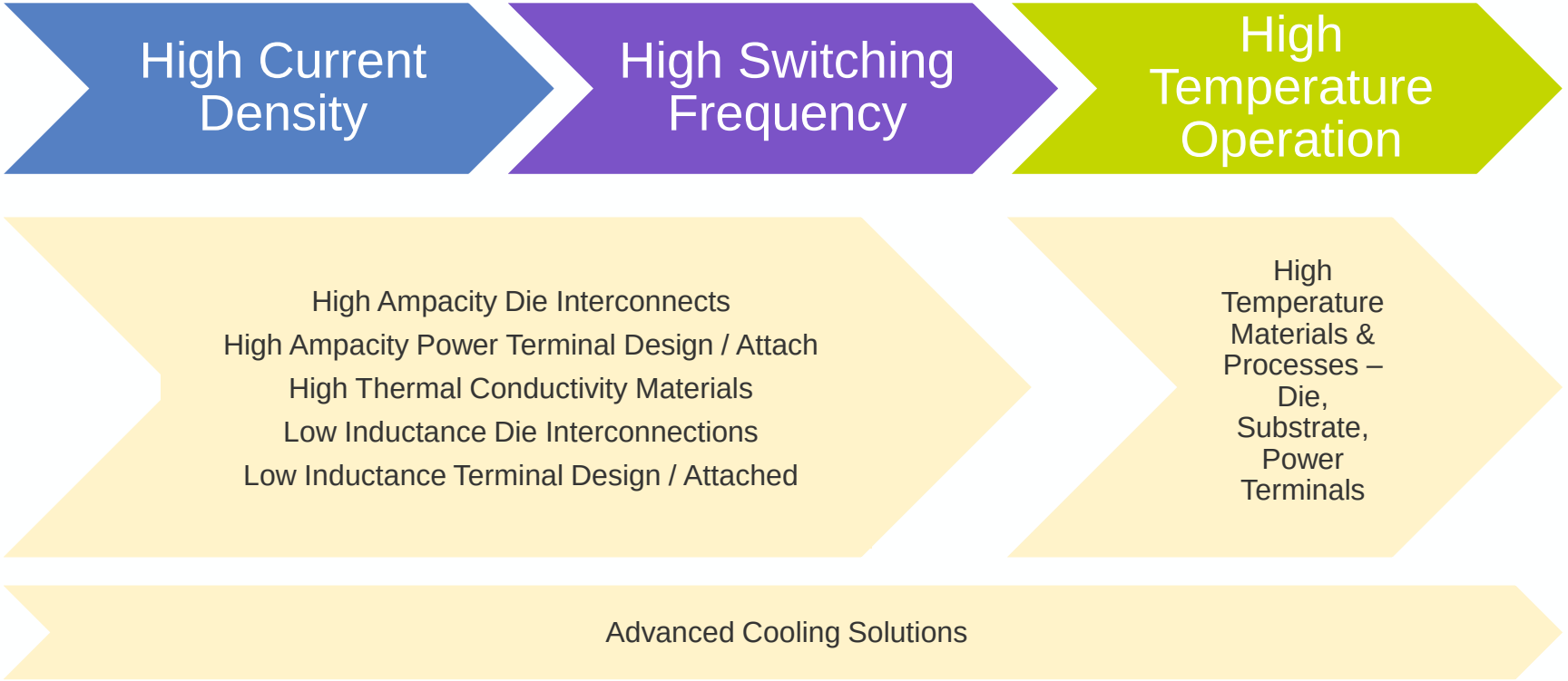
Reliability & System Level Design Considerations for SiC Power Modules

Ty McNutt, Ph.D.
April 24, 2019

Diverse Challenges



Wide Bandgap Package Challenges



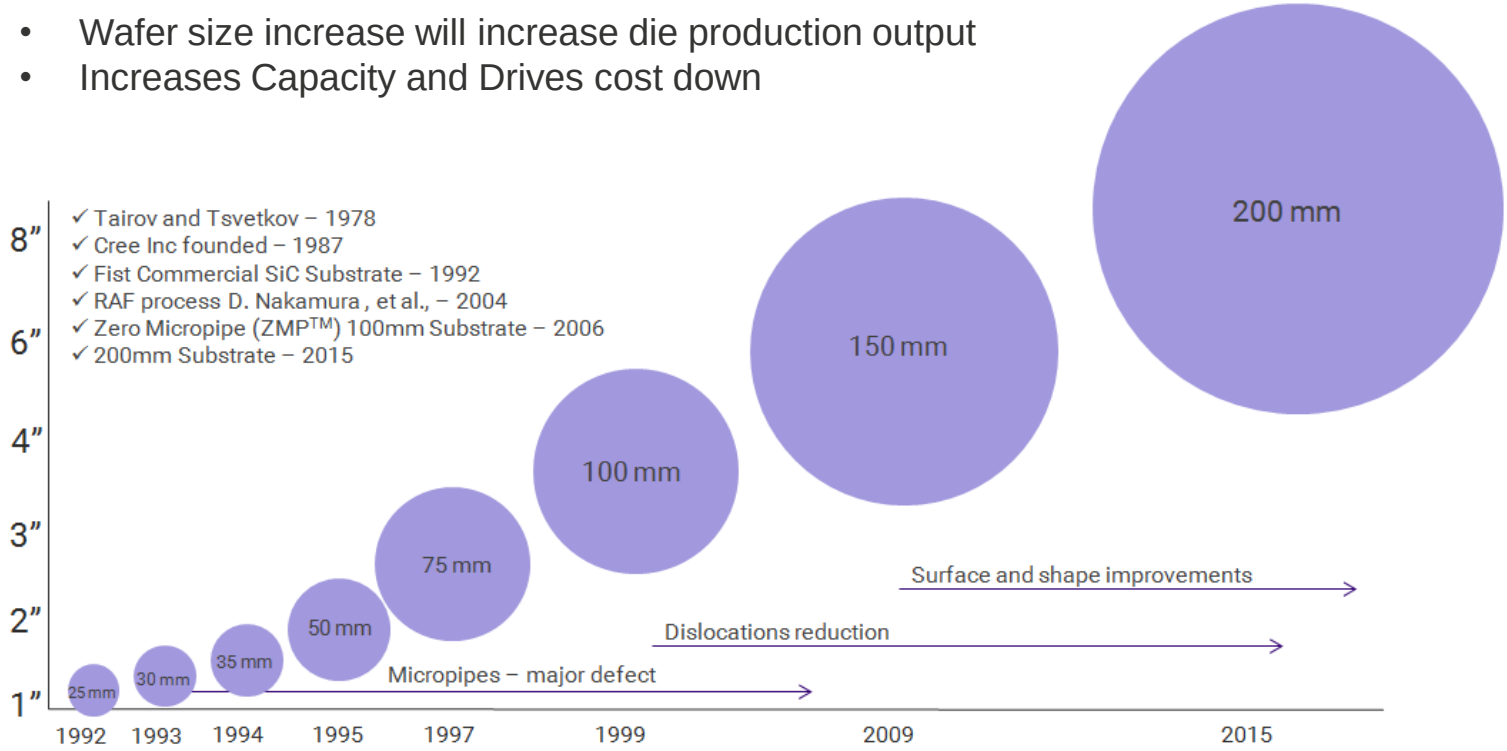
Outline

- Device Reliability
- Module Component Design & Testing
- System Level Considerations
- Extending to Medium Voltage
- Conclusion

Device Reliability

Wolfspeed – SiC Wafer Progression

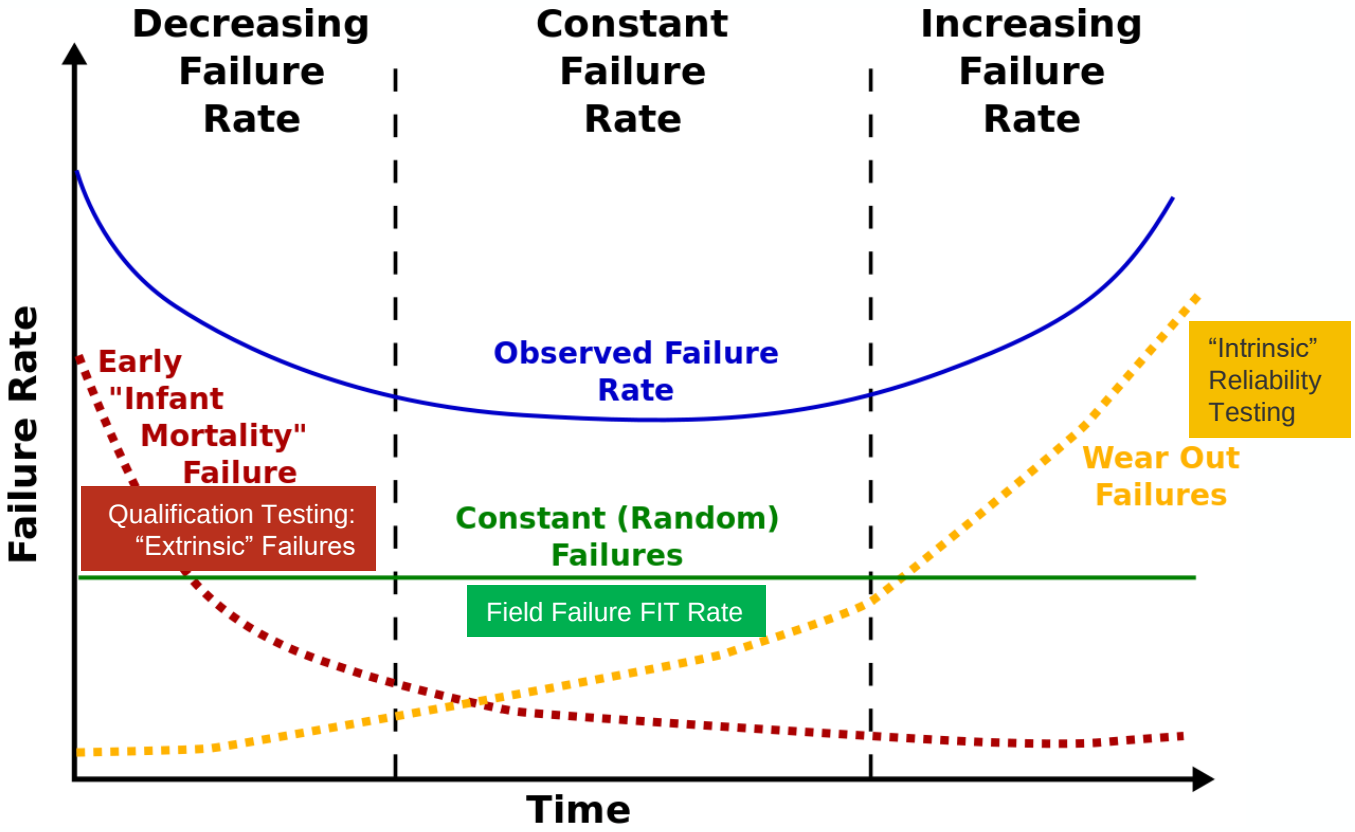
- Wafer size increase will increase die production output
- Increases Capacity and Drives cost down



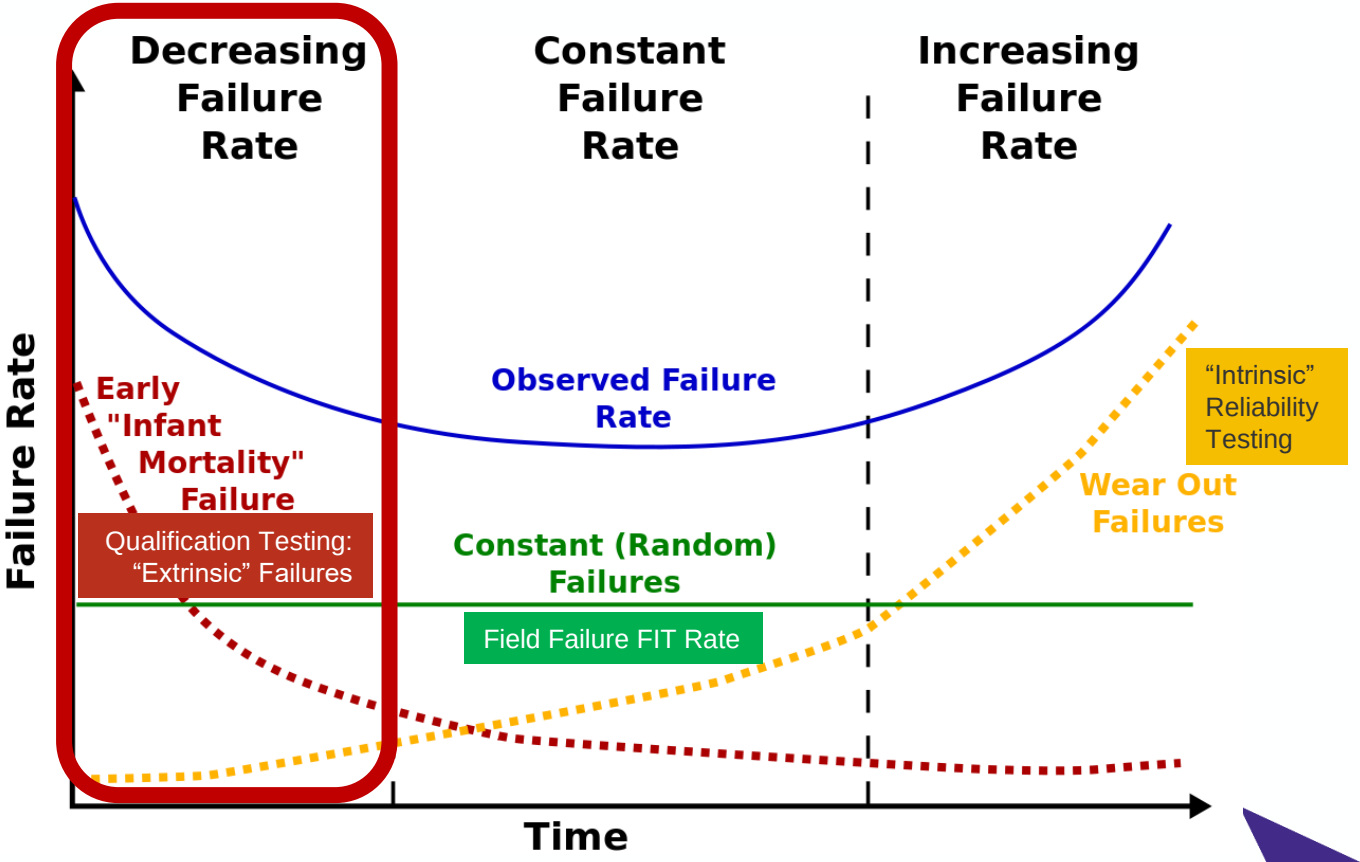
Reliability Testing

Testing Type	Purpose	Key Metric	Example
Qualification Testing	Designed to demonstrate a minimum outgoing quality and early life failure percentage	“Lot Tolerant Percent Defect” (LTPD)	3 lots * 77 samples per lot, with ZERO FAILURES, demonstrates LTPD < 1% with 90% statistical confidence
Reliability Testing	Designed to demonstrate the long-term wear-out lifetime that can be expected	Median Time To Failure (MTTF) or t1% (time to 1% failures)	TDDB testing to failure shows that C2M MOSFET MTTF is ~ 30 million hours

Reliability Overview – “Bathtub Curve”



Product Qualification

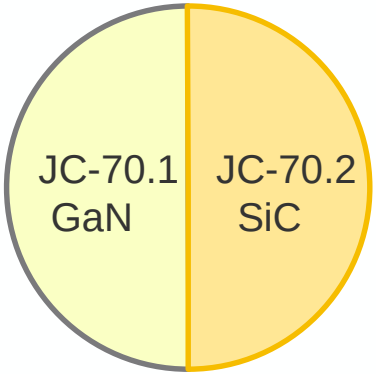


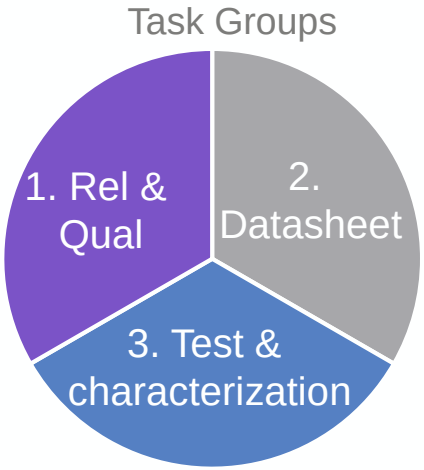
Industry consortia

Consortium	Abbreviation
Joint Electron Device Engineering Council	JEDEC
Automotive Electronics Council	AEC
International Electrotechnical Commission	IEC
Japan Electronics and Information Technology Association	JEITA

JEDEC

- JC-70 committee newly formed to create guidelines (JEPs) and standards (JESDs) for power conversion devices
- Each subcommittee has 3 task groups (TGs)
- TG702_1: SiC reliability and qualification
  - Kicked off activities at WIPDA 2017
  - Charter established, Teams formed to work on guidelines first, to be followed by standards
  - Currently > 50 members from >28 member companies + SMEs
  - Contact us if interested in participating!
- Task groups are open to paid member companies
  - Also welcome participation from subject matter experts from non-member entities, such as academia

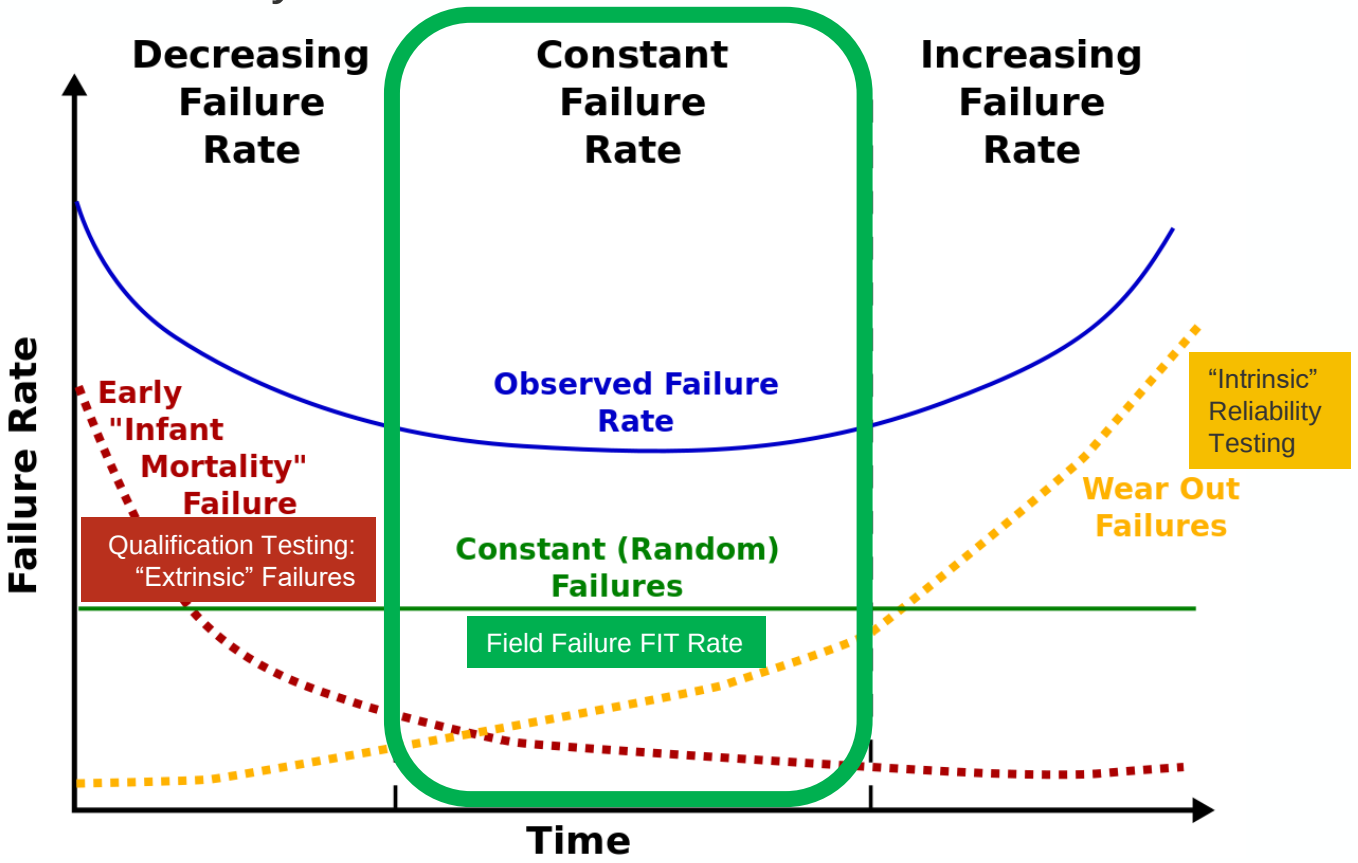




Typical Product Qualification

Stress	Abrv	Sample Size Per Lot	# of Lots	Reference (current revision)	Additional Requirements	Accept on # Failed
High Temperature Reverse Bias	HTRB	77	3	MIL-STD-750-1 M1038 Method A	1000 hours at Vmax and Tcmax	0
High Temperature Gate Bias	HTGB	77 each Vgs>0 and Vgs<0	3	JESD22 A-108	1000 hours at VGSmax and VGSmin and Tcmax	0
Temperature Cycling	TC	77	3	JESD22 A-104	1000 cycles Ta_max/Ta_min	0
Unbiased Highly Accelerated Stress Test	UHAST	77	3	JESD22 A-118	96 hours at 130 °C and 85% RH	0
High Humidity High Temp. Reverse Bias	H3TRB	77	3	JESD22 A-101	1000 hours at 85 °C, 85% RH with device reverse biased to 100 V	0
Intermittent Operational Life	IOL	77	3	MIL-STD-750 Method 1037	6000 cycles, 5 minutes on / 5 minutes off, devices powered to ensure DTJ ≥ 100 °C	0
Destructive Physical Analysis	DPA	2	3	AEC-Q101-004 Section 4	Random sample of parts that have successfully completed H3TRB and TC	0

Field Reliability

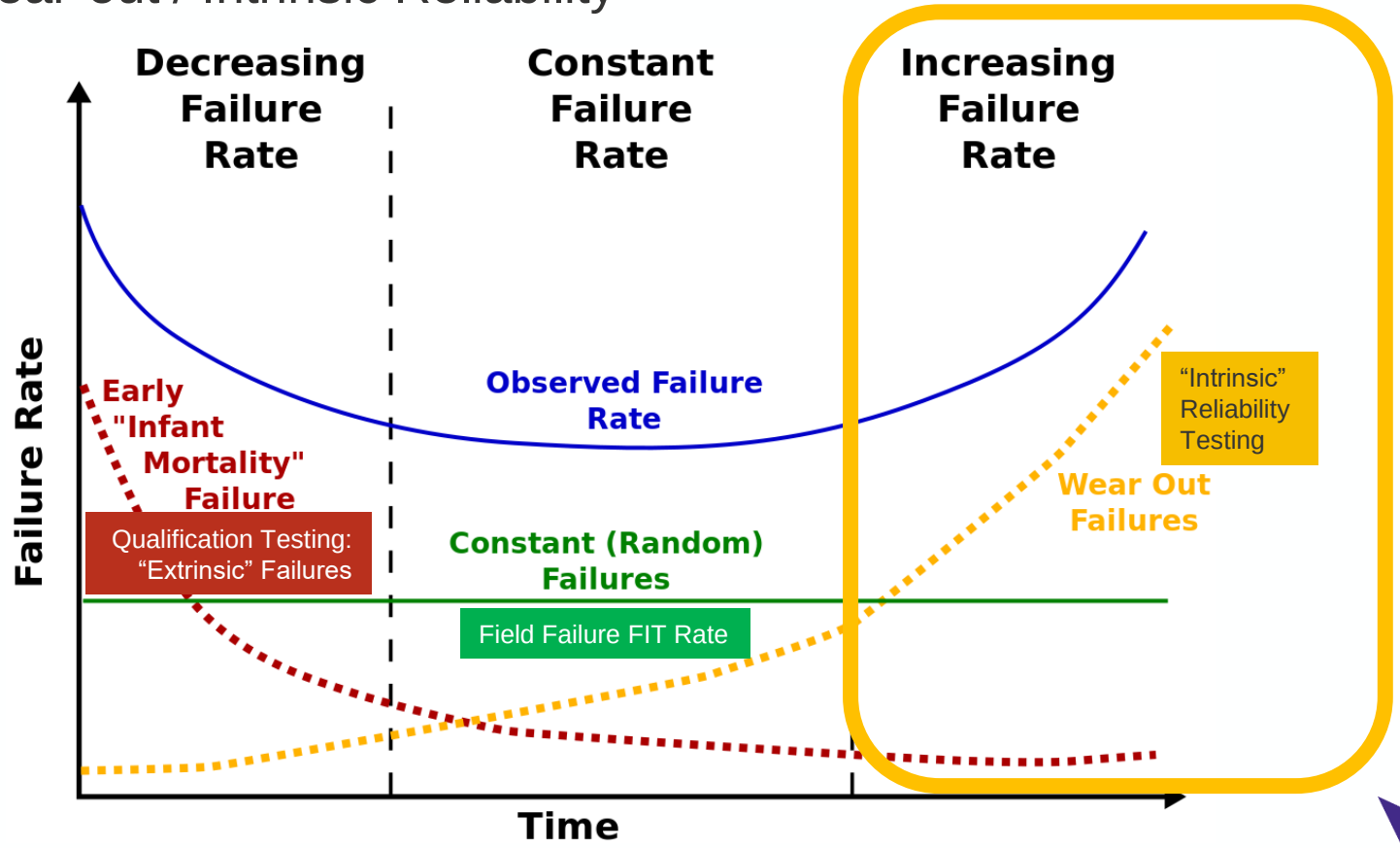


Wolfspeed Power Field Reliability

Technology	Fielded Device Hours (Billions)*	FIT Rate (valid field failures per billion device hours)**
CSDxxx060 Diode	1203	0.1
C2Dxxx120 Diode	511	0.6
C3Dxxx060 Diode	2919	0.06
C4Dxxx120 Diode	708	0.2
C2M MOSFET	63	3.7
C3M MOSFET	11	4.1

- *Calculated today's date minus confirmed ship date minus 90 days (allowing for time to put into service) * 12 hours per day
- **Calculated as: 2 times the number of valid field failures (excludes engineering evaluations, as-received visual defect escapes or issues, as-received test escapes, packaging and assembly quality issues) divided by fielded device hours; includes an additional factor for statistical confidence margin

Wear-out / Intrinsic Reliability

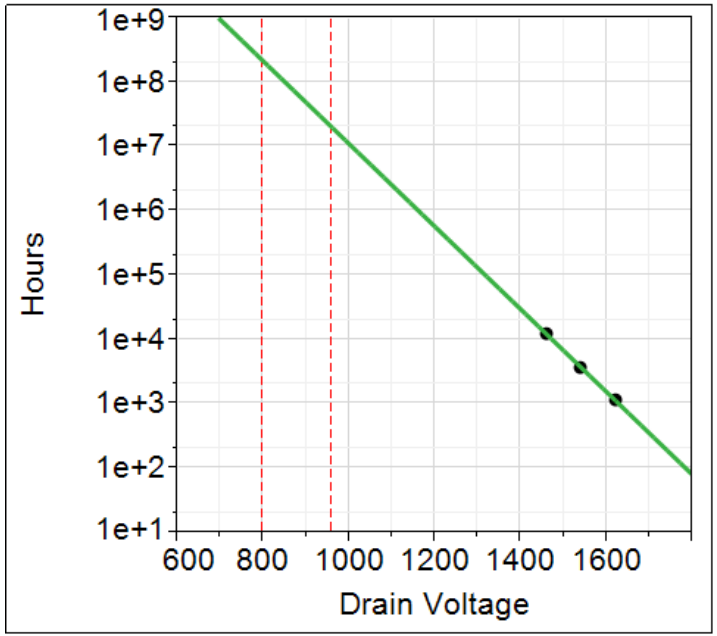


Potential Failure Mechanisms Summary

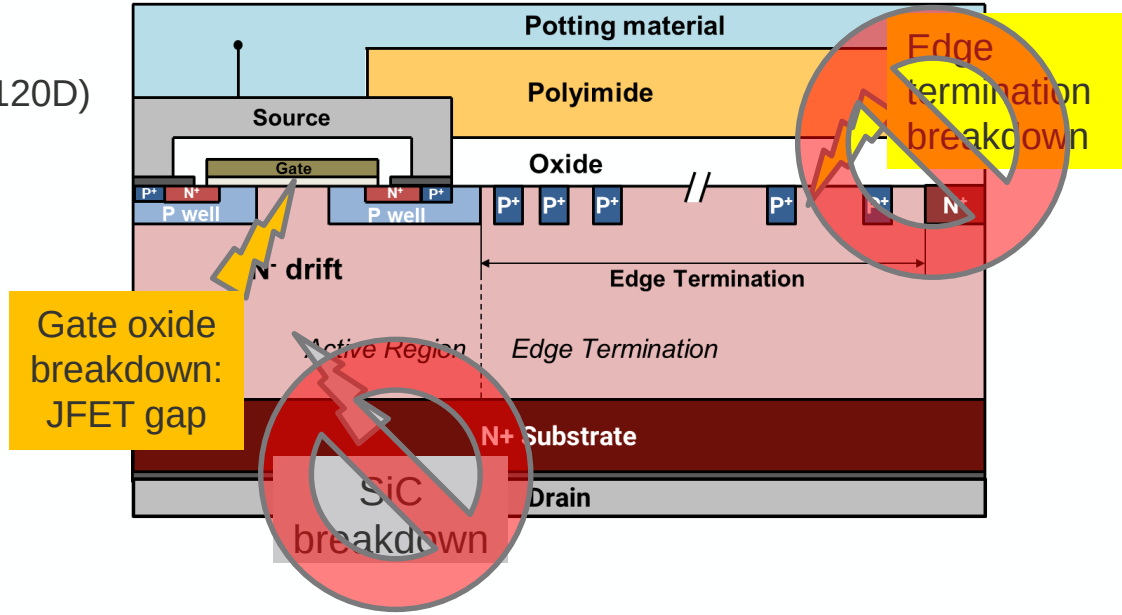
Requirement	Gate oxide breakdown	SiC breakdown	Termination breakdown	Threshold drift	Increased resistance / reduced current flow
High drain bias	HTRB, ALT-HTRB	HTRB, ALT-HTRB	HTRB, ALT-HTRB	HTRB, ALT-HTRB	
High altitude	n-irradiated HTRB	n-irradiated HTRB			
High humidity	THB		THB		THB
High gate bias	TDDB, HTGB			NBTI, PBTI	
3rd quadrant					Body diode HTOL

Accelerated life test high temperature reverse bias (ALT-HTRB)

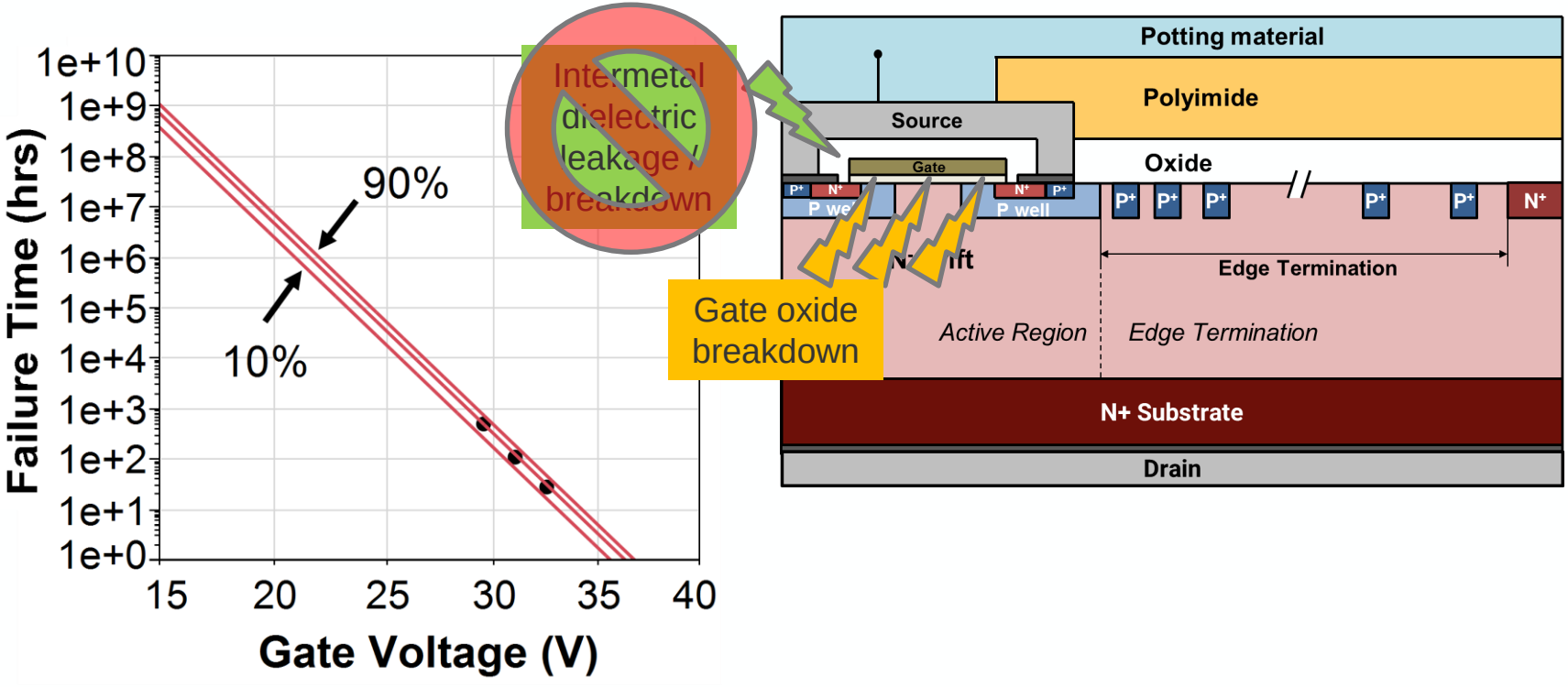
Full production 1200V, 80 mΩ MOSFETs in TO-247-3 packages (Wolfspeed C2M0080120D)



D. Gajewski et al., IIRW, 2016



Time-Dependent Dielectric Breakdown (TDDB)

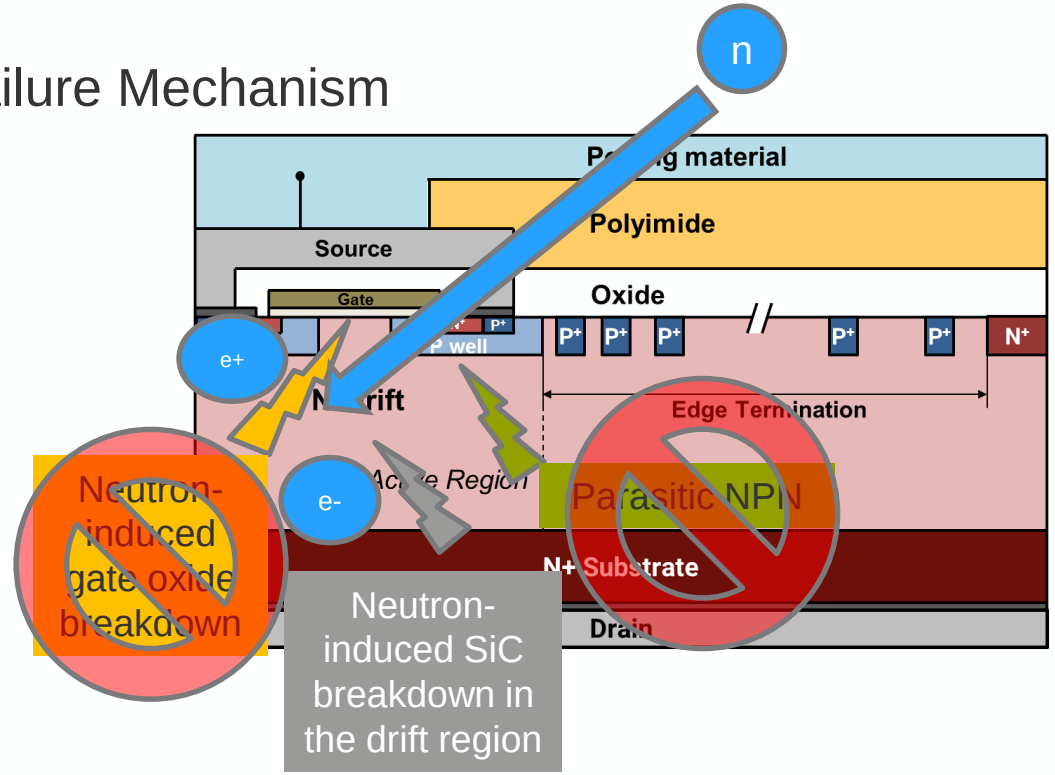


D. Lichtenwalner et al., ECSCRM 2018

Predicts >1E8 hours at 15V and 175C

Terrestrial Neutrons Failure Mechanism

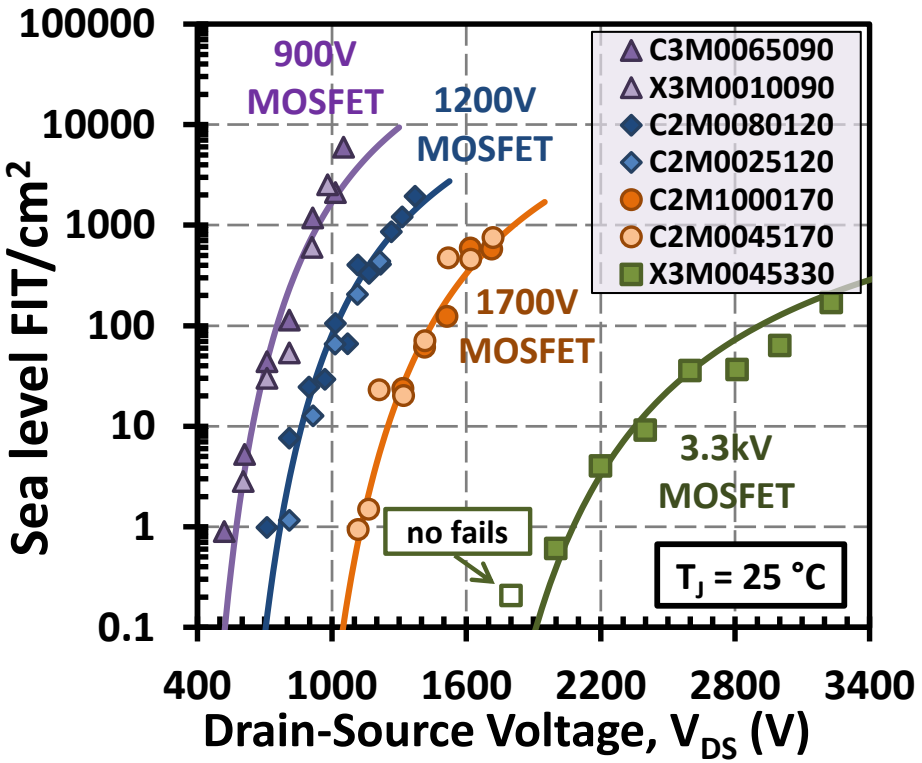
- Only drift-related breakdown is observed
- No gate oxide breakdown
- No parasitic NPN turn-on



Terrestrial Neutrons

- Wolfspeed SiC MOSFET FIT rates: scaling by active area
- Failure rate increases proportionally with device area
- Failure rate decreases as voltage rating increases
- FIT/cm^2 vs V_{DS} for Wolfspeed MOSFETs

  900V 65 mohm
  900V 10 mohm
  1200V 80 mohm
  1200V 25 mohm
  1700V 1000 mohm
  1700V 45 mohm
  3.3kV 45 mohm

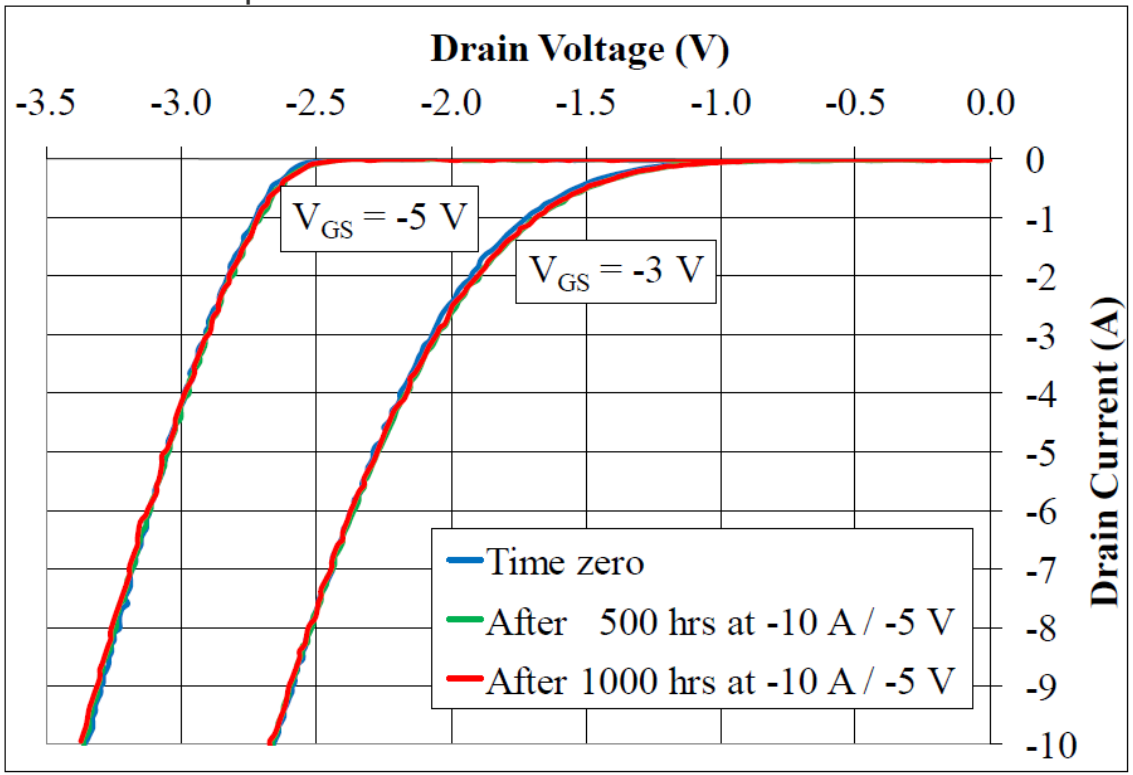


D. Lichtenwalner et al., IRPS 2018

Body Diode

- HTOL stress in 3rd quadrant mode
- Body diode and MOSFET VF values measured pre/post stress – negligible parametric drift

Wolfspeed Gen2 1200V 80 mOhm MOSFET



D. Gajewski et al., ICSCRM 2013 / Mat. Sci. Forum v.778-780

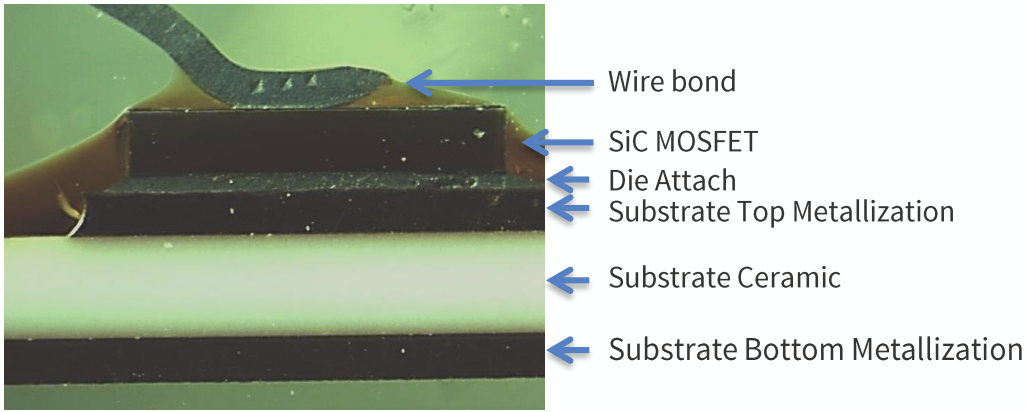
THB

- THB is a standard qualification test in all industry standard guidelines, but AEC-Q101 calls out THB stressing only up to 100 V
- In response to showing reliable performance under humid conditions, Wolfspeed has developed the “THB-80” test:
  - 85 °C and 85% RH at 80% of rated blocking voltage
- Recently released Wolfspeed E-Series :
  - Gen3 900 V MOSFETs
  - Gen4 1200 V Schottky diodes
  - Both have passed THB-80 qualification testing for 1000 hours with no visible evidence of corrosion

Module Component Selection & Design

Typical Power Module Stackup

- Start testing at subcomponent level, building up to the module level
- Thermal stress is used to evaluate the mechanical reliability of a module under various environmental conditions
  - Can be generated by ambient conditions (TS, TC, LTS, HTS) or by device heating (PC, IOL)
- Common failure points are located at interconnect points: substrate attach, substrate interfaces, wire bonds, dielectric materials



Typical power module stack-up

Ceramics in Packaging

- Aluminum oxide (Al_2O_3)
- Aluminum nitride (AlN)
- Beryllium oxide (BeO)
- Silicon Nitride (Si_3N_4)

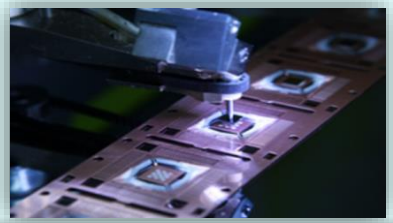
Material	Dielectric Constant	Dissipation Factor, tan δ	Electrical Resistivity, Ω-cm	CTE (ppm / °C)	TC (W / m-K)	Flex Strain (MPa)	Density (kg/cm³)
Al_2O_3	4.5 - 10	0.0004 – 0.001	> 10^{14}	6.5 – 7.2	22 - 40	300 - 385	3.75 – 4.0
AlN	8.5 - 10	0.001	> 10^{14}	2.7 – 4.6	100 - 260	280 – 320	3.2
BeO	6.5 – 8.9	< 0.001	> 10^{15}	6.3 – 9.0	260 - 300	170 - 240	2.95
Si_3N_4	5 - 10	-	> 10^{14}	2.3 – 3.2	25 - 35	255 - 690	2.4 – 3.4

- **Characteristics**
- Typically hard and brittle with low toughness and ductility
- Generally they are electrically and thermally insulating
- Ceramic materials normally have high melting temp
- High chemical stability
- May be amorphous, polycrystalline, or crystalline

Metal	Conductivity (nΩ-m)	CTE (ppm /°C)
Al	28.2 at 20°C	21 – 24
Cu	16.8 at 20°C	16 – 16.7

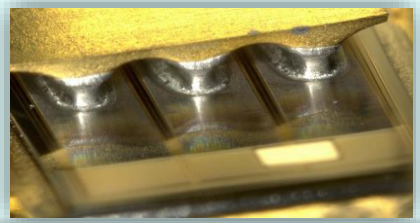
Advanced processes, materials, and design concepts enabling high performance SiC power packaging

Attaches



- Silver sintering paste
- Silver sintering film
- Diffusion soldering
- Ultrasonic welding
- Copper paste
- Diffusion bonding
- TLP soldering
- Exotic solder alloys
- High thermal conductivity epoxies

Interconnections

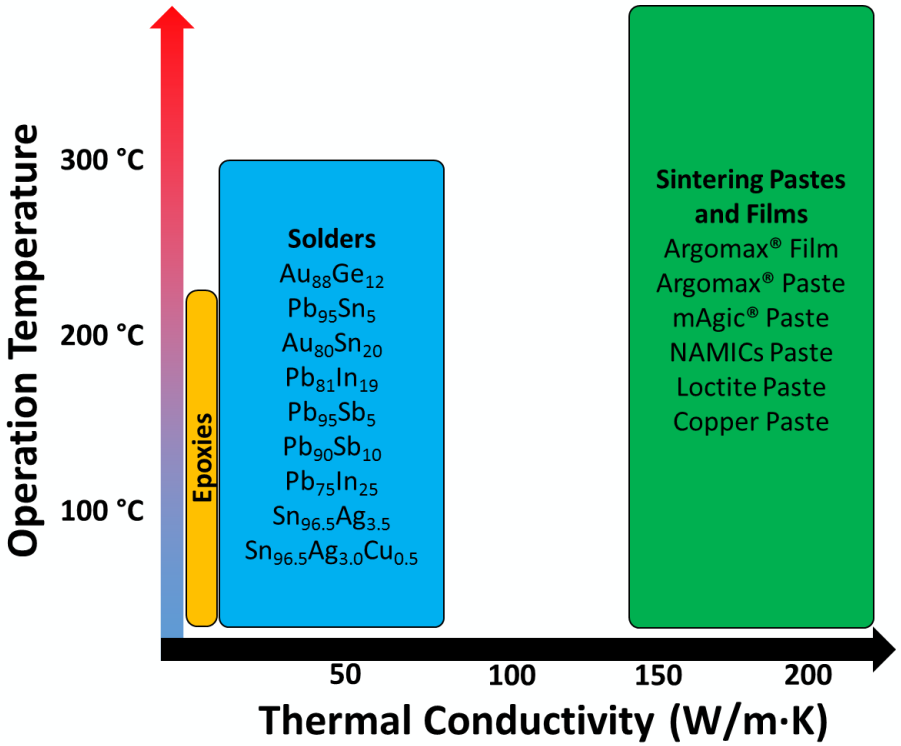


- Copper ribbon and large diameter wire bonding
- Double-sided power substrate attach
- Patterned dielectrics and metal deposition
- Patterned metal
- Flexible PCB
- Pressure-based interconnections

Advanced Cooling

- Direct-cooling
- Double-sided cooling
- Jet impingement
- Two-phase cooling
- Baseplate embedded heat spreader
- Baseplate or substrate embedded micro-fluidic channels
- Liquid immersion

Die and Substrate Attach materials

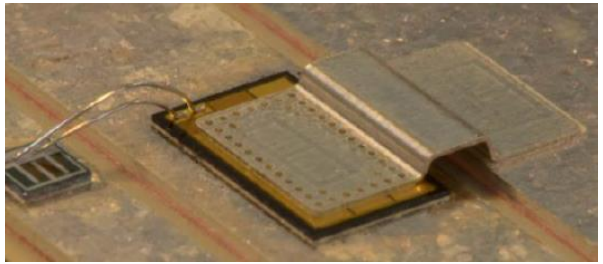


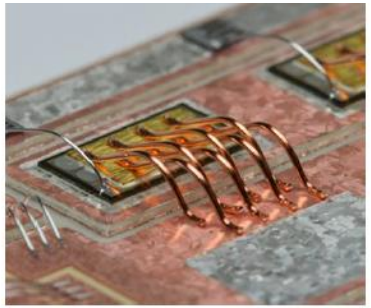
- Sintering paste materials exhibit high thermal conductivities (4× good solders) and high operation temperatures (~ 2×)
- Before a sintering material is selected, extensive thermal, electrical, and mechanical testing must be carried out before down-selecting to a single material.
- All sintering materials are not made equal.

[1], [2], [3], [4], [5]

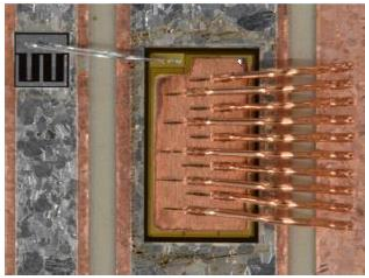
Wolfspeed 1200V, 13mOhm SiC MOSFET die in custom power module

- Cu plate sintered to top of die using Ag sintering at 250C, with pressure
- Wirebonds connect Cu plate (far right top and bottom) using so-called bond buffer technology
- Sintered Ag clip connection to source (left)
- 1000 cycle thermal shock passed successfully (-40 to +150°C)
- More results in manuscript





Wolfspeed MOSFET with sintered top plate



pcim EUROPE

Nuremberg, 16 – 18 May 2017

Reliable interconnection technologies for high-temperature operation of SiC MOSFETs

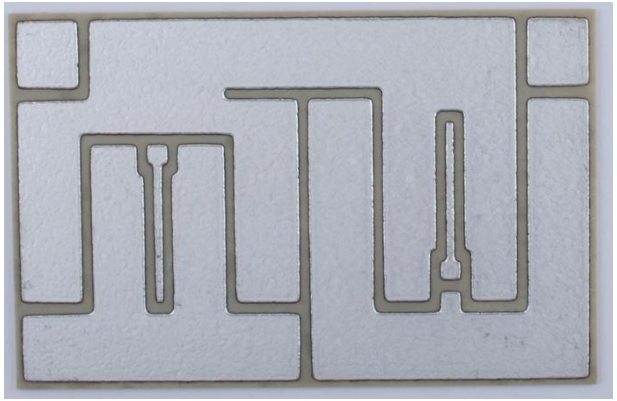
Fabian Mohn, ABB Switzerland Ltd., Corporate Research, Switzerland, fabian.mohn@ch.abb.com
Chunlei Liu, ABB Switzerland Ltd., Corporate Research, Switzerland, chunlei.liu@ch.abb.com
Jürgen Schuderer, ABB Switzerland Ltd., Corporate Research, Switzerland, juergen.schuderer@ch.abb.com

ABB

Subcomponent Testing

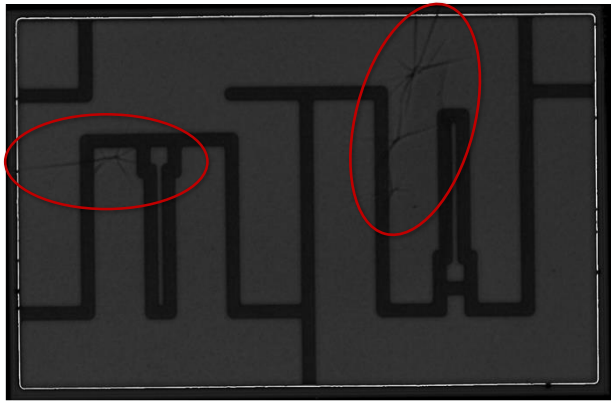
Thermal Cycling

- Two different failure mechanisms were screened for during thermal cycling:
  1. Delamination of the metal traces from the ceramic
     - Screened by visual inspection and scanning acoustic microscopy (SAM) analysis
  2. Cracking of the ceramic layer underneath the metal traces
     - Screened by SAM analysis



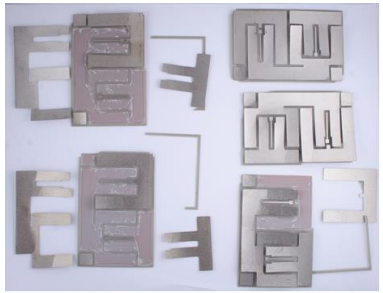
Photograph of substrate with induced failure.

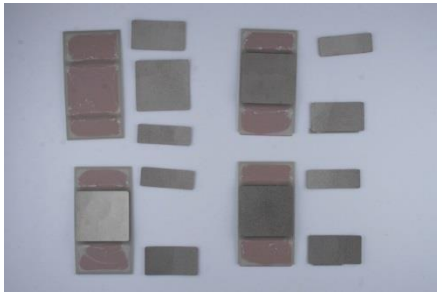
SAM image of substrate with induced failure.

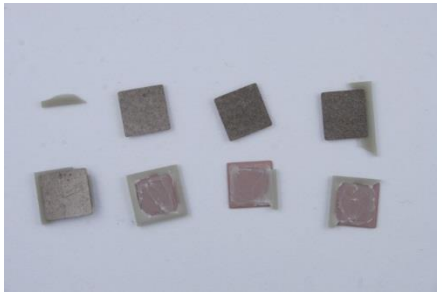


Thermal Cycling

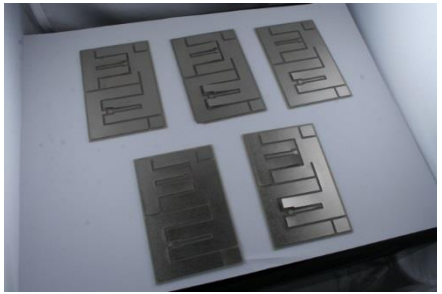
After 100 cycles every DBC substrate suffered delamination of the metal from the ceramic layer, regardless of layout or thickness (28 in total).

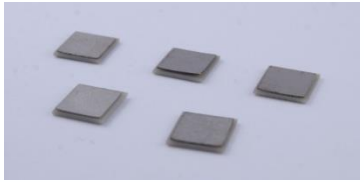


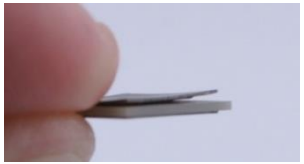




0.3/0.635/0.3 mm AlN DBC



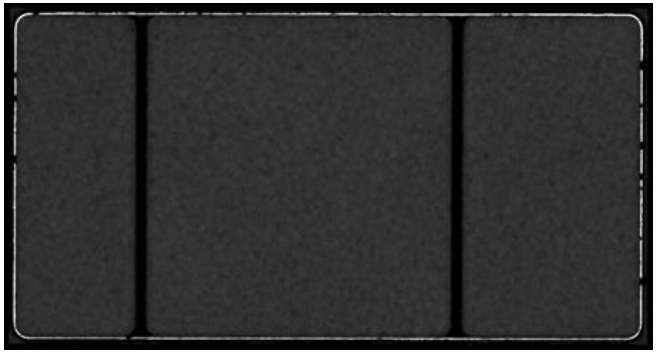




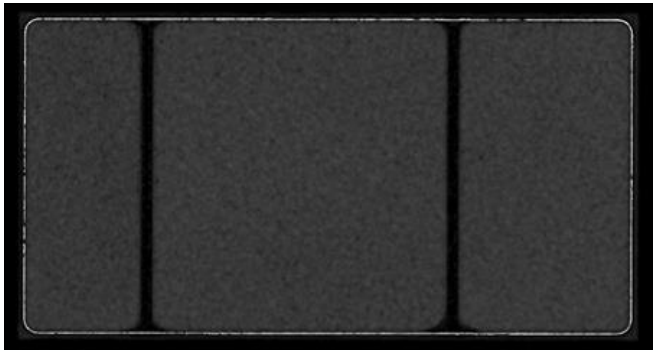
0.2/0.635/0.2 mm AlN DBC

Thermal Cycling

After 1000 cycles, no AMB or DBA substrates suffered any catastrophic failures.



0.2/0.32/0.2 mm Si_3N_4 AMB
0 cycle SAM image

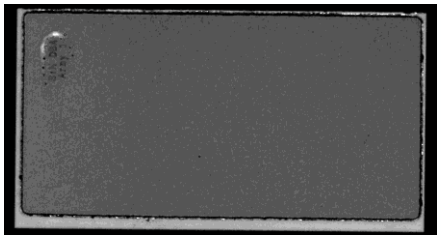


0.2/0.32/0.2 mm Si_3N_4 AMB
1000 cycle SAM image

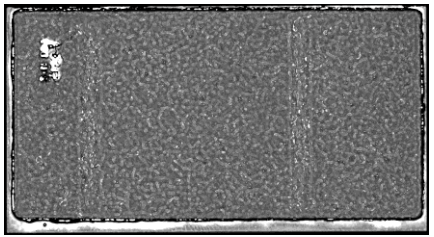
Thermal Cycling

Thermal cycling induces restructuring and reorientation of grain boundary, resulting in a change in surface roughness

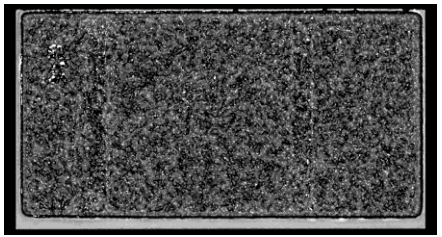
- This occurred in both AlN and Si_3N_4 samples and for all layout geometries



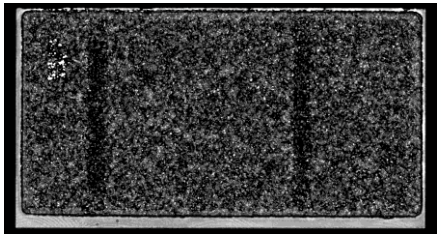
0 cycles



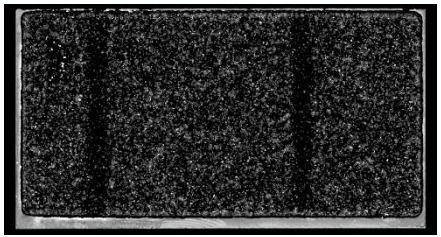
100 cycles



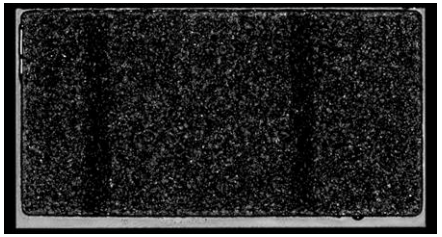
300 cycles



500 cycles



700 cycles

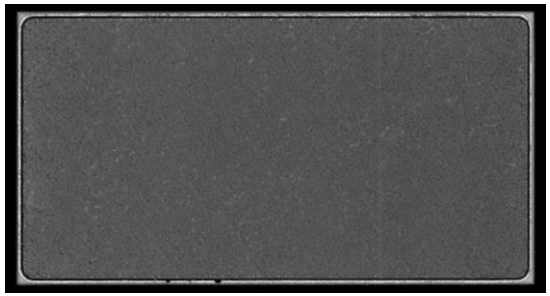


1000 cycles

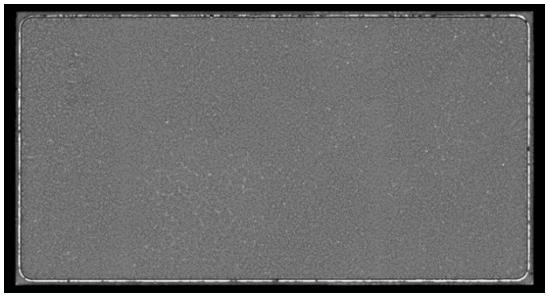
0.4/0.635/0.4 mm Si_3N_4 DBA

Thermal Cycling

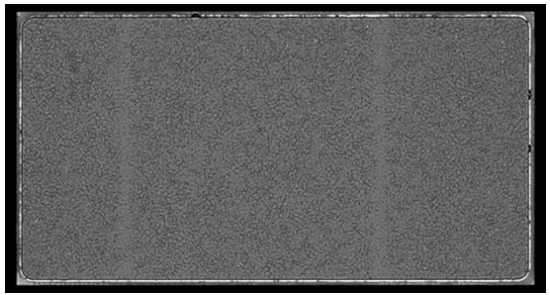
The AMB samples have similar grain boundary shifting, but not to the extent of the DBA samples.



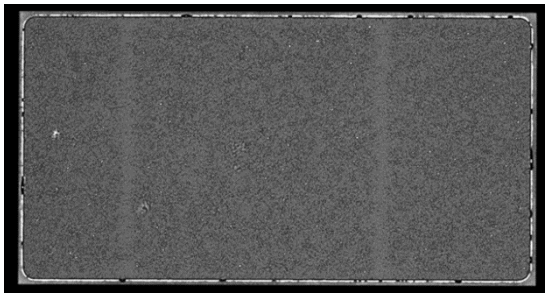
0 cycles



500 cycles



800 cycles



1000 cycles

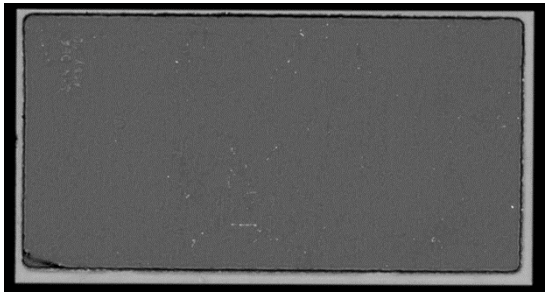
0.2/0.32/0.2 mm Si_3N_4 AMB

Thermal Dwell

Voiding was noticed at 0 hours; however, after 3000 hours of thermal dwell, no change in the voids was observed (both AlN and Si_3N_4).

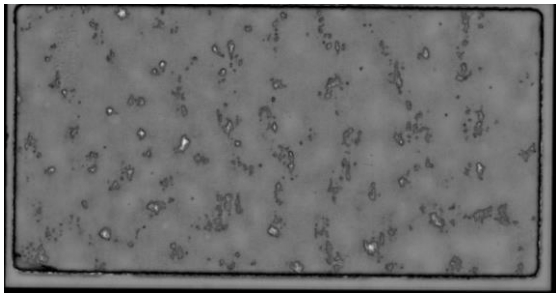
Top surface

0.4/0.635/0.4 mm AlN DBA
0 hour SAM image

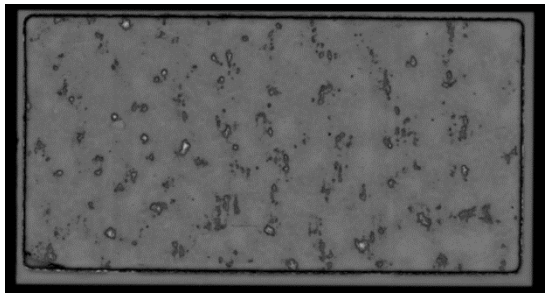


0.4/0.635/0.4 mm AlN DBA
3000 hour SAM image

Center slice of aluminum layer



0.4/0.635/0.4 mm AlN DBA
0 hour SAM image

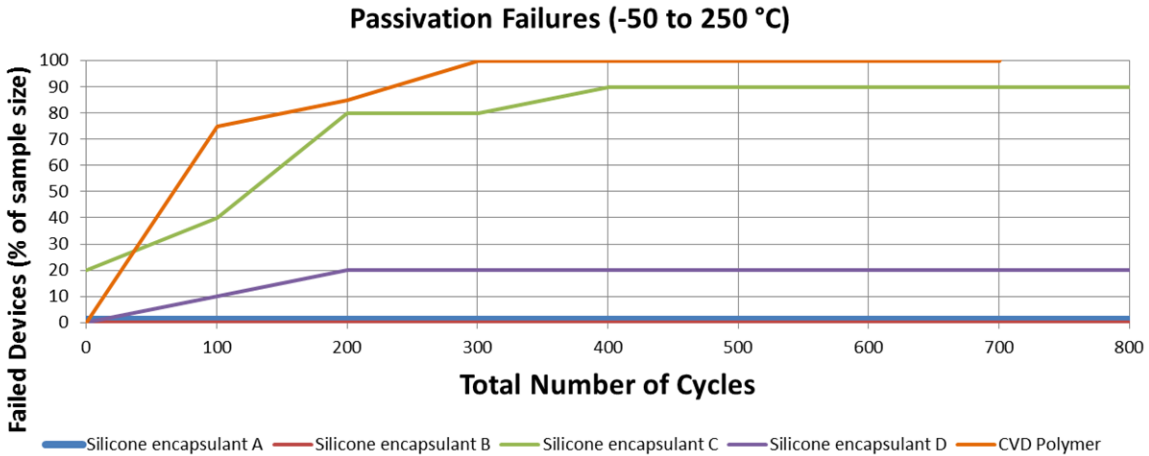


0.4/0.635/0.4 mm AlN DBA
3000 hour SAM image

Thermal Cycling

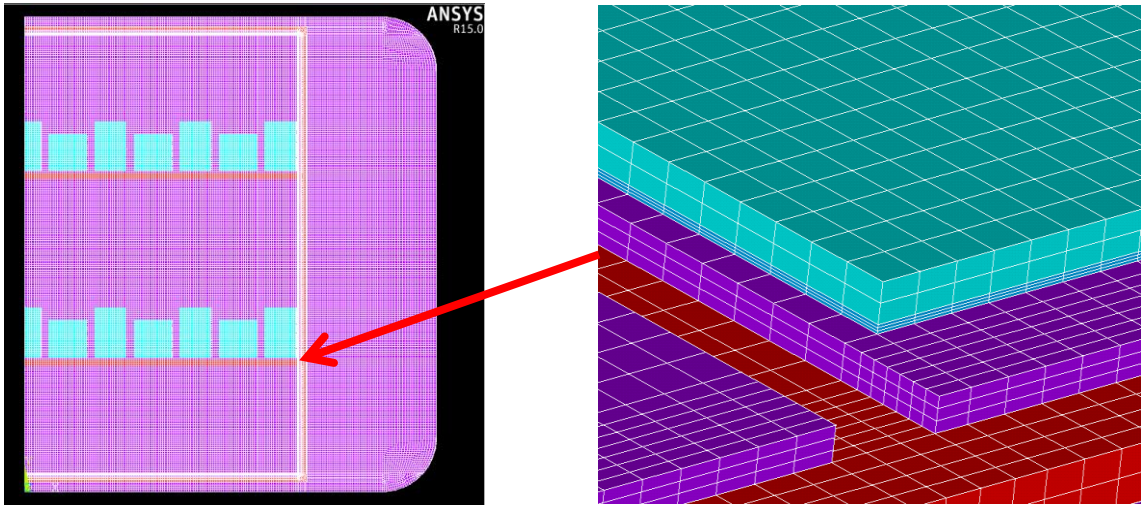
Expansion and contraction of passivation materials during thermal cycling can cause degradation.

Failure mode and rate is highly dependent on passivation material, geometry of product, and thermal cycle profile.



Module Design for Reliability

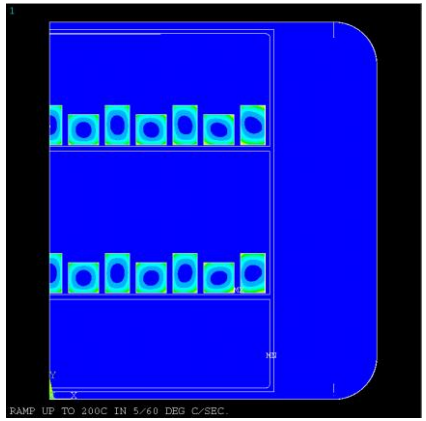
Thermomechanical Model: Loading Conditions



- Used a half-symmetric model of the power module
- Loading conditions:
  - -40°C to 200°C thermal cycle
  - 5°C/min ramp rate
  - 15 min dwell time

Die-Attach Results – Strain Energy Density

Configuration No	Baseplate	Substrate	Vol. Avg. Creep Strain Energy Density /Cycle (MPa)	Max. Strain Energy Density – Accumulated (MPa)
1	Cu	Si_3N_4	0.23	3.82
2		AlN	0.23	3.77
3	AlSiC	Si_3N_4	0.13	2.13
4		AlN	0.15	2.48



Strain-energy density

- *AlSiC baseplate with Si_3N_4 substrate configuration is the best choice.*

Testing of Module Design

HALT Test Method

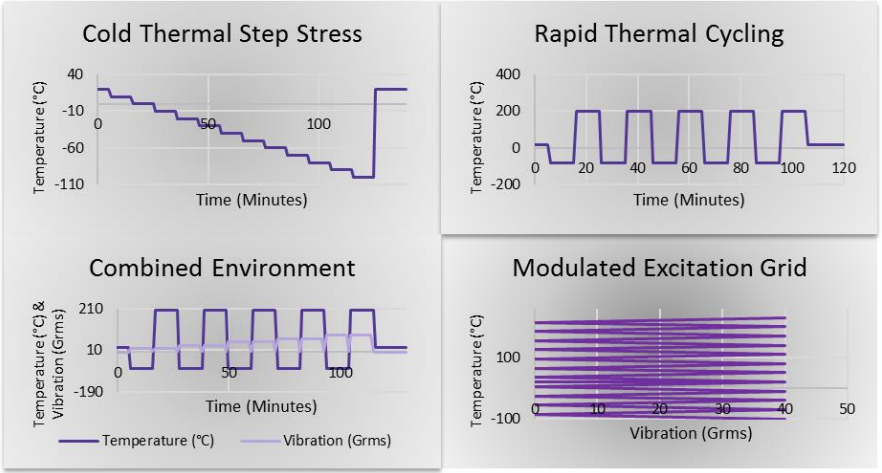
Reliability test method focused on finding product defects

HALT testing is a product improvement method, not a product qualification method

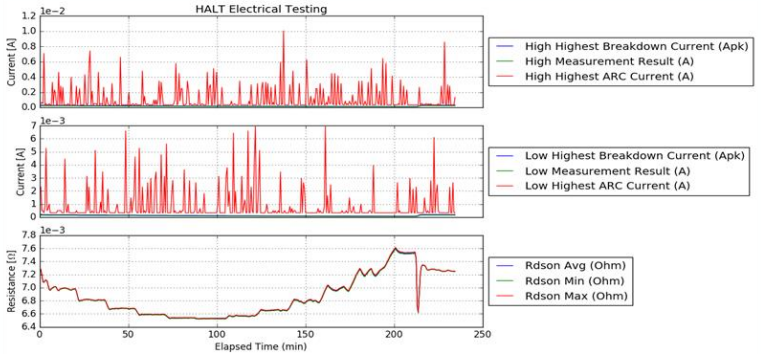
Reveal defects in a matter of hours/days compared to weeks/months with traditional reliability tests

Performing HALT

- Profiles
  - Cold Thermal Step Stress
  - Hot Thermal Step Stress
  - Rapid Thermal Cycling
  - Vibration Step Stress
  - Combined Environment
  - Modulated Excitation



- Power Module Monitoring
  - HiPot Testing
    - Voltage Blocking
    - Arc Detection
  - Rdson



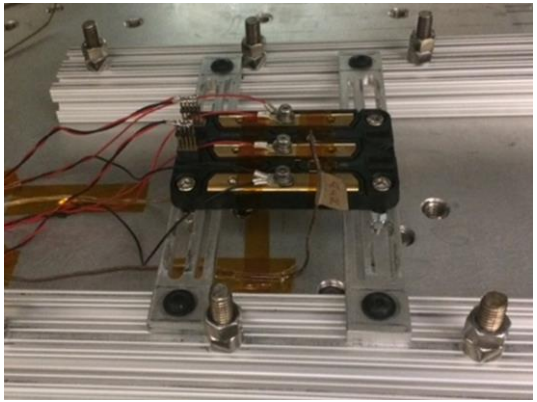
HALT Utilization

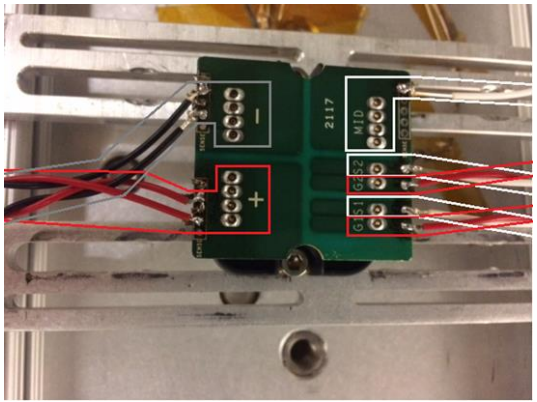
- **HALT is a product development tool used to excite rapid failures that can determine areas of improvement:**
  - Mechanically
  - Electrically

- Development Phase:
- Spot design weaknesses
  - Test early and often between revisions

- Product Improvement:
- Find the next point of failure
  - Creates product robustness
  - Continue to test and improve until the module is sufficiently rugged

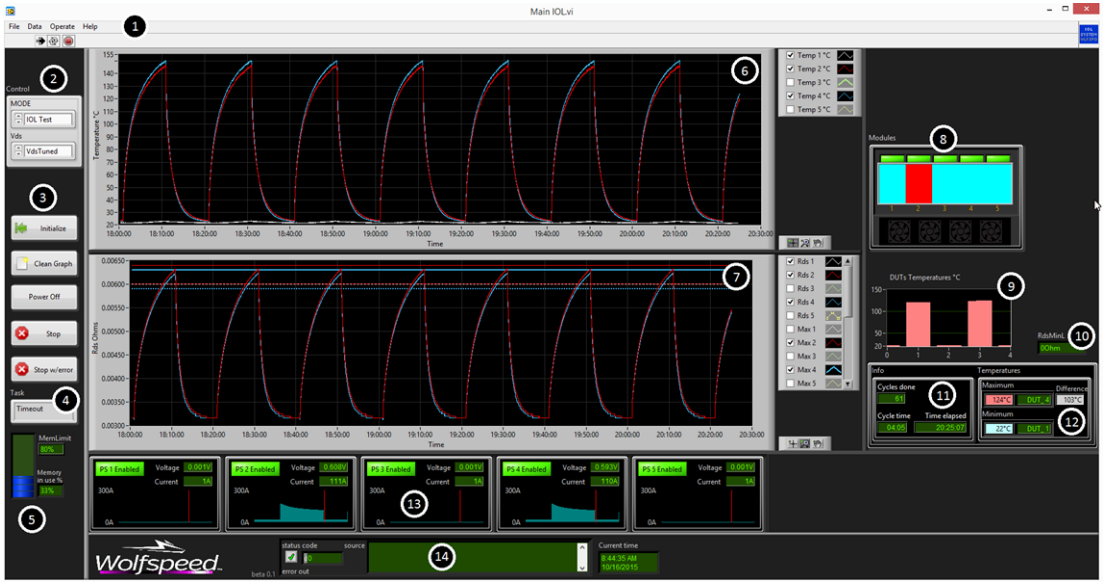
- Accelerated Reliability Testing:
- Find early lifetime failures
  - Precipitates failures faster than standard lifetime testing
  - Lower number of failures in the field





Intermittent Operational Lifetime

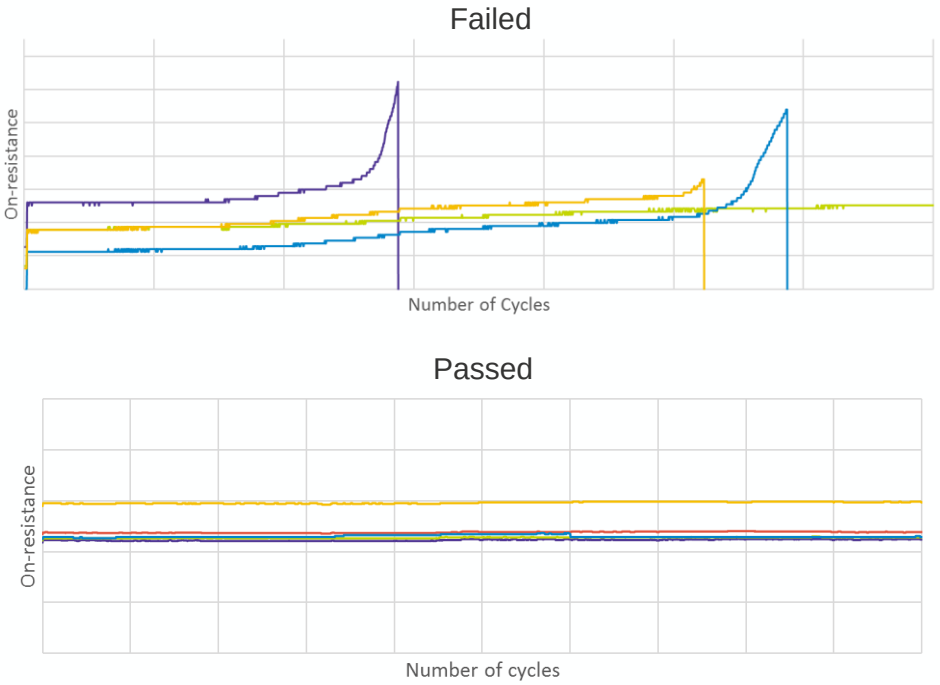
- Thermal excursions are due to device heating that propagates throughout the package.
- Thermal ramp profile for IOL is on the order of minutes, e.g., 10 minute ramp up, 10 minutes ramp down.



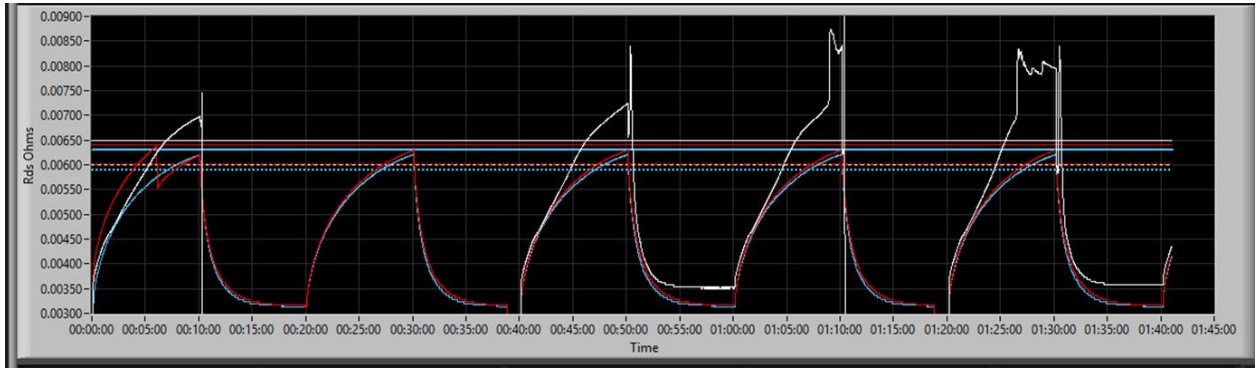
Intermittent Operational Lifetime

The IOL test causes high thermal gradients from junction to case during ramp up/down due to the lack of a thermal management system.

- Case reaches near junction temp during end portion of ramp
- Large amounts of stress across all interconnects due to high ramp rates



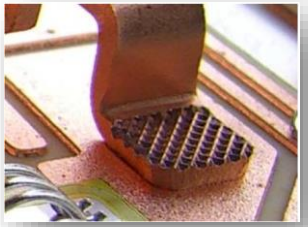
Intermittent Operational Lifetime

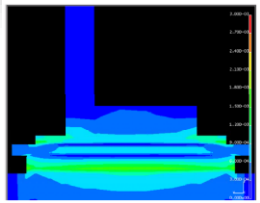


Sudden shifts in on-resistance can indicate an intermittent gate connection.

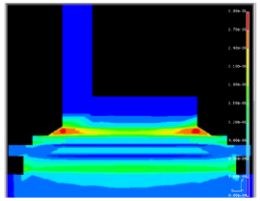
Intermittent Operational Lifetime

- Ultrasonic welding provides very strong, reliable, high current bond between a power terminal and substrate pad
- Relatively fast, room temperature process
- The attach process can be performed at anytime during the assembly process → higher density packaging due to the reduction in wire bond head clearance
- Stresses now move into other layers, e.g., substrate metal/ceramic interface.





(a) Ultrasonic Welding



(b) Soldering

K. Kido, F. Momose, Y. Nishimura and T. Goto, "Development of copper-copper bonding by ultrasonic welding for IGBT modules," *2010 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT)*, Melaka, 2010, pp. 1-5.O. Tamm, “New Packaging Technology enabling High Density Low Inductance Power Modules,” Bodo’s Power Systems, May 2014, pp.1-3.

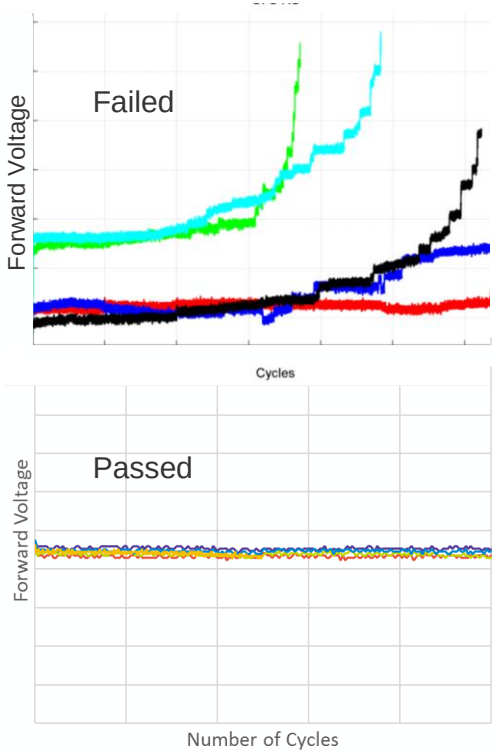
Power Cycling

- Thermal excursions are a result of device heating and are localized to the immediate die area due to the module being mounted to a cold plate.

Pulse widths are on the order of seconds (Pc_{sec}) or minutes (PC_{min}).

Large thermal gradients are seen near the die in the thermal path and wire bonds.

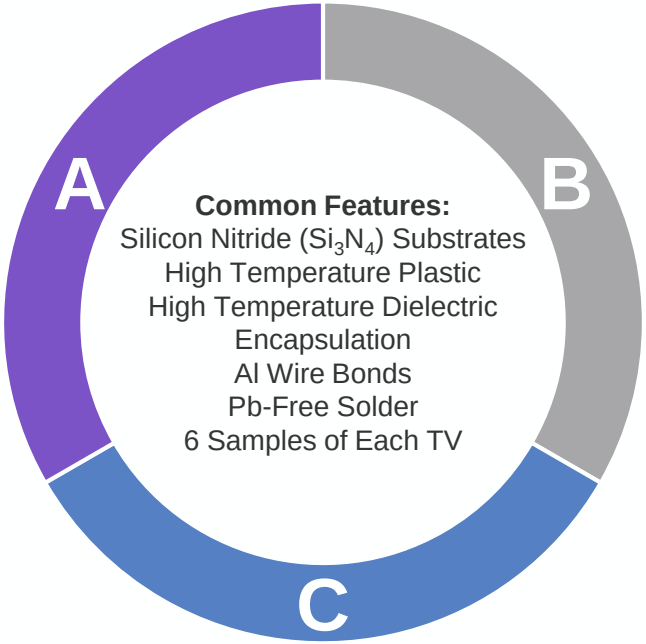
Common failure mechanisms are wire bond lifts at the die and R_{th} degradation.



Power Cycling - Test Vehicle Study on Production Stackups

Sn-Rich Solder + AlSiC Baseplate

Sn-Rich Solder + Cu Baseplate



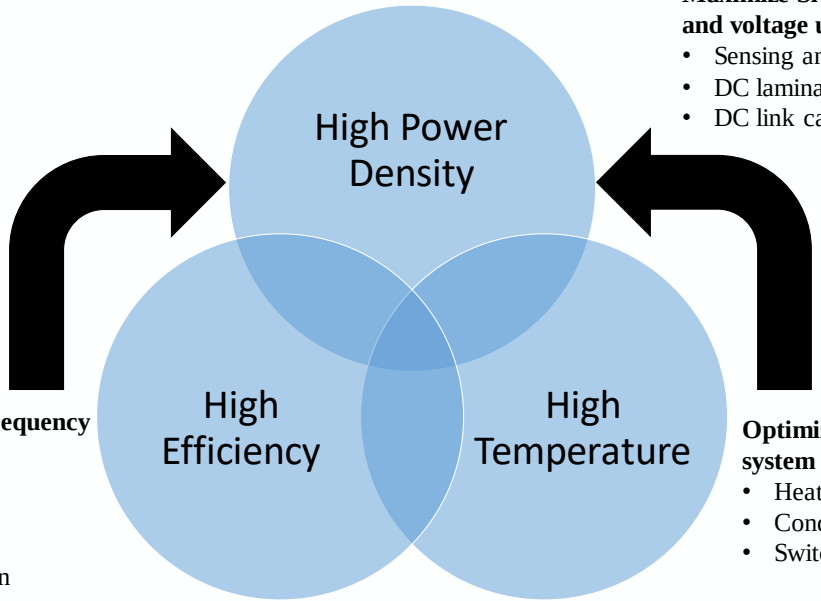
Au-Rich Solder + Cu Baseplate

Lauren Kegley
Modeling & Reliability Session
Thursday 4:45 PM

System Considerations

System Attributes and Interplay of Converter Subsystems of Interest

Optimization approach allows the end user to cover the extreme points of the solution space to maximize the advantage that SiC-based systems can offer

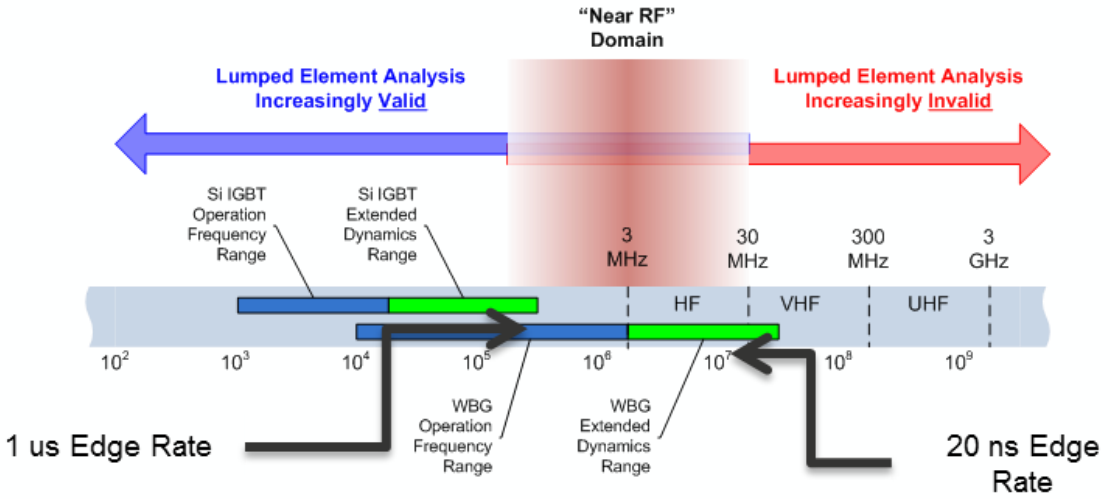


Maximize SiC MOSFET current and voltage utilization
- Sensing and controls
- DC laminated bus
- DC link capacitors

Optimum switching frequency
⇑ Power module
⇑ EMI filters
⇑ CM & DM filters
⇑ Switching losses
⇑ Gate drive design

Optimize thermal management system based on loss analysis
- Heat sink / Cold plate design
- Conduction losses
- Switching losses

Power Electronics: Spectral Considerations

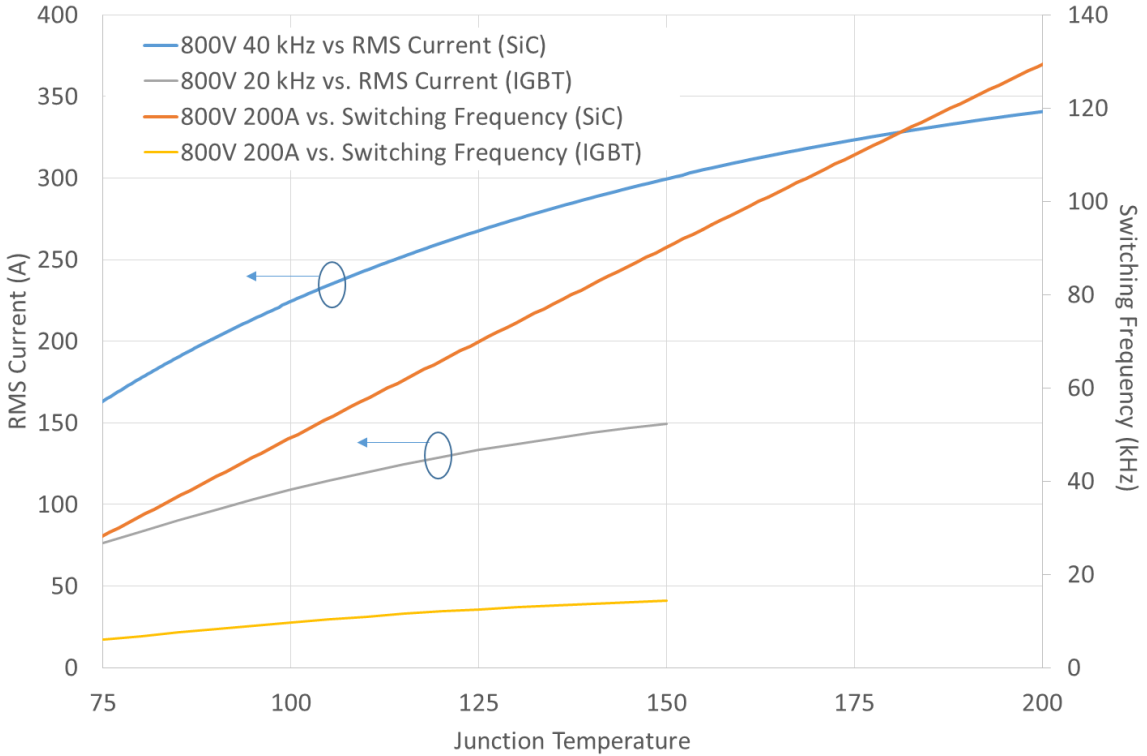


- Traditional IGBT-based systems:
  - Operation Frequencies to ~50 kHz
  - Easily-suppressed extended dynamics
  - Lumped circuit analysis works well
  - Packaging impedances are not critically important

- WBG-based systems:
  - Operation Frequencies to a few MHz
  - Extended dynamics to ~50 MHz
  - Lumped circuit analysis in question
  - Packaging impedances are critically important in "Near-RF" domain

Courtesy Prof. Andy Lemmon, Dept. of Electrical & Computer Engineering, The University of Alabama

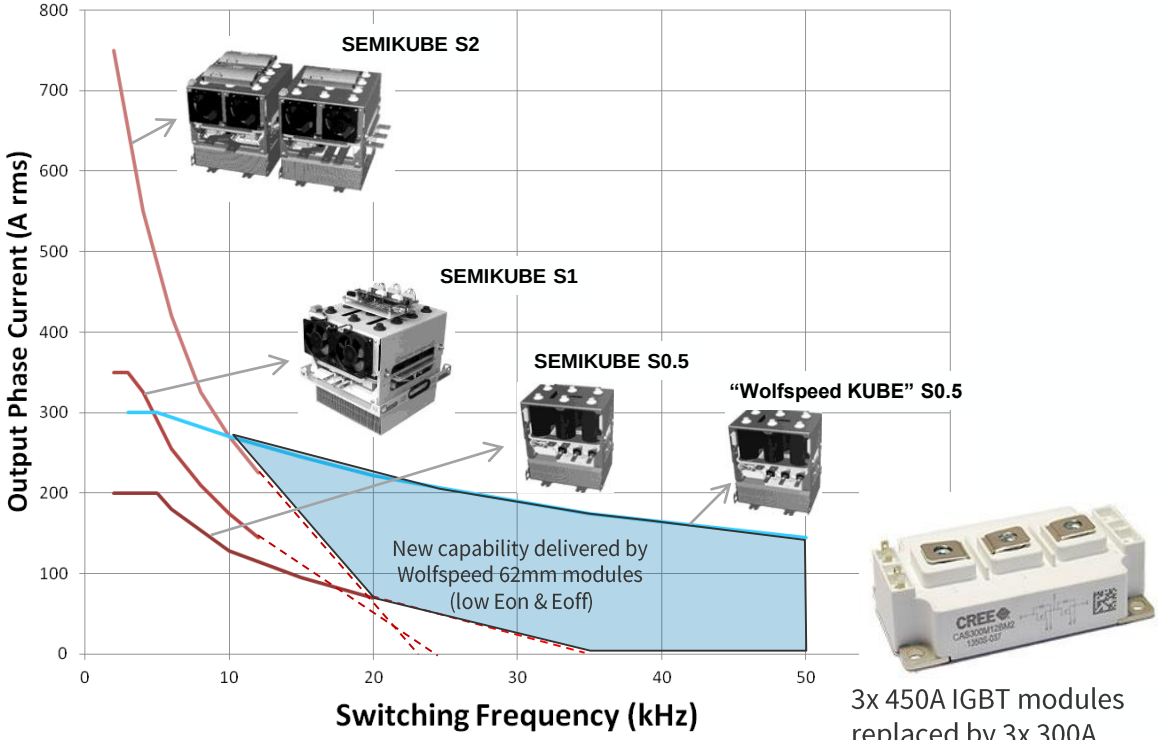
Higher T_{jmax} for Increased T_{Amb}/T_{Liq}, Increased F_{sw}, or Increased Current



25 °C case assumed

WOLFSPEED S0.5 Kube Enables High Frequency Operation

Outperforms All SEMIKUBE Products at f_{sw} > 10 kHz



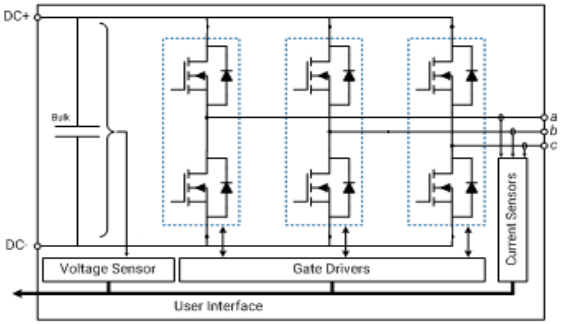
3x 450A IGBT modules replaced by 3x 300A Wolfspeed All-SiC modules

250 kW SiC Three-phase Evaluation Unit

INCLUDES

- Three 900 V HT-3291-VB High Performance Half Bridge Power Modules
- Three ITGD2-3011 SiC-Optimized Companion Gate Drivers
- Ultra-Low inductive (~3.3 nH) DC Laminated Bus Bar
- DC Link Film Capacitors
- Voltage & Current Sensing
- Liquid-Cooled Cold Plate

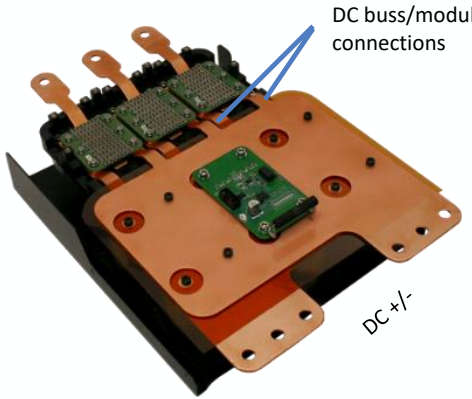
USES THE NEW CRD200DA12E REFERENCE DESIGN – OPTIMIZED FOR 900 V – 1700 V VARIANTS OF THE HT-3000 MODULE



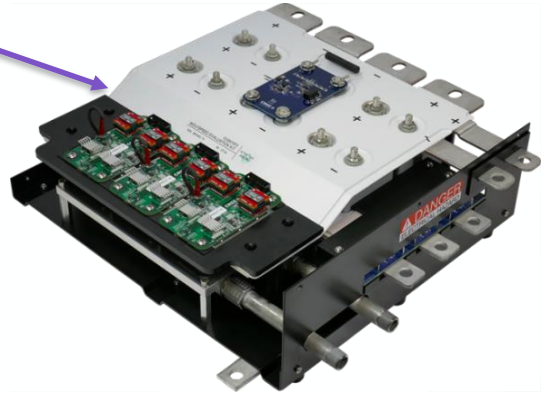
MAXIMUM RATINGS FOR THE 900 V SYSTEM

Nominal DC Link Voltage	800 V
RMS AC Phase Current Output	300 A
Fundamental Output Frequency	4 kHz
Max Coolant Temperature	70 °C
Storage Temperature	-55 °C to 85 °C
Dimensions (L x W x H)	16.6 in x 11.5 in x 5.2 in
Weight	35.2 lbs / 16 kg

3-Phase Inverter Design for Increased Power Capability

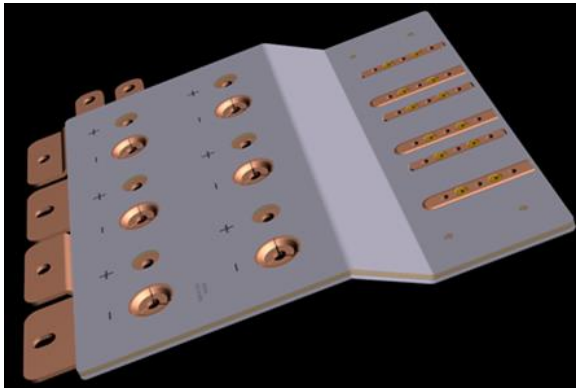


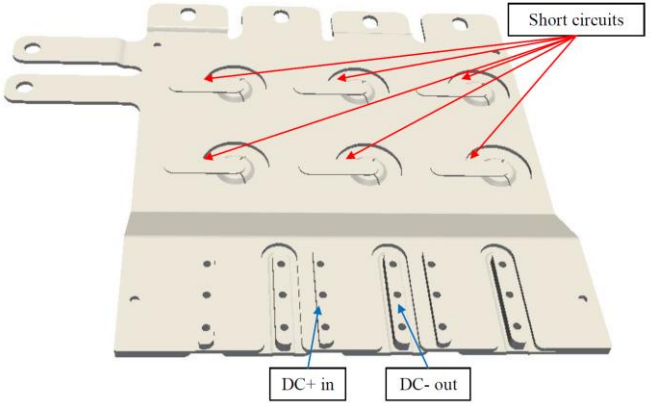
Design with non-optimized DC laminated Bus structure



Design with optimized DC laminated Bus structure

DC Bussing is a Multi-Physical Design Problem





Electrically, the DC bus needs low:

- ESR (i.e., high conductivity material, “large” cross-sectional conduction area)
- ESL (i.e., thin and wide “planes”) structure
- Higher Density Module complicates the issue

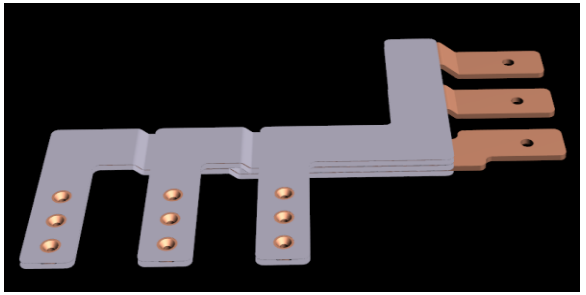
- Thermally, DC bus needs a low temperature rise (e.g., < 80°C from room temperature) for maximum expected rms current passing through the structure is required.
- Mechanically, a high level of robustness against normal shock and vibration during use is required

Meshing of the DC laminated bus structure

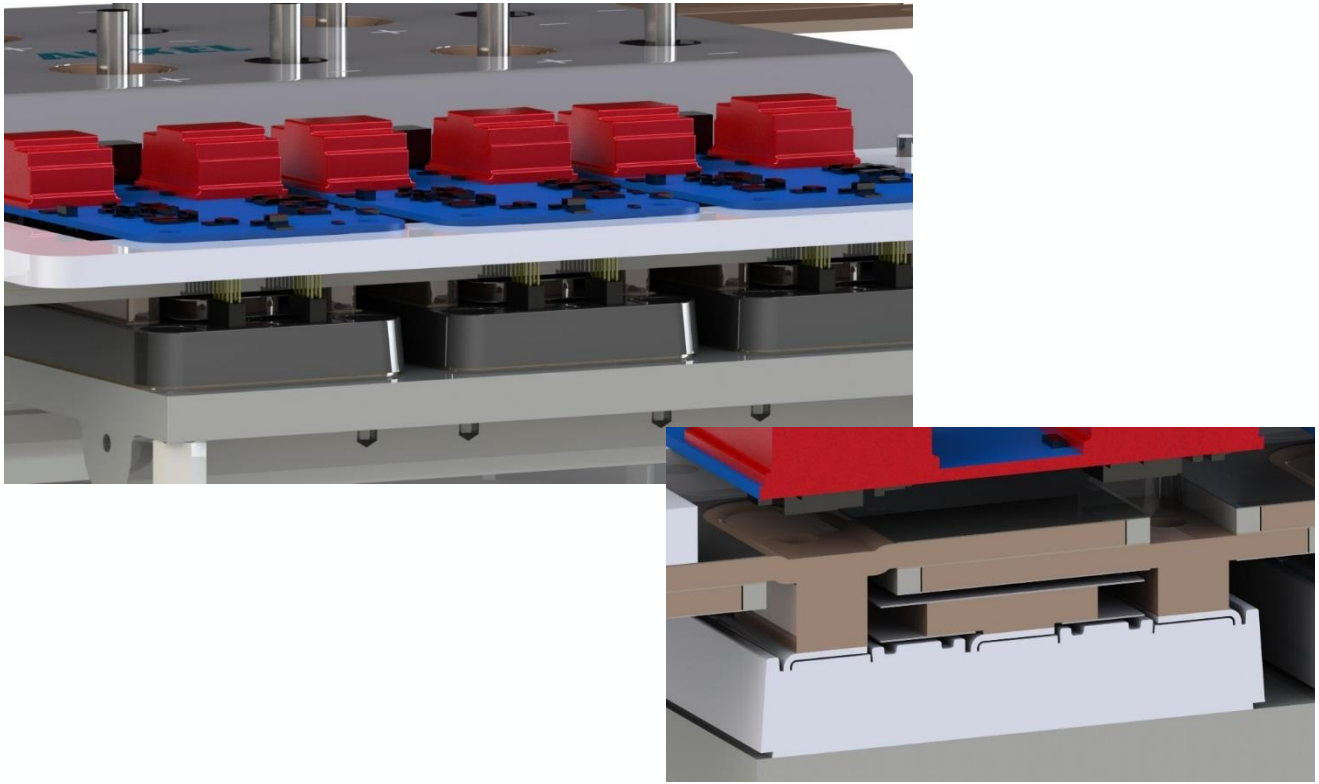
- 11 million elements , 6 Hrs.
- Ultra-fine to account for frequency dependent skin and proximity effects
- Calculation time ~ 20 Hrs.

AC Bussing Design Less Complex for 3-Phase Inverter

- Electrically, needs to have a low ESR
  - (i.e., high conductivity material, “large” cross-sectional conduction area) structure
- No real design constraint on the AC output bus bar inductance (i.e., ESL). ESL of output phase appears in series with its respective phase inductance
- Thermally, need low temperature rise at maximum RMS current output of >325 A rms
  - Rise of 80°C maximum is permitted to not degrade the dielectric-copper adhesive which is rated to 105°C

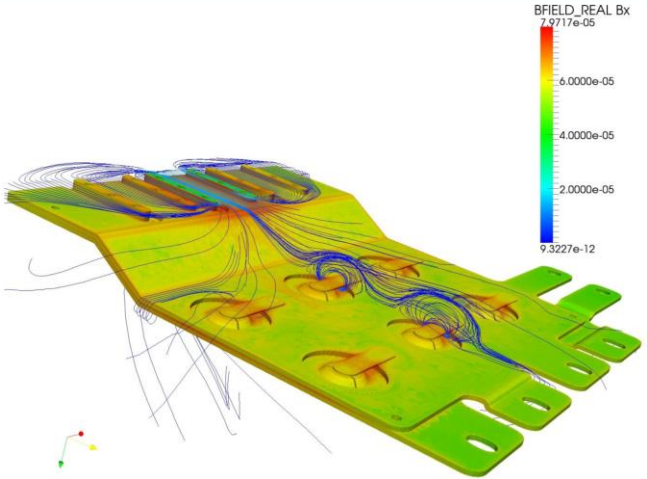


Low Inductance Modules & Bussing Need Careful Stack-Up Implementation



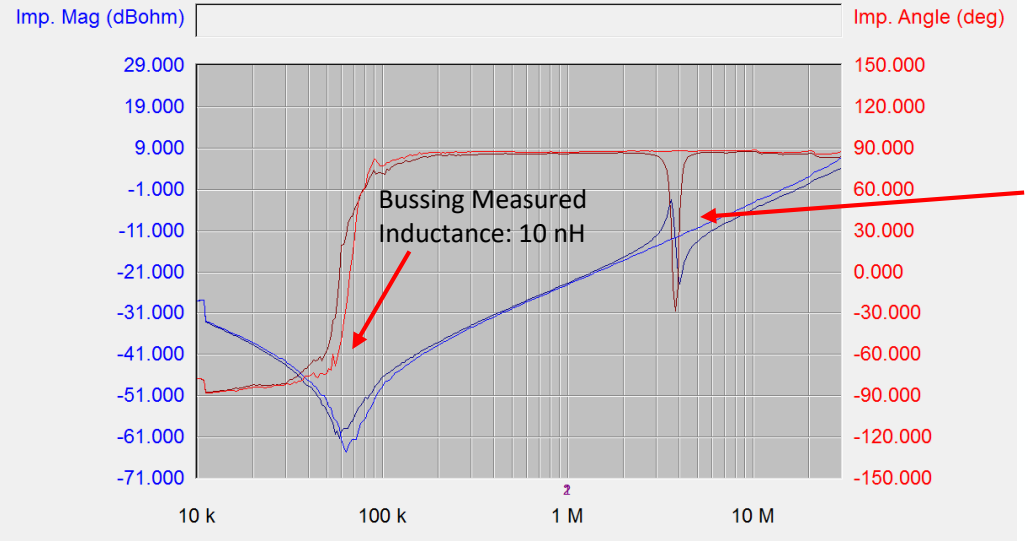
Magnetic Field Component B_x of B

- Complex-valued test current phasor $\mathbf{I}_{test} = 1 \angle 0°$ A injected between “DC+ in” and “DC- out” terminals
- $\mathbf{V}_{test} = \mathbf{Z}_{Th}\,\mathbf{I}_{test}$,
- The module input-output (I/O) port is $\mathbf{V}_{test} = \mathbf{Z}_{Th}$. The stray inductance value is calculated by $\mathrm{Im}\{\mathbf{Z}_{Th}\} = \mathrm{Im}\{\mathbf{V}_{test}\} = j\omega L_\sigma\ \Omega = 1.11014\times10\text{E-}2\ \Omega$. or $L_\sigma = 3.53$ nH.



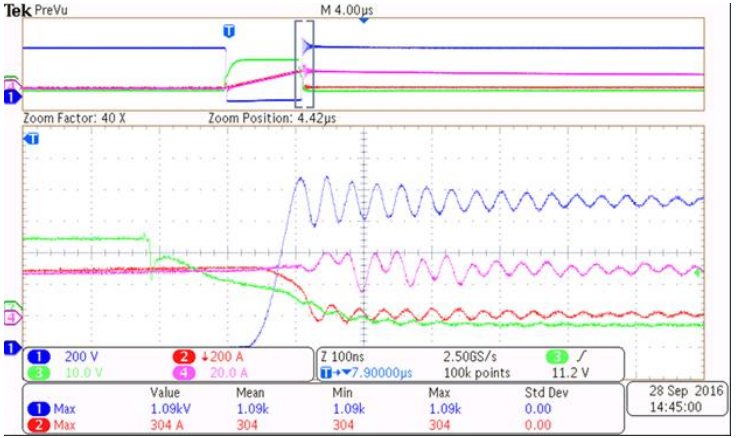
250 kW Evaluation Kit Equivalent DC Bus Measurements

Snubbers can lower effective inductance, but introduce potential oscillation

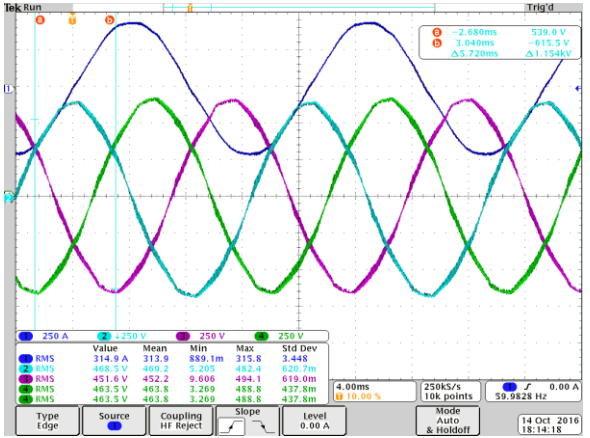


Bussing with Snubber Effective Inductance: 6.8 nH

1200 V-Based, 250 kW 3-Phase Inverter



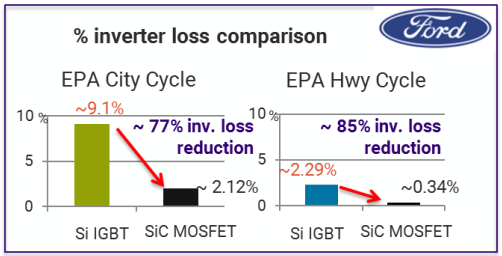
Single-phase test, a 900 VDC bus and turn-off at 304 A demonstrates an ultra-low overshoot



Inverter 3-phase voltage and phase current for 250 kW at f_{sw}=20 kHz & 700 VDC bus demonstrating clean switching waveforms

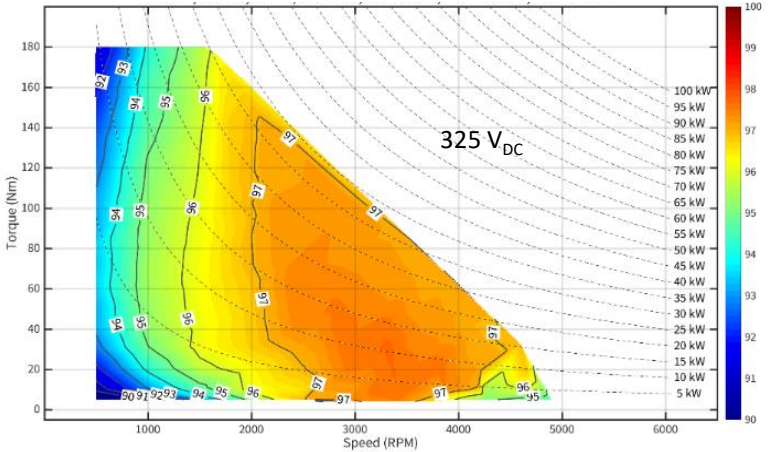
900 V Inverter Outperforms DoE VTP Efficiency Target of >93%

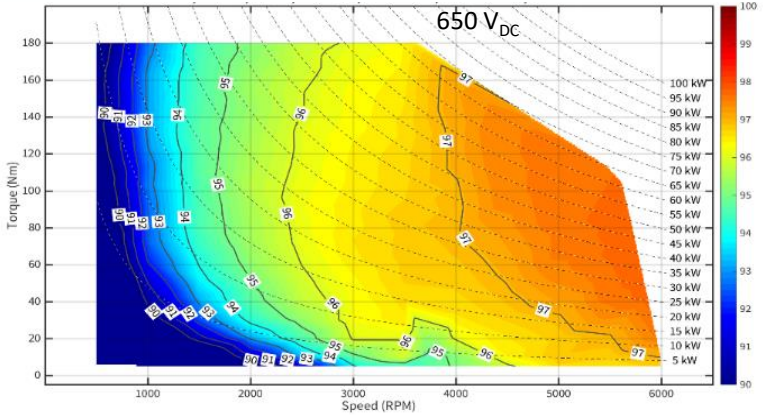
	AVERAGE EFFICIENCY	PEAK EFFICIENCY
200 V_{DC}	95.72 %	97.29%
325 V_{DC}	95.98 %	97.52%
450 V_{DC}	95.74 %	97.61%
650 V_{DC}	95.79 %	97.58%
Overall	95.56 %	97.52%



Ref. M. Su, et al, WiPDA 2016

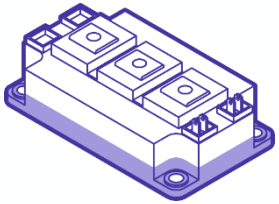
DOE Contract EE0006920





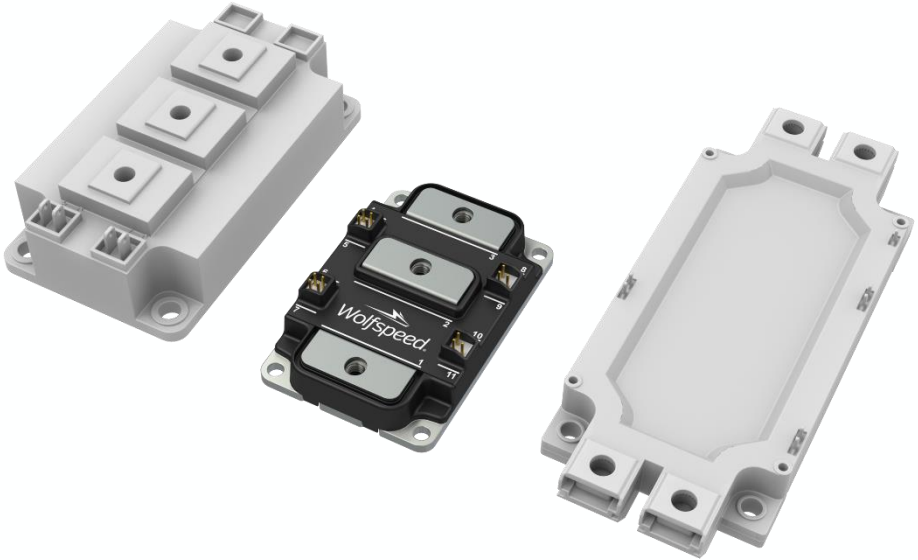
Testing limited to 88 kW capability of Dyno

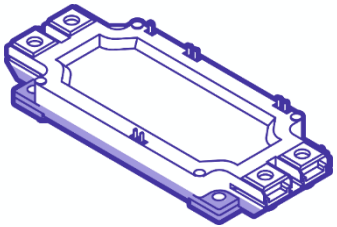
Next Gen Modules Targeting Power Density



Volume

66% Less



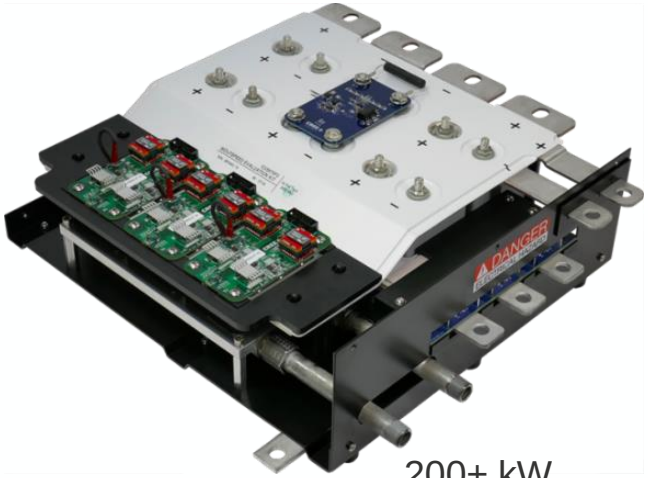


Volume

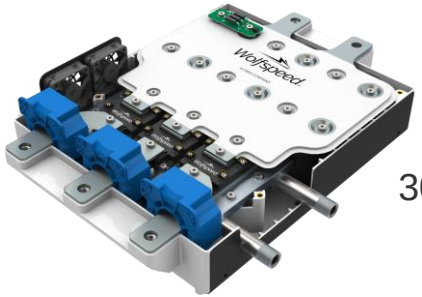
60% Less

XM3 Platform Targets Optimized Designs for Quick-Start

- Form-factor fitting gate drivers
- Integrated protections for temperature, overcurrent and UVLO
- 300 kW three-phase inverter
- Integrated LEM closed-loop current sensors
- Modular controller integration inside enclosure
- Liquid-cooled cold plate
- Enables Quick-Start with minimal engineering time required



200+ kW

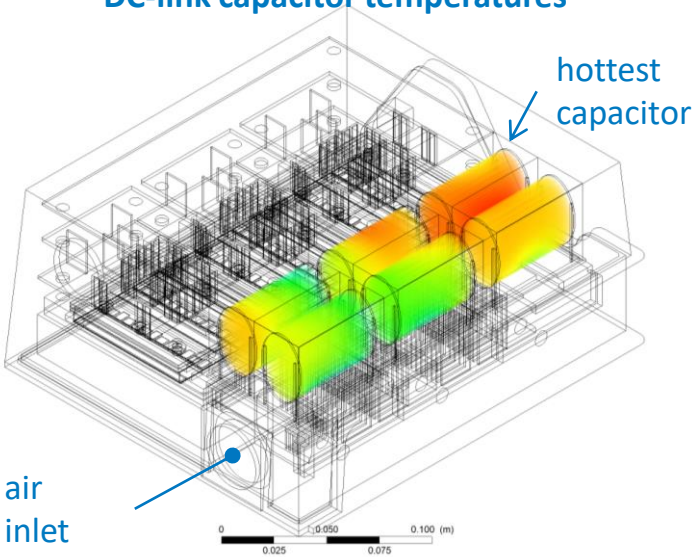


300 kW

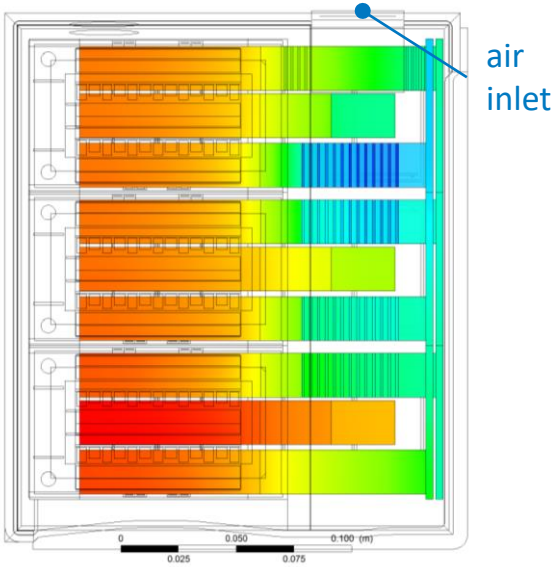
Not to scale

CFD Results: Component Temperatures

DC-link capacitor temperatures



Bus bar temperatures

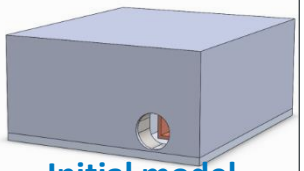


- Hottest capacitor is the one furthest from the inlet—no heat sink on its bus bar
- Heat conducted from power modules via bus bars

CFD Results: Maximum Component Temperatures

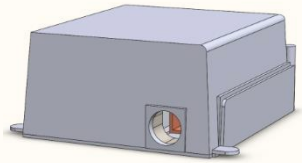
Component	Inlet Air Temperatures: 50°C	
MOSFETs	**114.0**	**114.1**
DC capacitors	**94.0**	**88.0**
Snubber capacitors	**104.8**	**96.1**
Electrical boards	**97.1**	**97.0**
Air temperature	**123.5**	**120.0**

140°C under-hood temperature, 30 kW steady-state operation



Initial model

- Low-capacity fan



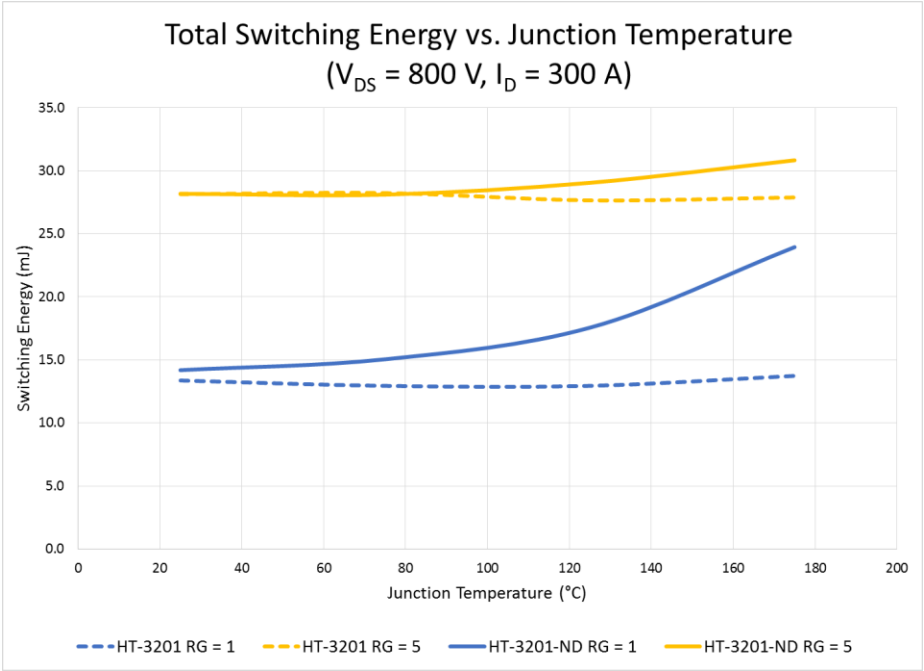
Modified model

- High-capacity fan
- Heat sinks on bus bars

Snubber capacitors and electrical boards within their allowable temperature limits (< 125°C)

Utilization of Gen2 Body Diode for Performance/Cost Trade-off

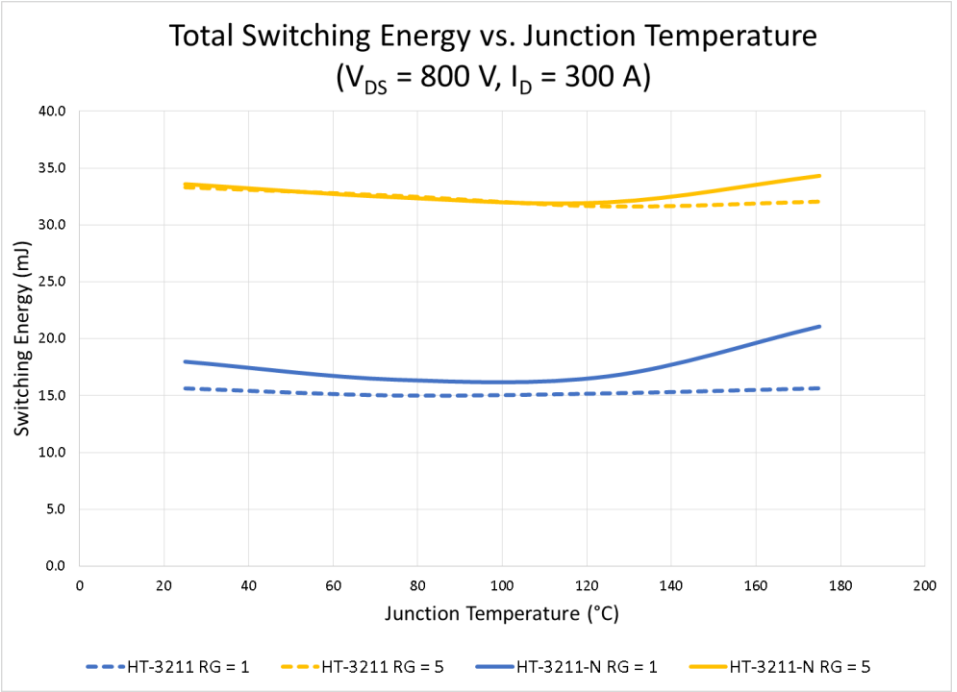
- HT-3000 module used in 250 kW 3-phase inverter with Gen2 1200 V FETs/diodes
- In the HT-3201 module nearly half of the real estate is occupied by diodes.
- Body diode fully qualified, and does not experience V_f degradation
- The elimination of the Schottky diodes has little effect at $R_G = 5\ \Omega$
- At 175 °C there is a difference of 10 mJ in total switching loss, which corresponds to an extra 200 W of loss at 20 kHz



Solid – Body Diode Used
Dashed – Anti-Parallel Schottky Diodes

Gen3 Modules With & Without SBD in Parallel

- The elimination of the Schottky diodes have little effect at RG = 5 Ω
- At system level, room for optimization of Rg vs loss
  - Must consider voltage overshoot for Lsystem
- At 175 °C there is a difference of 5 mJ in total switching loss, which corresponds to an extra 100 W of loss at 20 kHz



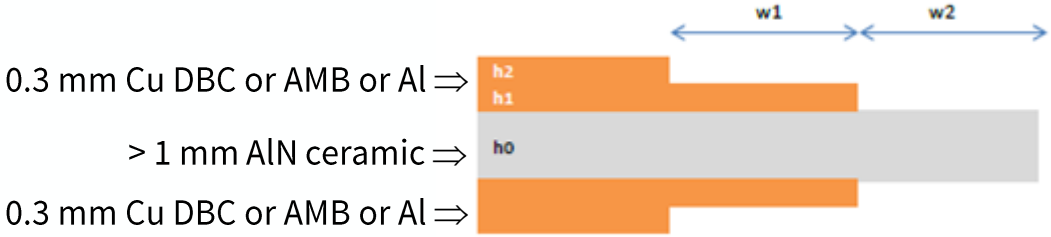
Solid – Body Diode Used
Dashed – Anti-Parallel Schottky Diodes

Medium Voltage Considerations

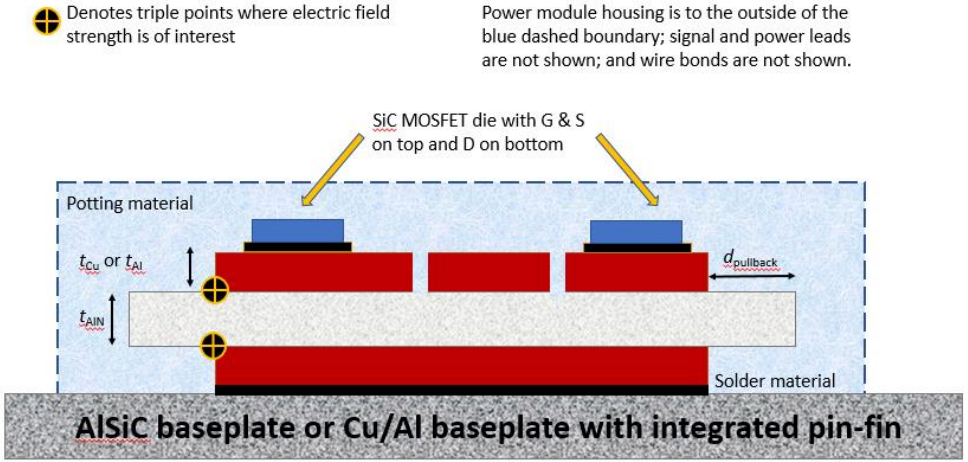
Electrical Concerns

1. Insulation Coordination
   - Creepage
   - Clearance
   - External vs. internal
2. Dielectric Test / “High-Pot” Test
   - Vertical Isolation
   - Lateral Isolation
   - Need for testing beyond 50/60 Hz
   - Testing at temperature
3. Partial Discharge Test
   - PD inception voltage
   - PD extinction voltage
   - Need for testing beyond 50/60 Hz
   - Testing at temperature

$$T_{ceramic} \in [20\ °C \ldots 200\ °C]$$

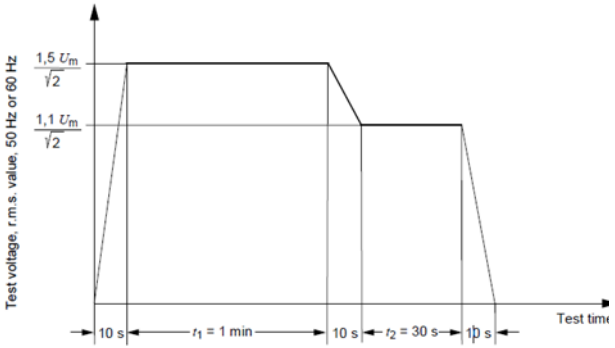


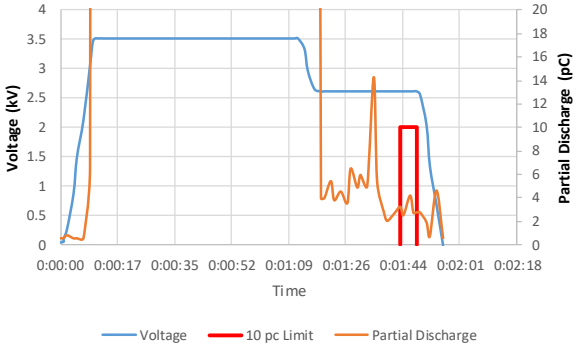
Power substrate structure within a MV power module



Design Considerations

- Application specific
  - Electro-, Thermal-, Mechanical
- DBC vs. Cu AMB
- Need for dimpling
- Metal etching to improve
- E field management
- Soldering/Brazing vs. US welding





Material	Thermal Conductivity W/mK @ 20°C	CTE ppm/K @ 20°C	Lifetime – Cycles Without Dimples★ Cu/Ceramic/Cu (mm)	Lifetime – Cycles with Dimples★	Dielectric Constant @ 1 MHz	Dielectric Constant @ 1 GHz	Dielectric Strength, ASTM D116, kV/mm (AC)	Dielectric Strength, JIS C 2141, kV/mm (AC)	Ceramic Thickness (0.635 mm)	Ceramic Thickness (1.00 mm)
Al_2O_3	24	6.8	> 65 0.3/0.32/0.3	~650	9.8	10.0	15	15	×	×
Si_3N_4	54	2.5	> 5000 0.5/0.32/0.5	~50,000	8.0	7.5	17.7	12	0.32 mm	
AlN	170	4.7	> 35 0.3/0.635/0.3	~350	9.0	7.5	15	14	×	×

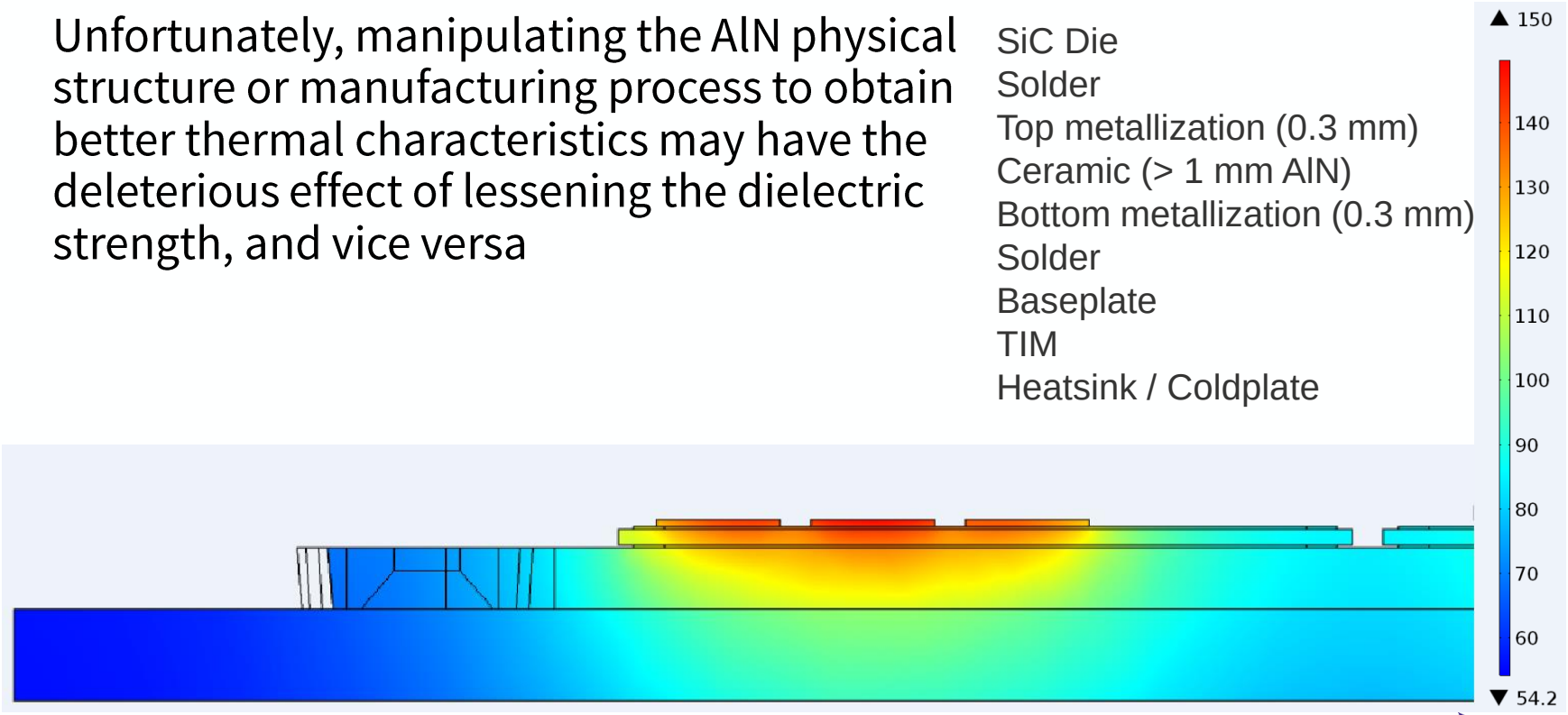
Source: Curamick Ceramic Substrates, DBC technology, Design Rules, Version 12/2014.
Blue shaded columns contain results in Fluorinert or some other kind of engineered dielectric fluid.
★ Lifetime measurement conditions: -55 °C to 150 °C thermal shock testing

Thermal Concerns

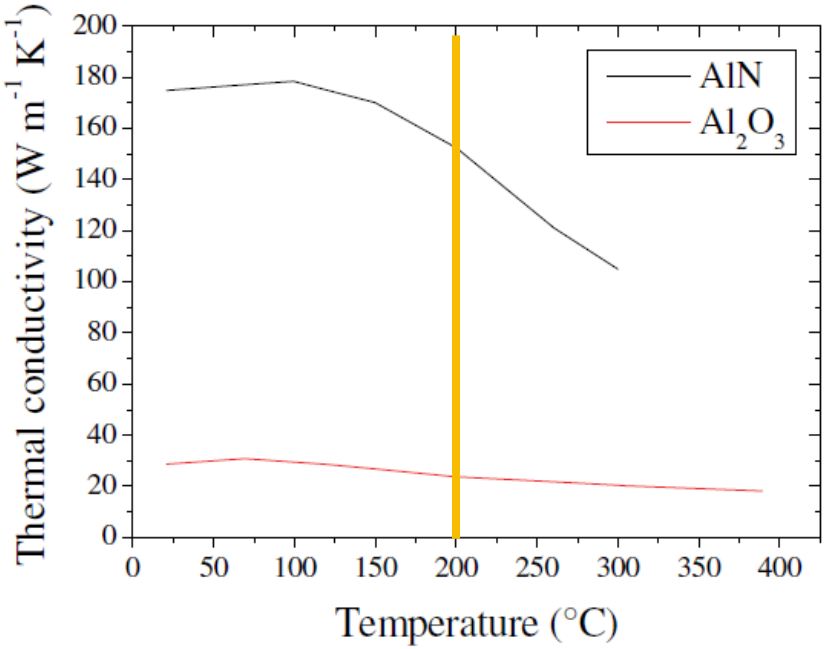
Unfortunately, manipulating the AlN physical structure or manufacturing process to obtain better thermal characteristics may have the deleterious effect of lessening the dielectric strength, and vice versa

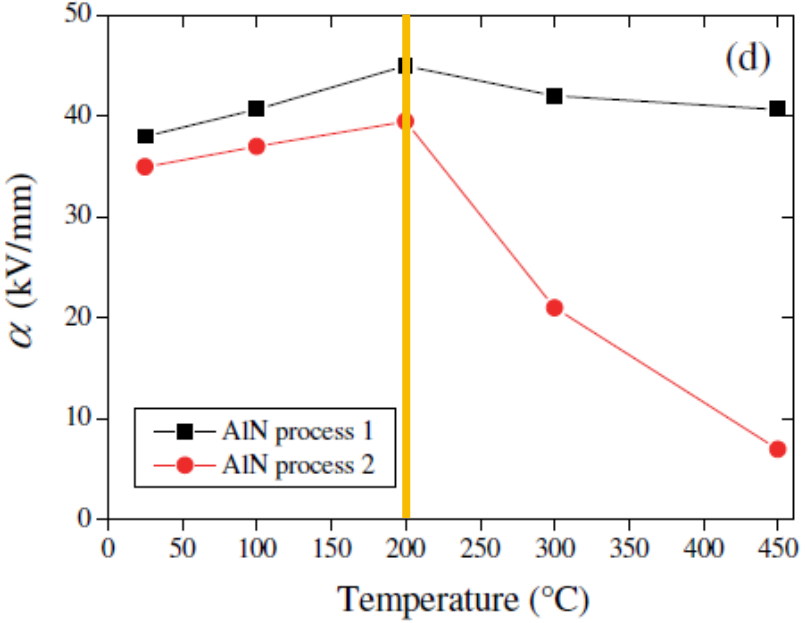
Layers (Top to Bottom)

SiC Die
Solder
Top metallization (0.3 mm)
Ceramic (> 1 mm AlN)
Bottom metallization (0.3 mm)
Solder
Baseplate
TIM
Heatsink / Coldplate



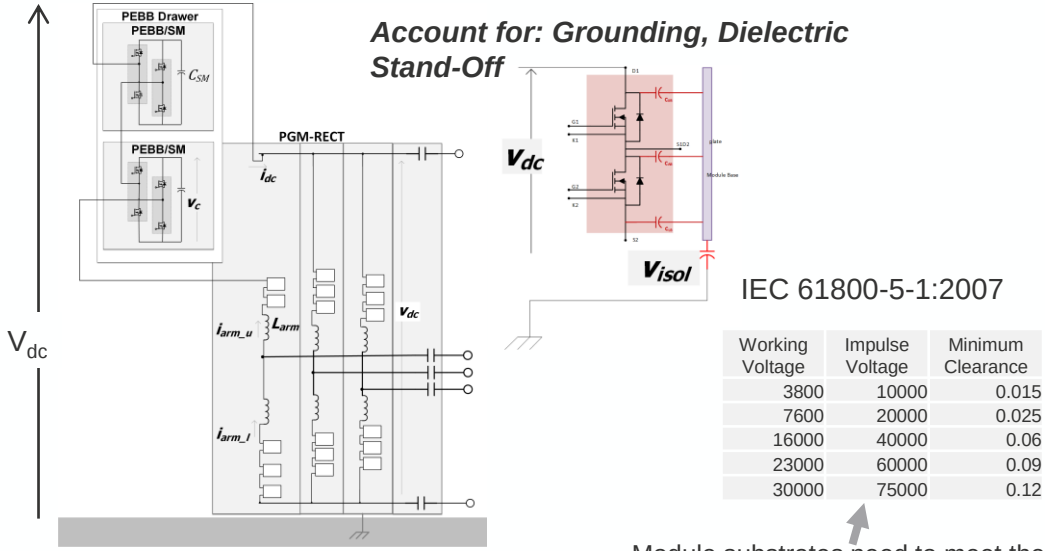
Thermal Concerns





Sombel Diaham, Marie-Laure Locatelli and Zarel Valdez-Nava (2011). Dielectrics for High Temperature SiC Device Insulation: Review of New Polymeric and Ceramic Materials, Silicon Carbide – Materials, Processing and Applications in Electronic Devices, Dr. Moumita Mukherjee (Ed.), ISBN: 978-953-307-968-4, InTech.

Dielectric Stand-Off vs. Module Substrate Voltage Rating



Courtesy Prof. Cuzner, UW-Milwaukee

IEC 61800-5-1:2007

Working Voltage	Impulse Voltage	Minimum Clearance
3800	10000	0.015
7600	20000	0.025
16000	40000	0.06
23000	60000	0.09
30000	75000	0.12

Module substrates need to meet these values to avoid additional stand-off distances from the drawer frame

Conclusion

Conclusion

- SiC power devices have some unique reliability considerations in addition to Si power devices
- Reliability assessments need to be comprehensive and specific
- The SiC failure mechanisms have been identified and testing methods have been developed, but more work needs to be done
- Successful product qualifications and field reliability show that the reliability science is paying off, and SiC is ready for large volume manufacturing for high reliability applications
- Industry-wide reliability guidelines and standards are being actively developed
- System level constraints increase, the “Near RF” domain require careful consideration
- Medium Voltage creates challenges with subcomponent optimization, dV/dt, and the proper balance of system integration/component integration