The Increasing Importance & Challenges of Packaging in The 21st Century

Chuck Richardson, iNEMI
Topics

• iNEMI Introduction
• Roadmap Process Overview
• 2017 Packaging & Component Substrates TWG Scope & Highlights
• Packaging Technology Needs & Gaps
• Proven Industry Collaboration Model
• How to Get Involved
• Back-up - Project Examples
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ASM

Assembléon

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ASE GROUP

Fiber QA LLC

ALENT

Dow

HOVER·DAVIS

Heraeus

iST Integrated Service Technology

hillcrest labs

Experts in Motion

FIT

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- Moldex3D
- Shengyi Sci. Tech
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- Indium Corporation
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- Nippon Micrometal Corporation
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- MST
- Micro Systems Technologies
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calce

Exponent

DfR Solutions

Green Electronics Council

CEA Leti

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Berkeley University of California

CIT Center for Innovative Technology

Compliance & Risks

ECIA Electronic Components Industry Association

Georgia Institute of Technology

INEMI
Methodology

- Technology Evolution
- Product Needs
- Government
- Research
-gap
- Disruptive Technology
- Academia
- Projects
- Competitive Solutions
- Available to Market Place
- Global Industry Participation
- Industry Solution Needed
- No Work Required
- iNEMI Members Collaborate
Industry Led Teams

• Technical Working Group Teams
  – Develops the roadmap technology chapters
  – Presently 21 Teams and Chapters

• Product Emulator Group Teams
  – “Virtual Product”: future product attributes plus key cost and density drivers – Presently 7 Teams and Chapters
    • Portable / Wireless
    • Office / Consumer Systems
    • High-End Systems
    • Medical Products
    • Automotive
    • Aerospace/Defense
    • IoT/Wearables
## 2017 Product Emulator Descriptions

<table>
<thead>
<tr>
<th>Emulator</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wireless / Portable</td>
<td>Produced in high volumes, cost is a primary driver, hand held battery powered products are also driven by features, size, weight reduction and battery life</td>
</tr>
<tr>
<td>Office / Consumer Systems</td>
<td>Driven by the need for maximum performance and lowest cost</td>
</tr>
<tr>
<td>Automotive Products</td>
<td>Products that must operate in an automotive environment</td>
</tr>
<tr>
<td>High-End Systems</td>
<td>Products that serve the high end computing, networking, datacom and telecom markets and cover a wide range of cost and performance targets</td>
</tr>
<tr>
<td>Medical Products</td>
<td>Products that must operate with high reliability and, in some cases, support life critical applications</td>
</tr>
<tr>
<td>Aerospace / Defense</td>
<td>Products that must operate reliably in extreme environments</td>
</tr>
<tr>
<td>IoT / Wearables</td>
<td>Presently driven by a wide range of costs and capabilities. By adding internet connectivity and some intelligence to sensors/actuators, a wide range of applications including consumer and industrial product and process monitoring and control are made possible.</td>
</tr>
</tbody>
</table>
## Selected Automotive PEG Key Attributes

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Descriptions</th>
<th>Metric</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
<th>2021</th>
<th>2027</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reliability</td>
<td>Typical Product Family</td>
<td>Deg C - Deg C</td>
<td>-40 to 115</td>
<td>-40 to 115</td>
<td>-40 to 125</td>
<td>-40 to 125</td>
<td>-40 to 125</td>
</tr>
<tr>
<td>Temperature Range</td>
<td>State of the Art (production volume)</td>
<td>-40 to 115</td>
<td>-40 to 115</td>
<td>-40 to 125</td>
<td>-40 to 125</td>
<td>-40 to 125</td>
<td></td>
</tr>
<tr>
<td>Number of Cycles</td>
<td>State of the Art (production volume)</td>
<td>Cycles to Pass</td>
<td>1000</td>
<td>1200</td>
<td>1300</td>
<td>1500</td>
<td>2000</td>
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<tr>
<td>Vibrational Environment (PWB level)</td>
<td>State of the Art (production volume)</td>
<td>G²/Hz</td>
<td>2.1</td>
<td>4.06</td>
<td>4.06</td>
<td>4.06</td>
<td>4.06</td>
</tr>
<tr>
<td>Humidity Range</td>
<td>State of the Art (production volume)</td>
<td>% - %</td>
<td>95-100</td>
<td>95-100</td>
<td>95-100</td>
<td>95-100</td>
<td>90-98</td>
</tr>
<tr>
<td>Altitude</td>
<td>State of the Art (production volume)</td>
<td>Kilometers</td>
<td>4.54</td>
<td>4.54</td>
<td>4.54</td>
<td>4.54</td>
<td>4.54</td>
</tr>
<tr>
<td>Force</td>
<td>Rotational Force on MR</td>
<td>Gs</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
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</table>

### Devices

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Descriptions</th>
<th>Metric</th>
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<th>2017</th>
<th>2019</th>
<th>2021</th>
<th>2027</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of stacked die (Max)</td>
<td>State of the Art (production volume)</td>
<td>#</td>
<td>None</td>
<td>None</td>
<td>2</td>
<td>2</td>
<td>3</td>
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<tr>
<td>Sensors</td>
<td>State of the Art (production volume)</td>
<td>Types</td>
<td>Wheel Speed</td>
<td>Wheel Speed</td>
<td>Wheel Speed</td>
<td>Wheel Speed</td>
<td></td>
</tr>
<tr>
<td>Number of Die in SiP (max)</td>
<td>State of the Art (production volume)</td>
<td>#</td>
<td>None</td>
<td>None</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
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<tr>
<td>Maximum MEMS Power Consumption</td>
<td>State of the Art (production volume)</td>
<td>W</td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEMS</td>
<td>State of the Art (production volume)</td>
<td>Types</td>
<td>Accelerometers</td>
<td>Accelerometers</td>
<td>Accelerometers</td>
<td>Accelerometers</td>
<td></td>
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<tr>
<td>MEMS Reliability</td>
<td>State of the Art (production volume)</td>
<td>MTBF</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
</tr>
<tr>
<td>Embedded Actives</td>
<td>State of the Art (production volume)</td>
<td># per sq. cm</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
</tr>
<tr>
<td>Transformers</td>
<td>State of the Art (production volume)</td>
<td>Types</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
<td>UA</td>
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### Passive Components

<table>
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<th>Parameter</th>
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</tr>
</thead>
</table>
2017 Technology Working Groups (TWGs)

- Modeling, Simulation, and Design
- Electronic Connectors
- RF Components & Subsystems
- Passive Components
- Optoelectronics
- Power Conversion Electronics
- Mass Storage (Magnetic & Optical)
- Energy Storage
- Ceramic Substrates
- Organic PCB
- Board Assembly
- Final Assembly
- Test, Inspection & Measurement
- Thermal Management
- Sustainable Electronics
- Red=Business
- Green=Engineering
- Purple=Manufacturing
- Blue=Component & Subsystem
2017 Roadmap Schedule - Remaining

- June 9, 2016 European Roadmap Workshop/Webinar – 9:00 AM EDT
- June 22, 2016 – Asian Roadmap Workshop/Webinar – 8:00 PM EDT
- July 15, 2016 – TWG Drafts Due for TC Review
- August 24-25, 2016 – TC Face-to-Face Review with TWG Chairs, Nokia
- September 23, 2016 Final Chapters of Roadmap Due
- September 27, 2016 Industry Briefing/SMTAI at Rosemont, IL
- October 30, 2016 – Edit, Prepare Appendix A-D, Executive Summary
- November 18, 2016 – Go To “Press”
- December 16, 2016 – Ship to Members
- April TBD, 2017 – Global industry roadmap presentations via webinars
2015 Roadmap

- > 500 participants
- > 280 companies/organizations
- 20 countries from 4 continents
- 19 Technology Working Groups (TWGs)
- 5 Product Emulator Groups (PEGs)
- ≈ 2000 pages of information
- Roadmaps the needs for 2015-2025
2017 Roadmap
Packaging & Component Substrates TWG Highlights

Bill Bottoms, 3MTS
Raja Swaminathan, Intel
William Chen, ASE
Chairs
Markets Are The Drivers

The drivers for the next decade will be:

– The end of Moore’s Law scaling (an economic issue)
– Rise of the Internet of Things
– Migration of data, logic and applications to the Cloud
– The consumerization of data and data access

Technology will be the enabler

The question is which technologies
Data, logic and applications migration to the Cloud poses difficult challenges

- Power requirements
- Latency
- Physical density of bandwidth
The rise of the internet of things also poses difficult challenges

- Billions or trillions of devices; but will any be high volume?
- New security risks
- A range from low cost, high latency to high cost low latency
- Environments from deserts and glaciers to in-body and under the hood
Consumerization of data and data access poses difficult challenges

- Big data
- High performance
- Battery life
- Latency
- Reliability
- The ultimate internet hub (it is coming in Autos)

**Smart Phone Shipment History**

- Shipments in Millions
- 2009
- 2010
- 2011
- 2013
- 2014
- 2015

- **70 exabytes of memory shipped in smart phones for 2015 alone**
IT includes all systems and components for:

- physical devices to create, store, secure and exchange all forms of data
- Networking for all forms of data movement and sharing
- Physical devices and software to transform data into information and make it available worldwide in real time.
These 4 driving forces present requirements we cannot satisfy through scaling CMOS.

Lower Power, Lower latency, Lower Cost with Higher Performance.

We must bring all electronics closer together and interconnect with photonics.

This can only be accomplished by packaging with Heterogeneous Integration and 3D-Complex SiP.
Prismark TSV Wafer Forecast

TSV WAFER FORECAST

Thermal, Cross talk, bandwidth density, test and cost issues must be solved for this forecast to come true.
Slow growth is projected for SiP by Prismark in these segments.
Executive Summary

Introduction

Situation Analysis - *benchmark state of the art*

Background

Packaging Markets
- Consumer
- Automotive
- Data Center
- Wireless
- Medical
- Aerospace and Defense
- IoT

Difficult Challenges
Single and Multi-chip packaging
  – Electrical Requirements
  – Thermal Requirements
  – Mechanical Requirements
  – Cost
  – Interconnect Technologies for Single Chip Packaging

Fan-in and Fan-out Wafer Level Packaging
  – Embedded WLP
  – Difficult Challenges for WLP

2.5D Integration
3D Integration
- Difficult Challenges for 3D Integration
- Processes for 3D-TSV integration
- Wafer/Device Stacking
- Power Integrity
- Thermal Management
- Test for 3D Integration

System Level Integration In Package (SiP)
- Definition of SiP
- Difficult Challenges for SiP
- Package-on-package
- Complex 3D SiP
- SiP Level system design vs. Board level system design
- Thermal Management for SiP
- Power delivery/Power integrity
- Testing of SiP
Heterogeneous Integration

The need for coherent Chip-Package-System Co-Design, Modeling and simulation

Packaging for Specialized Functions

– Optoelectronic Packaging
– Packaging for MEMS
– Packaging for Automotive Applications
Packaging and Component Substrate Chapter
Outline (5)

Packaging Materials Requirements
– Dielectric materials
– Conductors
– Composite materials

Manufacturing Equipment and Processes

Package Substrates

Reliability

Packaging Gaps and Technology Needs
Difficult Challenges by Package Type

• SiP
  – Physical density
    • Thermal management
    • Cross talk
    • Noise isolation
  – Power delivery
  – Heterogeneous integration (compound semiconductors, photonics to the package, MEMS, etc.)

• Wafer level packaging
  – 3D
  – Heterogeneous integration
  – Embedded components
  – Alignment accuracy

• Large area packages and interposers
  – Stress due to CTE mismatch
  – Warpage

• 3D Integration
  – Cost
  – Power integrity (lower operating voltage)
  – Thermal management
  – Thin wafer and die handling
  – Bandwidth
    • Increase total requirement
    • Increasing physical density requirement
Difficult Challenges: Materials and Equipment

• Materials
  – Incorporation of ballistic conductors
  – Improved thermal conductivity (die attach, underfill, encapsulant, interlayer dielectric, other)
  – Pb free solder materials
  – Low temp bonding (adhesives and other materials)
  – Low cost, high density component substrates with low CTE
  – Flexible component substrates compatible with wearable electronics

• Equipment and Process
  – Placement accuracy (sub-micron)
  – Processes with maximum temperature below 250°C
  – Low cost Handling of thinned die and wafers
New Materials Will Be Required

Many are in use today

- Cu interconnect
- Ultra Low k dielectrics
- High k dielectrics
- Organic semiconductors
- Green Materials
  - Pb free
  - Halogen free

100% of the packaging materials changed during the last decade

But improvements are needed

Many are in development

- Nanotubes
- Nano Wires
- Macromolecules
- Nano Particles
- Composite materials

50% will change again during this decade
Carbon Conductors Look Better Than Cu

Many questions still to be answered before graphene or CNT can be considered as practical interconnect materials. The results so far are very promising.

<table>
<thead>
<tr>
<th></th>
<th>Cu</th>
<th>CNT</th>
<th>GNR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max current density (A/cm²)</td>
<td>~10⁶</td>
<td>&gt; 1x10⁸</td>
<td>&gt; 1x10⁸</td>
</tr>
<tr>
<td>Melting Point (K)</td>
<td>1356</td>
<td>3800 (graphite)</td>
<td>3800 (graphite)</td>
</tr>
<tr>
<td>Tensile Strength (GPa)</td>
<td>0.22</td>
<td>22.2</td>
<td>23.5</td>
</tr>
<tr>
<td>Thermal Conductivity (×10³ W/m-K)</td>
<td>0.385</td>
<td>1.75</td>
<td>3 - 5</td>
</tr>
<tr>
<td>Temp. Coefficient of Resistance (10⁻³ /K)</td>
<td>4</td>
<td>&lt; 1.1</td>
<td>-1.47</td>
</tr>
<tr>
<td>Mean Free Path @ room-T (nm)</td>
<td>40</td>
<td>&gt; 1000</td>
<td>~ 1000</td>
</tr>
</tbody>
</table>
Thermal Management Materials Requirements

*Examples*
Thermal Interface Mat.
Mold Compound
Conductors
Adhesives
Underfill

This will not be easy! It has been called the Hexagon Of Death

- Highly coupled Material Properties
- Novel materials to achieve optimal performance for each parameter
## Package Warpage at Process Temperature

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
<th>2021</th>
<th>2023</th>
<th>2025</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pitch (mm)</strong></td>
<td>Ball Dia. (mm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.60</td>
<td>-0.13, +0.21</td>
<td>-0.13, +0.21</td>
<td>-0.11, +0.18</td>
<td>-0.11, +0.18</td>
<td>-0.11, +0.18</td>
<td>-0.10, +0.16</td>
</tr>
<tr>
<td>0.40</td>
<td>-0.13, +0.20</td>
<td>-0.13, +0.20</td>
<td>-0.11, +0.18</td>
<td>-0.11, +0.18</td>
<td>-0.11, +0.18</td>
<td>-0.10, +0.15</td>
</tr>
<tr>
<td>0.50</td>
<td>-0.13, +0.21</td>
<td>-0.13, +0.21</td>
<td>-0.11, +0.18</td>
<td>-0.11, +0.18</td>
<td>-0.11, +0.18</td>
<td>-0.10, +0.16</td>
</tr>
<tr>
<td>0.30</td>
<td>-0.10, +0.10</td>
<td>-0.10, +0.10</td>
<td>-0.09, +0.09</td>
<td>-0.09, +0.09</td>
<td>-0.09, +0.09</td>
<td>-0.08, +0.08</td>
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<tr>
<td>0.45</td>
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<td>-0.10, +0.10</td>
<td>-0.09, +0.09</td>
<td>-0.09, +0.09</td>
<td>-0.09, +0.09</td>
<td>-0.08, +0.08</td>
</tr>
<tr>
<td>0.30</td>
<td>-0.09, +0.09</td>
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<td>-0.08, +0.08</td>
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<td>-0.07, +0.07</td>
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<tr>
<td>0.5</td>
<td>-0.09, +0.09</td>
<td>-0.09, +0.09</td>
<td>-0.08, +0.08</td>
<td>-0.08, +0.08</td>
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<td>0.25</td>
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<td>-0.07, +0.07</td>
<td>-0.07, +0.07</td>
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<td>-0.07, +0.07</td>
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<td>-0.07, +0.07</td>
<td>-0.065, +0.065</td>
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<td>-0.065, +0.065</td>
<td>-0.065, +0.065</td>
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<td>-0.065, +0.065</td>
<td>-0.065, +0.065</td>
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<td>0.15</td>
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<td>-0.06, +0.06</td>
<td>-0.055, +0.055</td>
<td>-0.055, +0.055</td>
<td>-0.055, +0.055</td>
<td>-0.05, +0.05</td>
</tr>
</tbody>
</table>
# Selected Parameters for Automotive Electronics

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2015</th>
<th>2017</th>
<th>2019</th>
<th>2021</th>
<th>2023</th>
<th>2025</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Battery performance for HEV (Power oriented development)</strong></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Power density per weight (W/kg)</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td>4000</td>
<td></td>
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</tr>
<tr>
<td>2017</td>
<td>4300</td>
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</tr>
<tr>
<td>2019</td>
<td>4450</td>
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<tr>
<td>2021</td>
<td>4550</td>
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<tr>
<td>2023</td>
<td>4650</td>
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<tr>
<td>2025</td>
<td>4750</td>
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<tr>
<td>Energy density per weight (Wh/kg)</td>
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</tr>
<tr>
<td>2015</td>
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<td>2025</td>
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<tr>
<td><strong>Battery performance for BEV (Energy oriented development)</strong></td>
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<tr>
<td>Power density per weight (W/kg)</td>
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<td></td>
</tr>
<tr>
<td>2015</td>
<td>1350</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
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The most common reason for “no known solution” is cost not meeting market need.

Potential Solutions include:
- Increase parallelism in manufacturing
- Reduce the number of process steps
WLP, FOWLP and Panel Processing Increase Parallelism and Reduce Cost

→ Yield, test and productivity of FOWLP lines will rapidly increase

→ Production volume will increase dramatically with time

→ Depreciation of the infrastructure with time

→ New infrastructure will emerge for Panel Processing manufacturing

Cost reduction!

FOWLP – in production

Panel Processing – in development

Source: Yole
Electronic/Photonic Sip Through Heterogeneous Integration

- Antenna
  - Package integration for 2.4G/5G/60GHz
  - Molding
    - MUF
    - Exposed die

- Mechanical Assy
  - Laser welding
  - Flex bending

- Die/Pkg Stacking
  - Die thinning
  - Die interconnect

- SMT
  - Passives
  - Components
  - Connectors

- Shielding
  - Board or package level
  - Compartmental

- Interconnection
  - Flip Chip & Wire Bond

- Photonics Layer
  - PIC Chip - optical bus
  - Embedded Technology
    - Passive component
    - Active device

- Die/Pad Stackings
  - Leadfree / Cu Pillar
  - Bare die package
  - Wafer Bumping/WLP

- Source: ASE with additions
Next Steps: Identify Initiatives to Close Gaps

- Technology Evolution
- Product Needs
- Disruptive Technology
- Government
- Academia
- Industry Solution Needed
- No Work Required or Outsourced
- Global Participation

Available to Market Place

Competitive Solutions

Implementation

Projects

Research

Roadmap

- Technology Evolution
- Product Needs
- Disruptive Technology
- Government
- Academia
- Industry Solution Needed
- No Work Required or Outsourced
- Global Participation

Available to Market Place

Competitive Solutions
iNEMI
Collaborative Project Activities
Why Collaborative Projects?

- **Reduce cost by leveraging resources**
  - Reduce cost by new technologies
  - Reduce resource demands and $ investments for each company
  - Stimulate standards and common specification development
  - Work on issues facing all your suppliers/customers
  - Disseminate efficient business practices

- **Reduce risk of technology introduction**
  - Gain knowledge and accelerate deployment of new technologies
  - Developing industry infrastructure, source of supply
  - Ensure reliability and technology readiness when required

- **Reduce environmental risks**
  - Ensure sustainable solutions are put in place and in sync with industry
Profile of Successful iNEMI Projects

• Addresses knowledge gap of industry
  – Common problem solved by working together
  – Often a pre-cursor to standards development

• Brings together a segment of supply chain to provide industry-wide response

• Direct alignment with member companies’ commercial interests.

LCA Estimator
Tin Whisker Susceptibility
Warpage Characterization of Organic Packages
Creep Corrosion
<table>
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<tr>
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<th>TIG</th>
<th>Chair</th>
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<th>Est End Date</th>
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<td>Characterization of Pb-Free Alloy Alternatives Project - - Addendum to Scope of Work Version 3.2 June 2, 2015</td>
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iNEMI Involvement
Lead & Learn

Tell me and I forget. Teach me and I remember. Involve me and I learn.

- Benjamin Franklin

• iNEMI membership provides the critical mass required to affect significant changes
  – Set direction for future technologies
  – Influence supply base to develop solutions that will support product roadmap needs
  – Drive standardization to reduce cost and complexity through collaboration

• iNEMI consists of industry leaders, scientists and technologists with broad expertise
  – Senior people with 20+ years experience in the industry
Why iNEMI

• Strong Global Membership
  • Depth and Breadth of Supply Chain Leaders
  • Strong set of Universities & Research Institutes

• iNEMI Reputation
  • Track record of sustainability leadership
  • In demand for knowledge/science input
  • Results oriented workshops

• 10 year Technology | Business Roadmap
  • Delivered every two years
  • Unique Gap Analysis
  • Technical/Business Evolution Details

• Proven Collaborative R&D Methodology
  • Time tested over 20 years
  • 20-25 active collaborative R&D projects
iNEMI Member Testimonials

Flextronics depends on roadmaps coming from iNEMI. We need that level of support and visibility from a consortium like iNEMI that has a lot more visibility into the industry. — Murad Kurwa, Flextronics

These are the type of projects that not one company can do or drive it on its own. It really requires a collaborative effort across the entire supply chain. — Mostafa Aghazadeh, Intel

iNEMI is providing me an incredible window into the industry and the opportunity to be connected at a very low cost with everybody in the industry. — Jean-Luc Pelissier, Universal Instruments
Opportunities to Get Engaged

• Engage in roadmap activities

• Purchase the iNEMI Roadmap at:
  
  www.inemi.org

*Become involved in collaborative projects:
  1. Engage in existing projects
  2. Participate in projects being planned and defined
  3. Develop own proposal for project, which can be reviewed with iNEMI membership and technical committee (TC)

*Project involvement requires iNEMI membership
Completing the 2015 iNEMI Roadmap Cycle

- 2015 iNEMI Roadmap Development Cycle is wrapped up!
- 2015 iNEMI Technology Plan Development Closed
- 2015 iNEMI Research Priorities Document Development Closing and Available at www.inemi.org in late June
- 2015 Roadmap Available to Industry Now:
  - Order the 2015 iNEMI Roadmap flash drive at www.inemi.org
  - Individual roadmap chapters are also available as a PDF document at www.inemi.org
- 2017 iNEMI Roadmap moving forward with 7 product sectors and 21 technology chapters
  - Contact Chuck Richardson for more details at crichardson@inemi.org
- Get Involved in iNEMI – An organization with an Eye to the Future and a Means to Get There
Thank You
For Your Time & Attention
www.inemi.org
Bill Bader
bill.bader@inemi.org
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Back-up Collaborative Project Examples
Warpage Characteristics of Organic Packages

Chair:
Wei Keat Loh, Intel
Ron Kulterman, Flextronics
Tim Purdie, Akrometrix
Interested Packaging Technology based on field survey

Generous Donation of Samples from Industry

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Design</th>
<th>Schematic drawing of package construction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overmold TMV®</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Expose Die TMV®</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bare Die POP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interposer POP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pre-stack POP package</td>
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<td></td>
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<tr>
<td>MCEP®</td>
<td></td>
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</tr>
<tr>
<td>POP Memories</td>
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</tr>
<tr>
<td>FCBGA</td>
<td>17x17-35x35mm</td>
<td></td>
</tr>
<tr>
<td>FCBGA with Lid</td>
<td>Organic and ceramic substrate</td>
<td></td>
</tr>
<tr>
<td>PBGA</td>
<td>Ranges</td>
<td></td>
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</table>

Objective:
1) To characterize the package warpage with respect to existing warpage allowable
2) To understand the impact of bake and moisture exposure

* Paper published at ICEP 2015 conference in Japan.
• Benchmark or fingerprint package warpage characteristics to develop a better understanding of the current trends of warpage behavior for different package constructions.
  – Small BGA Packages:
    • Interposer, 2.5D, 3D stack packages, through via silicon (TSV); Memory technology (High Band Width Memory, DDR)
  – Large BGA Packages
    • Package stiffeners – picture frame stiffener, different stiffener attachment method, shapes and sizes
    • Either organic substrate or ceramic substrate
  – System In Package/Multi Chip Package (BGA)
    • Stack Die or multiple die
    • Die on interposer and/or with asymmetrical layout.
  – Embedded Package (embedded silicon, actives and passives)
• The measurement will be done at respective tool manufacturer.
• Identify measurement methods and protocols based on the different measurement techniques and technology such as below:
  – Confocal techniques
  – Projection moiré techniques
  – Thermo moiré techniques with or without convective reflow
  – 3D Digital Image Correlations (DIC)
• Other packaging materials and design evaluation if provided.
QFN Package Board Level Reliability Project

Project Chairs:
Richard Coyle, Alcatel-Lucent
David Ihms, Delphi
Published QFN thermal cycling data are lacking for characterizing longer product lifetimes, in more aggressive use environments, particularly using thicker printed circuit boards typical of higher reliability applications.

**Project Leader(s):**
- Richard Coyle – Nokia
- David Ihms - Delphi

**Project Start:** Aug 5, 2015
**Estimated End:** Feb, 2017

### Purpose and Scope of Project

- Provide QFN BLR data as a function of three printed circuit board thicknesses and two different thermal cycles. This will provide guidance for translating data from one board thickness or one temperature cycle to another.
- Compare the reliability performance of non-wettable and wettable surfaces on the QFN board attachments. Wettable side surfaces are being proposed to generate side fillets for increasing the thermal fatigue resistance.
- Industry standard testing protocols based on IPC-9701 will be used to evaluate the board level reliability.

### Project Tasks

- Material Selection
- Design of Experiment
- Test Board Design
- Board and Device Properties Characterization
- QFN Assembly, Test board fabrication, Stencil fabrication
- SMT
- Test and Data Collection
- Report

### Status Update

- Two QFN suppliers, six unique QFNs; 10x10 and 9x9 designs
- Rigid board designed and under fabrication
- Flex board design delayed
- Stencils provided by LaserJob
- All necessary “in-kind” resources identified
- The iNEMI variant molding compound CTE project is supported by this TIG; test board, assembly, and thermal cycle testing
Team Members

- Alcatel-Lucent
- Delphi
- Intel
- ASE Group
- akrometrix
- IST
- Wistron
- CMK

Stencil Fab:
- LaserJob
## QFN Packages

<table>
<thead>
<tr>
<th>PKG Size (mm)</th>
<th>Wettable (Dimple)</th>
<th>STD1</th>
<th>w/ FLK (step cut)</th>
<th>Wettable1 AOZG V766 (A): Dimple</th>
<th>A02L VFQFPN w/o Wet FLK</th>
<th>A02L VFQFPN w/ Wet FLK</th>
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<tbody>
<tr>
<td></td>
<td>10 x 10</td>
<td>10 x 10</td>
<td>10 x 10</td>
<td>9 x 9</td>
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<td>PKG Height</td>
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<td>Lead Pitch (mm)</td>
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<tr>
<td>Flag Size (mm)</td>
<td>7.7x7.7</td>
<td>7.7x7.7</td>
<td>7.7x7.7</td>
<td>6.9 x 6.9</td>
<td>4.55 x 5.25 (29.2%)</td>
<td>4.55 x 5.25 (29.2%)</td>
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<tr>
<td>(Pad to PKG ratio)</td>
<td>(59.3%)</td>
<td>(59.3%)</td>
<td>(59.3%)</td>
<td>(58.8%)</td>
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<tr>
<td>Die Size (mm)</td>
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<td>MAX 6.5x6.5 (42.3%)</td>
<td>MAX 6.5x6.5 (42.3%)</td>
<td>5.0 x 4.2 (25.9%)</td>
<td>4.0 x 3.0 (14.8%)</td>
<td>5.0 x 4.2 (25.9%)</td>
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<tr>
<td>(DTP ratio)</td>
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<tr>
<td>Leadframe Thick</td>
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<td>Leadframe Material</td>
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<td>C194</td>
<td>CuFe2P etched</td>
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<td>Surface Finish</td>
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<td>Sn</td>
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<td>Singulation Method</td>
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<td>CTE 1</td>
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<td>CET 2</td>
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<tr>
<td>Bonding Wire</td>
<td>Au</td>
<td>Au</td>
<td>Au</td>
<td>Au/Cu</td>
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<tr>
<td>Dia.</td>
<td>0.8mil</td>
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<td>1.0mil</td>
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iNEMI Project
BiSn Based Low Temperature Soldering Process and Reliability

Co-Chairs:
Raiyo Aspandiar, Intel
Scott Mokler, Intel
Project Purpose

- To assess the surface mount processibility and reliability of the solder joints formed when enhanced low temperature Bi-Sn based solder pastes are used for assembling electronic components on printed circuit boards.

Problem Statement for low temperature Bi-Sn Solders

- Bi causes hardening of the solder joints which are prone to brittle fractures under mechanical shock and drop forces.

Two Solution Paths to be Evaluated

- **Resin Reinforcement**: Resin added to the solder paste cures during reflow and provides reinforcement under mechanical stresses.

- **Ductile Bi-Sn Metallurgy**: Addition of Elemental Dopants increases ductility of BiSn solder by modifying microstructure and Intermetallic compound morphology.
Drivers for Low Temperature Soldering

Green House Gas Reduction

SMT Margin for Thin Designs

Lower Electricity Usage Reduces Cost

Reduced PLC Environmental Impact

➢ Low Temp Solders Provide Benefit to Each of These Challenges
Low Temperature Solders

- There are a variety of compositions and melting ranges for Potential Low Temperature Solders in Electronics Manufacturing.

**Standard Alloys**
- 99.3Sn/0.7Cu (+Ni,Ce)
- 96.5Sn/3.0Ag/0.5Cu
- 95.5Sn/4.0Ag/0.5Cu

**SAC alloys**
- 63Sn/37Pb

**Eutectic Tin-Lead Alloy**

**Low Temp Alloys**
- 59Sn/40Bi/Cu/Ni
- 57Bi/42Sn/xAg (x=0 to 1)
- 59Sn/40Bi/Cu/Ni

**Medium Temperature Solders**
- [SnAgCu+Bi,In]
  - melt in the 210 to 220°C range

**Low Temperature Solders**
- [Bi/Sn/X, X=Ag,Cu,Ni]
  - melt in the 139 to 175°C range

- **Bi-Sn system solders are being proposed for this Project**
- **More processing and economic benefits than Medium Temperature Solders**
Project Plan

• Objective:
  – To assess the two solution paths available for mitigating mechanical drop / shock risks associated with Bi-Sn based solder pastes for SMT assembly

• Scope
  – Solder Pastes
    • ductile Bi-Sn metallurgy
    • Resin Reinforced Bi-Sn based
    • SAC305 (for comparison)
    • standard BiSnAg (for comparison)
  – Components
    • High density BGAs
    • BTCs (such as QFNs)
    • Chip components
    • Other Non-IC (Switches, Connectors)
  – Board Surface Finishes
    • OSP
    • ENIG
    • ENEPIG
    • Other
  – SMT Process Development
    • Stencil Printing
    • Reflow Soldering
    • Rework Process
  – Shock/Drop Evaluation using Test Vehicle Designs
    • Per JEDEC or other standards
  – Thermal cycling
    • 2nd phase
  – Product Validation
    • Boards Assembled with Best performing solder pastes from each category
    • Subjected to selected Product level functional and mechanical shock/drop tests
    • 2nd phase