The Increasing Importance & Challenges of Packaging in The 21st Century

Chuck Richardson, iNEMI

International Symposium on 3D Power Electronics Integration and Manufacturing
McKimmon Conference and Training Center at North Carolina State University
June 14, 2016

iNEMI®
Advancing manufacturing technology

Topics

- iNEMI Introduction
- Roadmap Process Overview
- 2017 Packaging & Component Substrates TWG Scope & Highlights
- Packaging Technology Needs & Gaps
- Proven Industry Collaboration Model
- How to Get Involved
- Back-up - Project Examples

About iNEMI

Mission: Forecast and Accelerate improvements in the Electronics Manufacturing Industry for a Sustainable Future.

5 Key Deliverables:

- **Technology Roadmaps**
- **Collaborative Deployment Projects**
- Research Priorities Document
- Proactive Forums
- Position Papers

International Electronics Manufacturing Initiative (iNEMI) is an industry-led consortium of about 90 global manufacturers, suppliers, industry associations, government agencies and universities. A Non Profit Fully Funded by Member Dues; In Operation Since 1994.

Visit us at www.inemi.org

OEMODM/EMS Members

Supplier Members

5

Supplier Members (cont.)

DYCONEX
an MST company

unow®
材料连接未来
優諾

ITEQ
INNOVATION • TEAMWORK • EXCELLENCE • QUALITY

EMC
ELITE MATERIAL CO., LTD.

INSIDIX

i3 electronics

IMI

INTERFLUX®
ELECTRONICS

Hitachi Chemical
Working On Wonders

IBIDEN

isola
The Base for Innovation

Supplier Members (cont.)

MYCRONIC

Moldex3D
MOLDING INNOVATION

LOTES

Supplier Members (cont.)

TAKAOKA TOKO CO., LTD.

OAK-MITSUI
MITSUI KINZOKU CORPORATE GROUP

Rosenberger

JCET

STATSChipPAC®
A JCET Company

SMIC
Senju Comtek Corp.

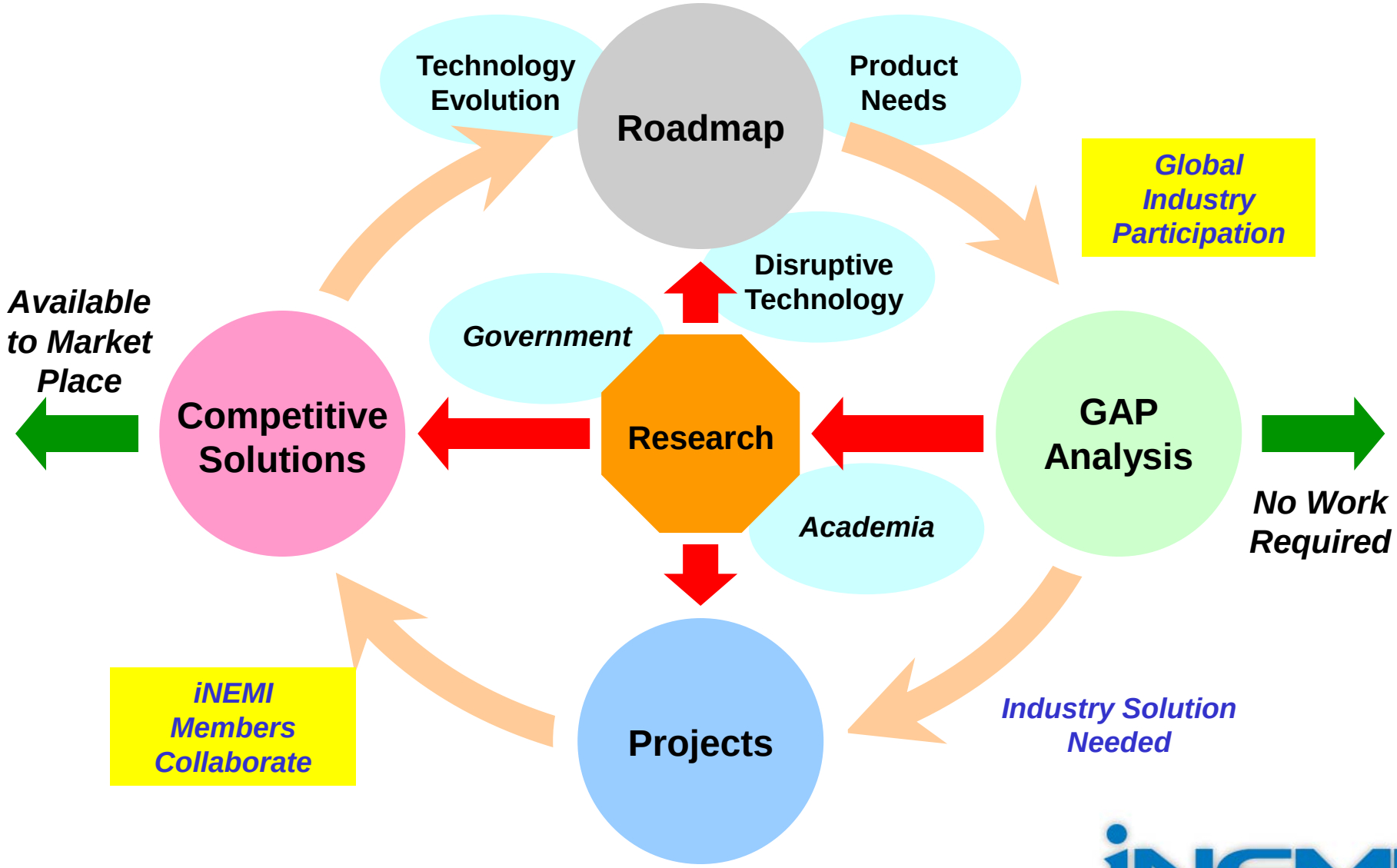
iNEMI

Association/Consortium, Government, Consultant & University Members

Association/Consortium, Government, Consultant & University Members, (con't.)

2017 Roadmap Process & Scope

Methodology



Industry Led Teams

- **Technical Working Group Teams**
  - **Develops the roadmap technology chapters**
  - **Presently 21 Teams and Chapters**

- **Product Emulator Group Teams**
  - **“Virtual Product”: future product attributes plus key cost and density drivers – Presently 7 Teams and Chapters**
    - **Portable / Wireless**
    - **Office / Consumer Systems**
    - **High-End Systems**
    - **Medical Products**
    - **Automotive**
    - **Aerospace/Defense**
    - **IoT/Wearables**

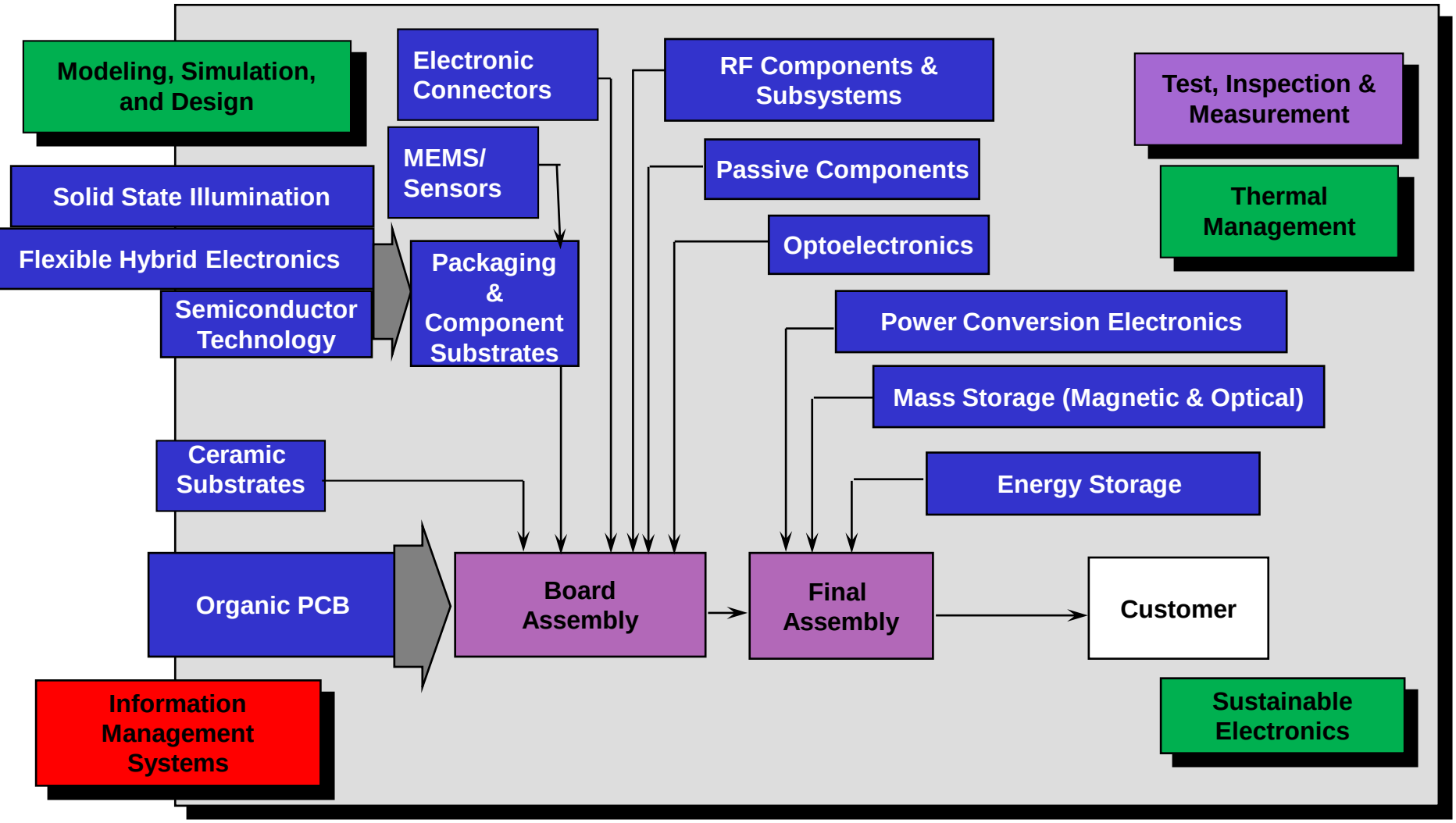
2017 Product Emulator Descriptions

Emulator	Characteristics
Wireless / Portable	Produced in high volumes, cost is a primary driver, hand held battery powered products are also driven by features, size, weight reduction and battery life
Office / Consumer Systems	Driven by the need for maximum performance and lowest cost
Automotive Products	Products that must operate in an automotive environment
High-End Systems	Products that serve the high end computing, networking, datacom and telecom markets and cover a wide range of cost and performance targets
Medical Products	Products that must operate with high reliability and, in some cases, support life critical applications
Aerospace / Defense	Products that must operate reliably in extreme environments
IoT / Wearables	Presently driven by a wide range of costs and capabilities. By adding internet connectivity and some intelligence to sensors/actuators, a wide range of applications including consumer and industrial product and process monitoring and control are made possible.

Selected Automotive PEG Key Attributes

Parameter	Descriptions	Metric	2015	2017	2019	2021	2027
Reliability	**Typical Product Family**						
Temperature Range	State of the Art (production volume)	Deg C - Deg C	-40 to 115	-40 to 115	-40 to 125	-40 to 125	-40 to125
Number of Cycles	State of the Art (production volume)	Cycles to Pass	1000	1200	1300	1500	2000
Vibrational Environment (PWB level)	State of the Art (production volume)	G^2/Hz	2.1	4.06	4.06	4.06	4.06
Use Shock Environment	1 meter drop on concrete	Gs & ms to Pass	25G, 15ms	25G, 15ms	25G, 15ms	25G, 15ms	25G, 15ms
Humidity Range	State of the Art (production volume)	% - %	95-100	95-100	95-100	95-100	90-98
Altitude	State of the Art (production volume)	Kilometers	4.54	4.54	4.54	4.54	4.54
Force	Rotational Force on MR	Gs	UA	UA	UA	UA	UA
Devices	**Max Used in Volume Production**						
Number of stacked die (Max)	State of the Art (production volume)	#	None	None	2	2	3
Sensors	State of the Art (production volume)	Types	Wheel Speed Steering Position Gas Pedal Position Throttle Position	Wheel Speed Steering Position Gas Pedal Position Throttle Position	Wheel Speed Steering Position Gas Pedal Position Throttle Position	Wheel Speed Steering Position Gas Pedal Position Throttle Position	Wheel Speed Steering Position Gas Pedal Position Throttle Position
Number of Die in SiP (max)	State of the Art (production volume)	#	None	None	UA	UA	UA
Maximum MEMS Power Consumption	State of the Art (production volume)	W					
MEMS	State of the Art (production volume)	Types	Accelerometers Gyroscopes Pressure Air Flow	Accelerometers Gyroscopes Pressure Air Flow	Accelerometers Gyroscopes Pressure Air Flow	Accelerometers Gyroscopes Pressure Air Flow	Accelerometers Gyroscopes Pressure Air Flow
MEMS Reliability	State of the Art (production volume)	MTBF	UA	UA	UA	UA	UA
Embedded Actives	State of the Art (production volume)	# per sq. cm	UA	UA	UA	UA	UA
Transformers	State of the Art (production volume)	Types	UA	UA	UA	UA	UA
Passive Components	**Typical Product Family**						

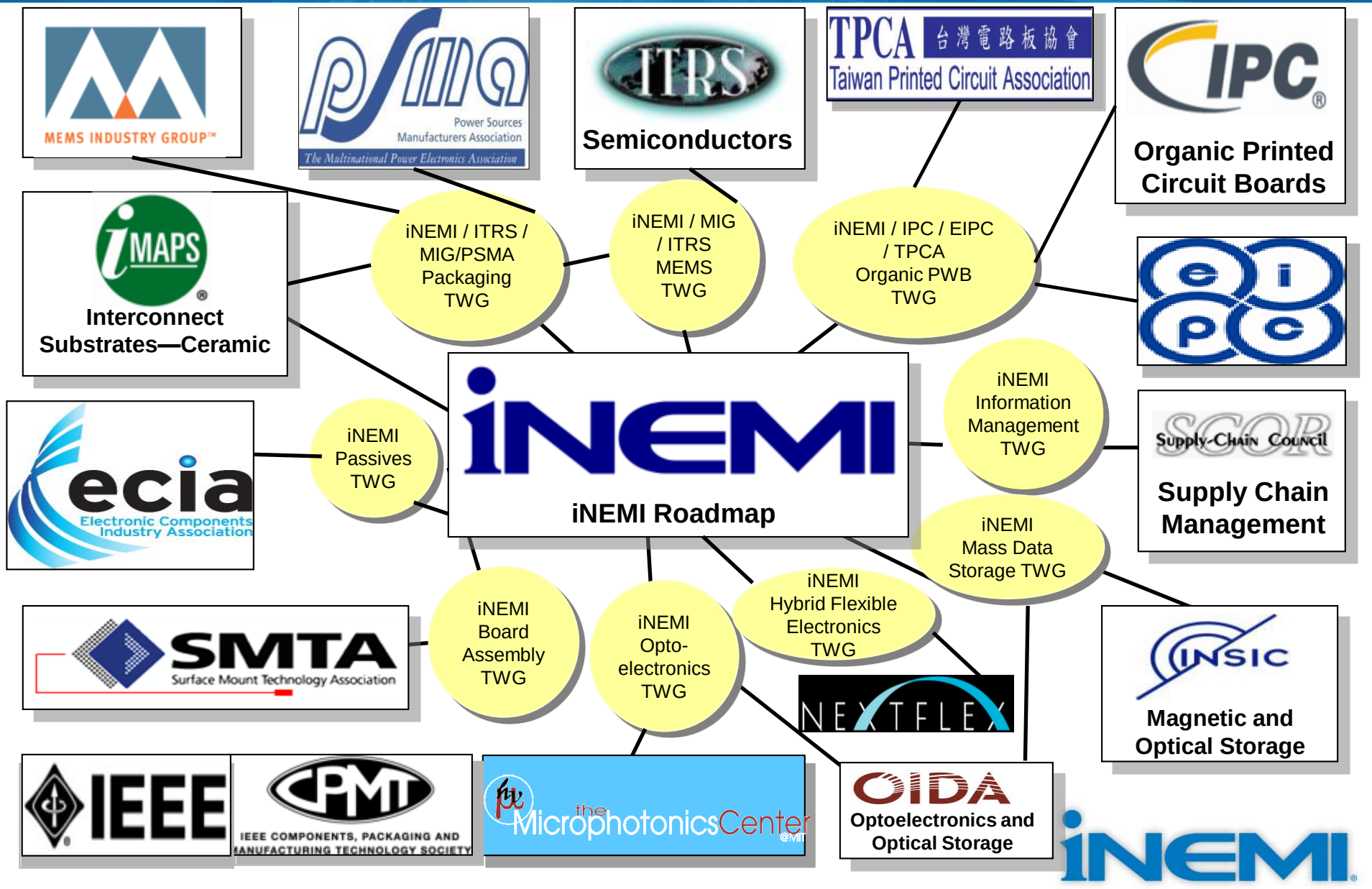
2017 Technology Working Groups (TWGs)



Red=Business Green=Engineering Purple=Manufacturing Blue=Component & Subsystem

iNEMI

Fifteen Contributing Organizations

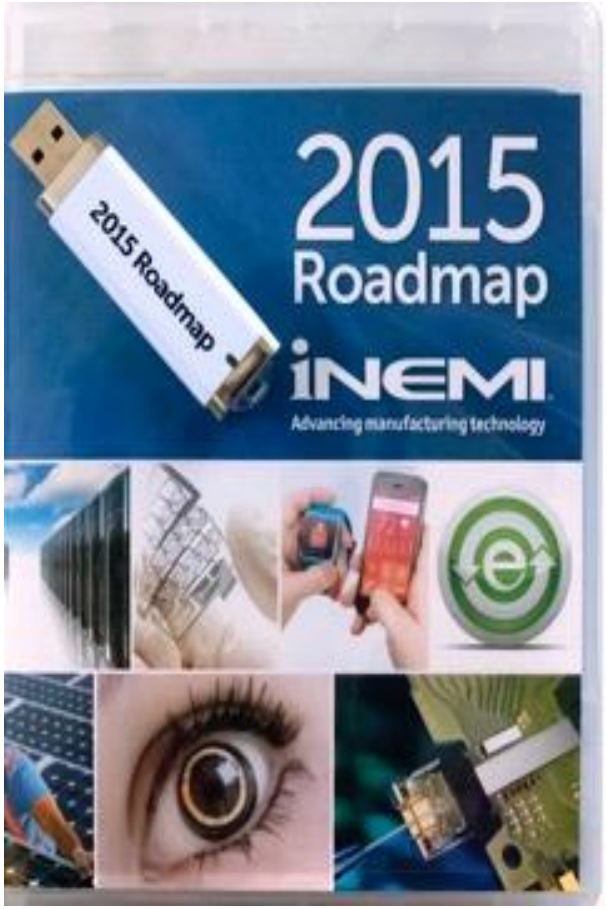


2017 Roadmap Schedule - Remaining

- May 31, 2016 – N.A. RM WS - Open Roadmap TWG Presentations in Las Vegas, NV (ECTC)
- June 9, 2016 European Roadmap Workshop/Webinar – 9:00 AM EDT
- **June 13-15, 2016 – PEIM Conference Roadmap Presentation, N.C. State U.**
- **June 22, 2016 – Asian Roadmap Workshop/Webinar – 8:00 PM EDT**
- **July 15, 2016 – TWG Drafts Due for TC Review**
- **August 24-25, 2016 – TC Face-to-Face Review with TWG Chairs, Nokia**
- **September 23, 2016 Final Chapters of Roadmap Due**
- **September 27, 2016 Industry Briefing/SMTAI at Rosemont, IL**
- **October 30, 2016 – Edit, Prepare Appendix A-D, Executive Summary**
- **November 18, 2016 – Go To "Press"**
- **December 16, 2016 – Ship to Members**
- **April TBD, 2017 – Global industry roadmap presentations via webinars**

2015 Roadmap

- > 500 participants
- > 280 companies/organizations
- 20 countries from 4 continents
- 19 Technology Working Groups (TWGs)
-
- 5 Product Emulator Groups (PEGs)
- ≈ 2000 pages of information
- Roadmaps the needs for 2015-2025



2017 Roadmap Packaging & Component Substrates TWG Highlights

Bill Bottoms, 3MTS
Raja Swaminathan, Intel
William Chen, ASE
Chairs

iNEMI®
Advancing manufacturing technology

Markets Are The Drivers

The drivers for the next decade will be:

- **The end of Moore's Law scaling (an economic issue)**
- **Rise of the Internet of Things**
- **Migration of data, logic and applications to the Cloud**
- **The consumerization of data and data access**

Technology will be the enabler

The question is which technologies

Migration To The Cloud

Data, logic and applications migration to the Cloud poses difficult challenges

- **Power requirements**
- **Latency**
- **Physical density of bandwidth**

The Internet Of Everything

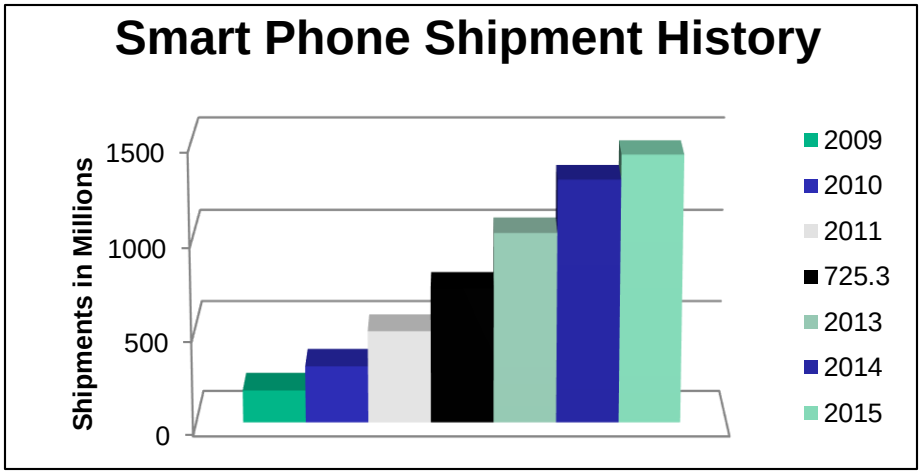
The rise of the internet of things also poses difficult challenges

- **Billions or trillions of devices; but will any be high volume?**
- **New security risks**
- **A range from low cost, high latency to high cost low latency**
- **Environments from deserts and glaciers to in-body and under the hood**

Consumerization Of Data

Consumerization of data and data access poses difficult challenges

- **Big data**
- **High performance**
- **Battery life**
- **Latency**
- **Reliability**
- **The ultimate internet hub (it is coming in Autos)**



70 exabytes of memory shipped in smart phones for 2015 alone

The Enabling Technology Will Be Information Technology

IT includes all systems and components for:

- **physical devices to create, store, secure and exchange all forms of data**
- **Networking for all forms of data movement and sharing**
- **Physical devices and software to transform data into information and make it available worldwide in real time.**

Everything Must Change Including Roadmaps

These 4 driving forces present requirements we cannot satisfy through scaling CMOS

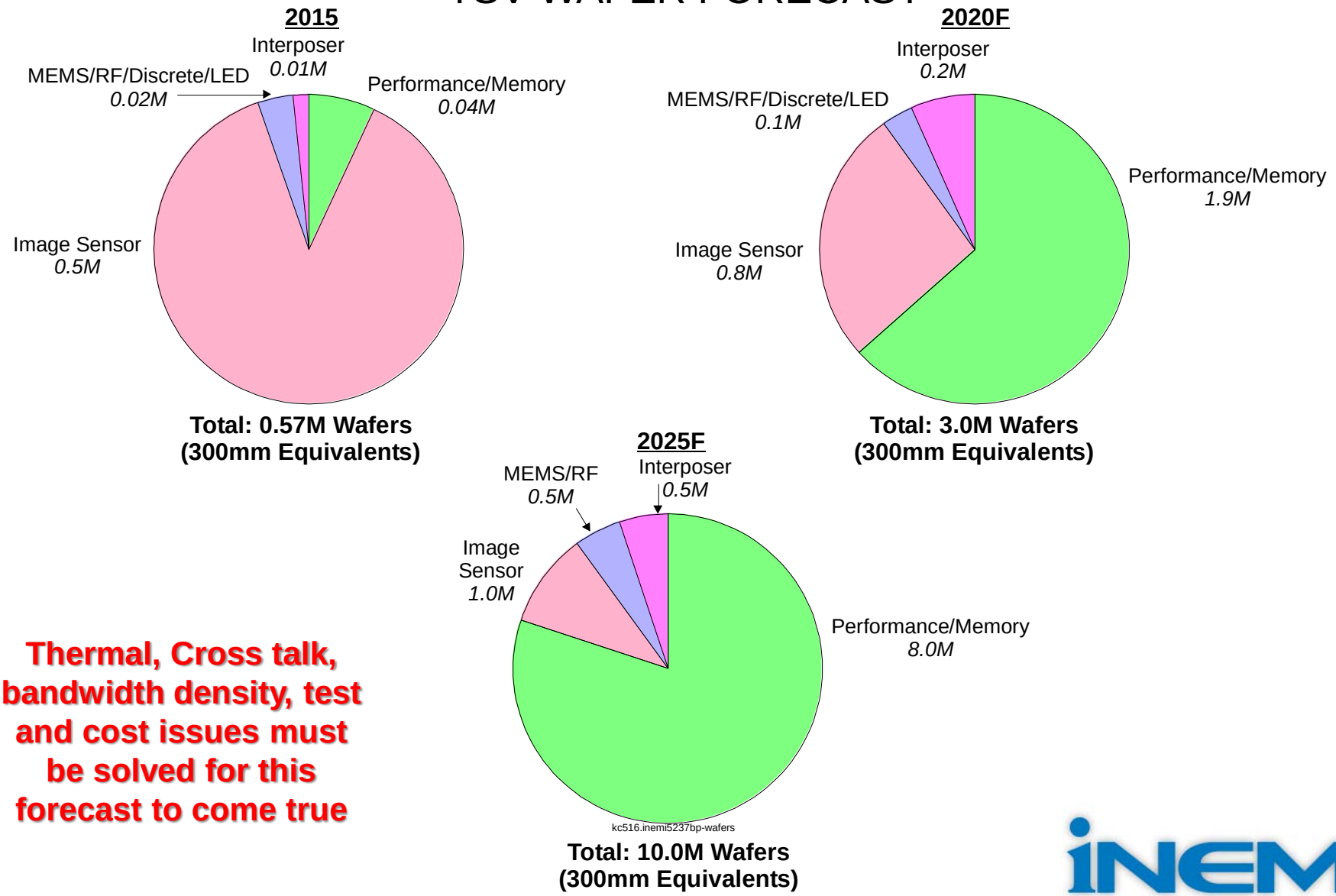
Lower Power, Lower latency, Lower Cost with Higher Performance

We must bring all electronics closer together and interconnect with photonics

This can only be accomplished by packaging with Heterogeneous Integration and 3D-Complex SiP

Prismark TSV Wafer Forecast

TSV WAFER FORECAST



Thermal, Cross talk, bandwidth density, test and cost issues must be solved for this forecast to come true

Prismark SiP/Module Forecast

Product/Package Type Volume (Bn Units)	2015	2020F	2025F	Leading Suppliers/Players
Stacked Memory SiP	8.7	11.0	12.0	Samsung, Micron, SKHynix, Toshiba, SanDisk, PTI, ASE, SPIL, Amkor, JCET/STATS
Stacked Package on Package: Bottom Package Only	1.0	1.2	1.5	Samsung, Apple, Qualcomm, MediaTek, HiSilicon, Amkor, JCET/STATS, ASE, SPIL
PA Centric RF SiP	4.5	5.0	6.0	Qorvo, Skyworks, Anadigics, Avago, Amkor, ASE, Inari, HEG, JCET, Unisem, ShunSin
Connectivity SiP (Bluetooth/WLAN)	0.8	1.2	1.8	Murata, Taiyo Yuden, Samsung, ACSIP, ALPS, USI
Graphics/CPU or ASIC MCP	0.2	0.2	0.2	Intel, AMD, NVIDIA, Xilinx, Broadcom
Power SiP	3.5	4.5	5.5	NXP, STMicro, TI, Freescale, Toshiba, Infineon, Renesas, ON Semi
MEMS and Controller SiP	9.1	12.2	15.0	STMicro, Analog, Bosch, Freescale, Knowles, InvenSense, Denso
Camera Module	3.9	5.5	6.5	LG Innotek, SEMCO, Hon Hai, Lite-on, Toshiba, Sunny Optical, Sharp, Cowell
Fingerprint Sensor Module	0.45	1.5	2.5	Apple, Synaptics, Fingerprint Cards, Silead, Goodix, NEXT Biometrics, Qualcomm
Display Touch Module	0.06	1.5	2.0	Synaptics, ASE
Total	**32.21**	**43.80**	**53.0**	

Slow growth is projected for SiP by Prismark in these segments

iNEMI

2017 iNEMI Packaging and Component Substrate Chapter Outline

Executive Summary

Introduction

Situation Analysis - *bench mark state of the art*

Background

Packaging Markets

- Consumer
- Automotive
- Data Center
- Wireless
- Medical
- Aerospace and Defense
- IoT

Difficult Challenges

Packaging and Component Substrate Chapter Outline (2)

Single and Multi-chip packaging

- Electrical Requirements
- Thermal Requirements
- Mechanical Requirements
- Cost
- Interconnect Technologies for Single Chip Packaging

Fan-in and Fan-out Wafer Level Packaging

- Embedded WLP
- Difficult Challenges for WLP

2.5D Integration

Packaging and Component Substrate Chapter Outline (3)

3D Integration

- Difficult Challenges for 3D Integration
- Processes for 3D-TSV integration
- Wafer/Device Stacking
- Power Integrity
- Thermal Management
- Test for 3D Integration

System Level Integration In Package (SiP)

- Definition of SiP
- Difficult Challenges for SiP
- Package-on-package
- Complex 3D SiP
- SiP Level system design vs. Board level system design
- Thermal Management for SiP
- Power delivery/Power integrity
- Testing of SiP

Packaging and Component Substrate Chapter Outline (4)

Heterogeneous Integration

The need for coherent Chip-Package-System Co-Design, Modeling and simulation

Packaging for Specialized Functions

- Optoelectronic Packaging
- Packaging for MEMS
- Packaging for Automotive Applications

Packaging and Component Substrate Chapter Outline (5)

Packaging Materials Requirements

- Dielectric materials
- Conductors
- Composite materials

Manufacturing Equipment and Processes

Package Substrates

Reliability

Packaging Gaps and Technology Needs

Difficult Challenges by Package Type

- SiP
  - Physical density
    - Thermal management
    - Cross talk
    - Noise isolation
  - Power delivery
  - Heterogeneous integration (compound semiconductors, photonics to the package, MEMS, etc.)
- Wafer level packaging
  - 3D
  - Heterogeneous integration
  - Embedded components
  - Alignment accuracy
- Large area packages and interposers
  - Stress due to CTE mismatch
  - Warpage
- 3D Integration
  - Cost
  - Power integrity (lower operating voltage)
  - Thermal management
  - Thin wafer and die handling
  - Bandwidth
    - Increase total requirement
    - Increasing physical density requirement

Difficult Challenges: Materials and Equipment

- **Materials**
  - Incorporation of ballistic conductors
  - Improved thermal conductivity (die attach, underfill, encapsulant, interlayer dielectric, other)
  - Pb free solder materials
  - Low temp bonding (adhesives and other materials)
  - Low cost, high density component substrates with low CTE
  - Flexible component substrates compatible with wearable electronics
- **Equipment and Process**
  - Placement accuracy (sub-micron)
  - Processes with maximum temperature below 250° C
  - Low cost Handling of thinned die and wafers

New Materials Will Be Required

Many are in use today

- Cu interconnect
- Ultra Low k dielectrics
- High k dielectrics
- Organic semiconductors
- Green Materials
  - Pb free
  - Halogen free

100% of the packaging materials changed during the last decade

But improvements are needed

Many are in development

- **Nanotubes**
- **Nano Wires**
- **Macromolecules**
- **Nano Particles**
- **Composite materials**

50% will change again during this decade

iNEMI

Carbon Conductors Look Better Than Cu

Many questions still to be answered before graphene or CNT can be considered as practical interconnect materials. The results so far are very promising.

	Cu	CNT	GNR	
Max current density (A/cm^2)	**~10^6**	**> 1x10^8**	**> 1x10^8**	**x10^2**
Melting Point (K)	**1356**	**3800** (graphite)	**3800** (graphite)	
Tensile Strength (GPa)	**0.22**	**22.2**	**23.5**	**x10^2**
Thermal Conductivity (×10^3 W/m-K)	**0.385**	**1.75** *Hone, et al. Phys. Rev. B 1999*	**3 - 5** *Balandin, et al. Nano Let., 2008*	**x10**
Temp. Coefficient of Resistance (10^{-3} /K)	**4**	**< 1.1** *Kane, et al. Europhys. Lett.,1998*	**-1.47** *Shao et al. Appl Phys. Lett., 2008*	
Mean Free Path @ room-T (nm)	**40**	**> 1000** *McEuen, et al. Trans. Nano., 2002*	**~ 1000** *Bolotin, et al. Phys. Rev. Let. 2008*	**x25**

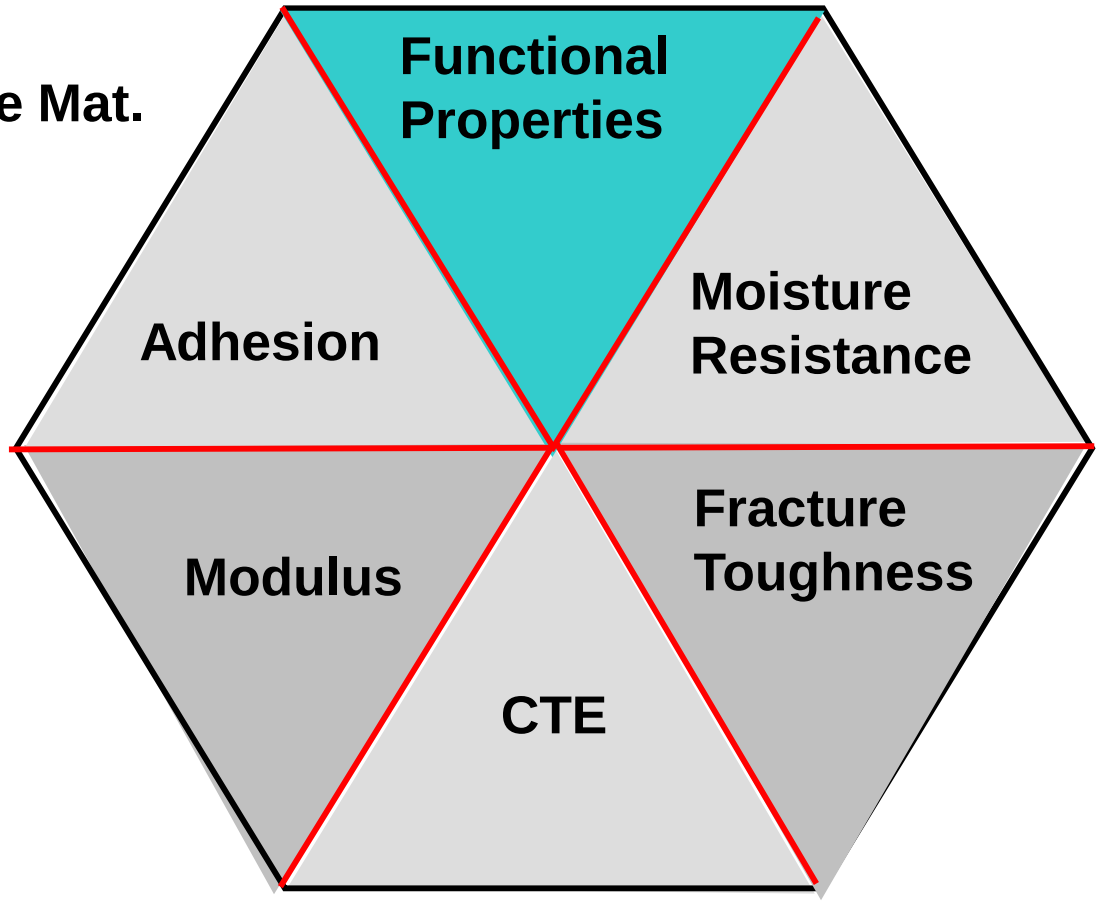
iNEMI

Thermal Management Materials Requirements

Examples

Thermal Interface Mat.
Mold Compound
Conductors
Adhesives
Underfill

This will not be easy! It has been called the Hexagon Of Death



- **Highly coupled Material Properties**
- **Novel materials to achieve optimal performance for each parameter**

Package Warpage at Process Temperature

Year of Production		*2015*	*2017*	*2019*	*2021*	*2023*	*2025*
Pitch (mm)	Ball Dia. (mm)						
1.0	0.60	**-0.13, +0.21**	**-0.13, +0.21**	**-0.11, +0.18**	**-0.11, +0.18**	**-0.11, +0.18**	**-0.10, +0.16**
	0.40	**-0.13, +0.20**	**-0.13, +0.20**	**-0.11, +0.18**	**-0.11, +0.18**	**-0.11, +0.18**	**-0.10, +0.15**
0.8	0.50	**-0.13, +0.21**	**-0.13, +0.21**	**-0.11, +0.18**	**-0.11, +0.18**	**-0.11, +0.18**	**-0.10, +0.16**
	0.30	**-0.10, +0.10**	**-0.10, +0.10**	**-0.09, +0.09**	**-0.09, +0.09**	**-0.09, +0.09**	**-0.08, +0.08**
0.65	0.40	**-0.10, +0.10**	**-0.10, +0.10**	**-0.09, +0.09**	**-0.09, +0.09**	**-0.09, +0.09**	**-0.08, +0.08**
	0.30	**-0.09, +0.09**	**-0.09, +0.09**	**-0.08, +0.08**	**-0.08, +0.08**	**-0.08, +0.08**	**-0.07, +0.07**
0.5	0.30	**-0.09, +0.09**	**-0.09, +0.09**	**-0.08, +0.08**	**-0.08, +0.08**	**-0.08, +0.08**	**-0.07, +0.07**
	0.25	**-0.08, +0.08**	**-0.08, +0.08**	**-0.07, +0.07**	**-0.07, +0.07**	**-0.07, +0.07**	**-0.065, +0.065**
0.4	0.25	**-0.08, +0.08**	**-0.08, +0.08**	**-0.07, +0.07**	**-0.07, +0.07**	**-0.07, +0.07**	**-0.065, +0.065**
	0.20	**-0.07, +0.07**	**-0.07, +0.07**	**-0.065, +0.065**	**-0.065, +0.065**	**-0.065, +0.065**	**-0.06, +0.06**
0.3	0.20	**-0.07, +0.07**	**-0.07, +0.07**	**-0.065, +0.065**	**-0.065, +0.065**	**-0.065, +0.065**	**-0.06, +0.06**
	0.15	**-0.06, +0.06**	**-0.06, +0.06**	**-0.055, +0.055**	**-0.055, +0.055**	**-0.055, +0.055**	**-0.05, +0.05**

iNEMI

Selected Parameters for Automotive Electronics

Year of Production	*2015*	*2017*	*2019*	*2021*	*2023*	*2025*
Battery performancefor HEV (Power oriented development)						
Power density per weight (W/kg)	4000	4300	4450	4550	4650	4750
Energy density per weight (Wh/kg)	105	115	125	133	138	142
Battery performancefor BEV (Energy oriented development)						
Power density per weight (W/kg)	1350	1430	1480	1530	1580	1600
Energy density per weight (Wh/kg)	220	235	245	255	265	270
Capacitor pack (F)	227	240	254	260	260	260
Power devices						
Inverter power density (W/cm3)	13	20	25	35	45	55
Specific on-resistance at breakdown voltage of 1.2kV [mOhm*cm2@1.2kV]	5	4	3	2	2	2
Max junction temperature (degree C)	220	240	260	270	280	290
Rthja required for inverter power density (W/cm3) with regard to Ta of 125deg C (deg C/W/cm3)	7.3	5.8	5.4	4.1	3.4	3.0
Max mold temperature (deg C)	200	200	200	200	200	200
package termical resistance (m Ohm)	0.16	0.16	0.16	0.16	0.16	0.16
Logic devices						
Temperature attached to engine (degree C)	155	175	175	175	175	175
Max junction temperature (degree C)	160	175	180	185	190	195

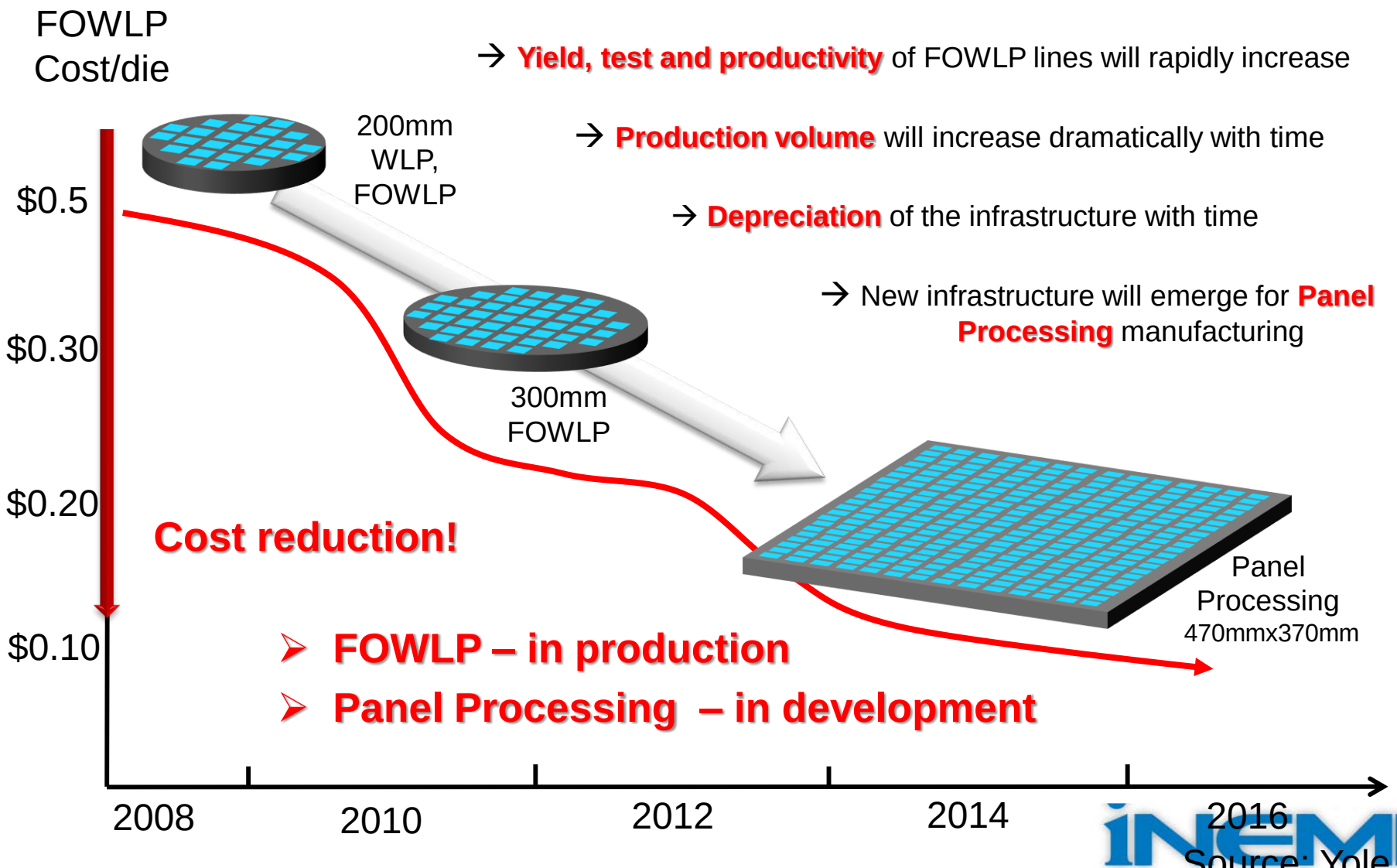
Gaps with no Known Solution

The most common reason for "*no known solution*" is cost not meeting market need

Potential Solutions include:

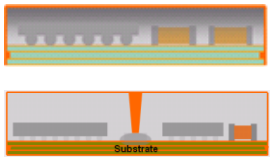
- **Increase parallelism in manufacturing**
- **Reduce the number of process steps**

WLP, FOWLP and Panel Processing Increase Parallelism and Reduce Cost

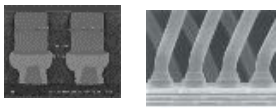


Source: Yole

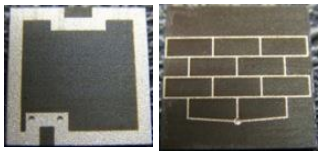
Electronic/Photonic Sip Through Heterogeneous Integration



Shielding
-Board or package level
-Compartmental



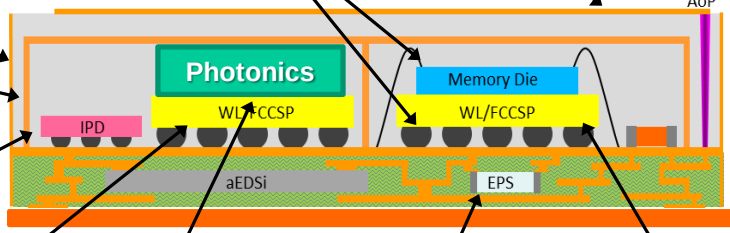
Interconnection
Flip Chip & Wire Bond



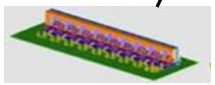
Antenna
-Package integration
for 2.4G/5G/60GHz

Molding
-MUF
-Exposed die

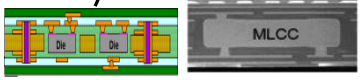
SMT
-Passives
-Components
-Connectors



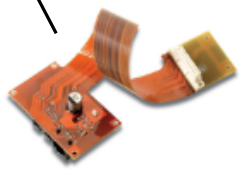
Passives/IPD
-Integrated Passive
Devices



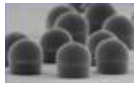
Photonics Layer
PIC Chip- optical bus



Embedded Technology
-Passive component
-Active device



Mechanical Assy
-Laser welding
-Flex bending

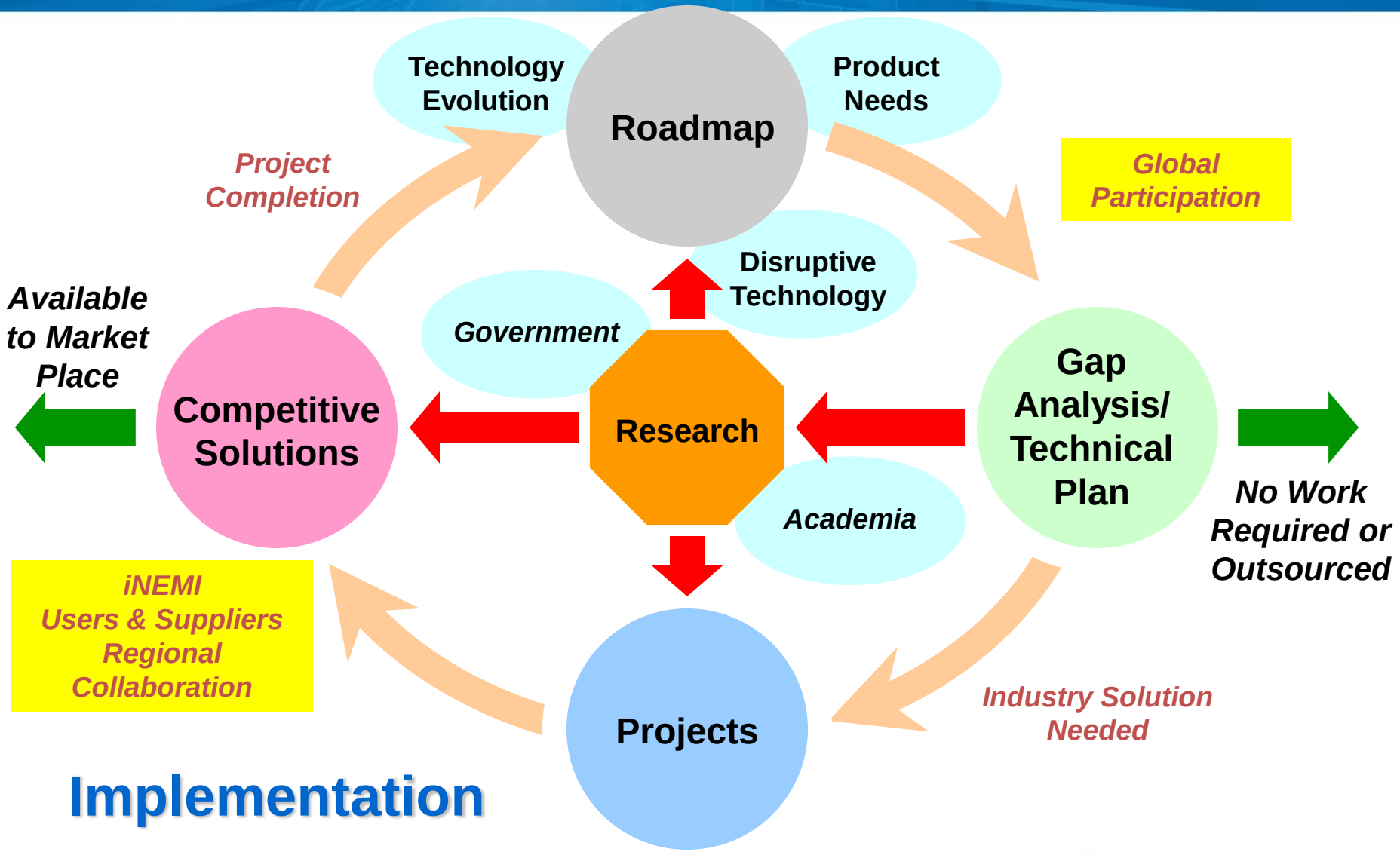


Wafer Bumping/WLP
-Leadfree / Cu Pillar
-Bare die package

Die/Pkg Stacking
-Die thinning
-Die interconnect

Source: ASE with additions

Next Steps: Identify Initiatives to Close Gaps



iNEMI Collaborative Project Activities

Why Collaborative Projects?

- **Reduce cost by leveraging resources**
  - Reduce cost by new technologies
  - Reduce resource demands and $ investments for each company
  - Stimulate standards and common specification development
  - Work on issues facing all your suppliers/customers
  - Disseminate efficient business practices

- **Reduce risk of technology introduction**
  - Gain knowledge and accelerate deployment of new technologies
  - Developing industry infrastructure, source of supply
  - Ensure reliability and technology readiness when required

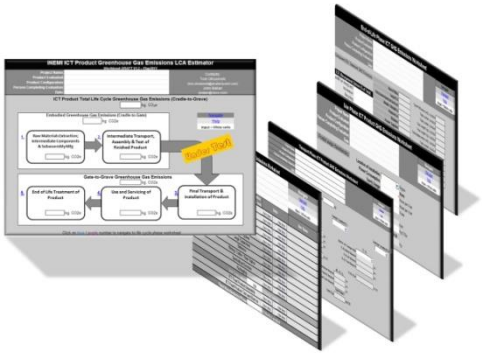
- **Reduce environmental risks**
  - Ensure sustainable solutions are put in place and in sync with industry

Profile of Successful iNEMI Projects

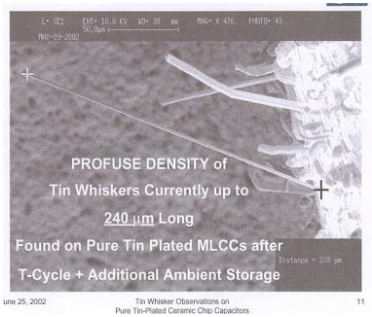
- **Addresses knowledge gap of industry**
  - **Common problem solved by working together**
  - **Often a pre-cursor to standards development**

- **Brings together a segment of supply chain to provide industry-wide response**

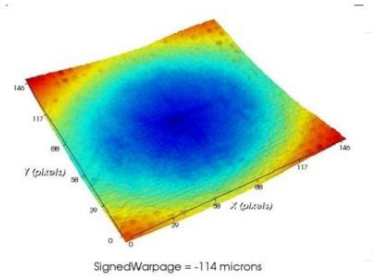
- **Direct alignment with member companies' commercial interests.**



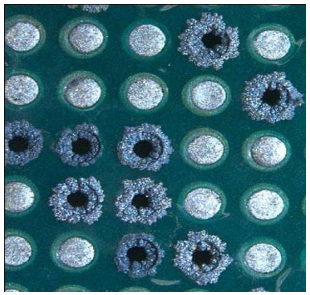
LCA Estimator



Tin Whisker Susceptibility



Warpage Characterization of Organic Packages



Creep Corrosion

18 New & Ongoing Projects

Project Name	TIG	Chair	Initiative - Start Date	Est End Date
BiSn Based Low Temperature Soldering Process and Reliability	BA	Intel	8/17/2015	9/30/2017
Characterization of Pb-Free Alloy Alternatives Project - - Addendum to Scope of Work Version 3.2 June 2, 2015	BA	Alcatel-Lucent		6/30/2017
Characterize and quantify the inspection capability of the AXI on HoP HiP (Head in Pillow) defects	Test	Intel	4/23/2015	
Connector High Speed Signaling Metrology Program: Phase 1	BA	Intel		3/31/2016
DC-DC Conversion Project - Phase 2		IBM		9/2/2016
Development of Cleanliness Specification for Expanded Beam	Opto	Celestica		4/29/2016
Final Assembly Automation and Optimization			1/12/2016	9/30/2017
Fine Pitch Circuit Pattern Inspection/ Metrology Project	Packaging	IBM	8/7/2015	
High Temp , Pb-free Die-Attach Material	Packaging	Indium	9/30/2015	
Impact of Low CTE Mold Compound on Board level Relability	Packaging	imec		
PCB/PCBA Material Characterization for Automotive Harsh Environments	BA	Alpha/Alent	1/4/2016	5/31/2017
QFN Package Board Level Reliability Project	BA	Alcatel-Lucent	10/15/2014	2/1/2017
Qualification Test Development for Creep Corrosion, Phase 3	BA	IBM	6/1/2015	2/4/2017
Reuse and Recycling Metrics - Phase 2	ESE	IBM	10/28/2015	12/15/2017
Semiconductor Package Miniaturization Test Vehicle for Medical Applications Program	Medical	MST	4/28/2015	2/28/2017
Ultra Low Loss Laminate/PCB for High Reliability & Performance	Organic PCB	Intel		5/31/2016
Value Recovery for EoL Electronics (Metals Phase 2)	ESE	Purdue		12/16/2016
Warpage Characteristics of Organic Packages Phase 3	Packaging	Intel	6/1/2015	12/11/2016

5 Active Initiatives

Initiative Name	iNEMI PM	TIG	Chair	Start Date
Quantify Impact of Board Design and Process Control to SMT Performance	H Fu	Board Assembly	Intel	7/31/2015
SiP Module Mold-ability Study	M Tsuriya	Packaging	SCK	12/18/2015
Develop Cleanliness Specification for Single-Mode and Multi-Mode Expanded Beam Connectors (SM and MM)	D Godlewski	Optoelectronics	Celestica	6/30/2016
Investigation of multi-pass interference (MPI) conditions and connector quality for Data Center applications	D Godlewski	Optoelectronics	Celestica	11/30/2016
Phase 2 - iNEMI Connector Reliability Test Recommendations	D Godlewski	Board Assembly		6/30/2016

iNEMI Involvement

iNEMI®
Advancing manufacturing technology




Lead & Learn

Tell me and I forget. Teach me and I remember. Involve me and I learn.

- Benjamin Franklin

- **iNEMI membership provides the critical mass required to affect significant changes**
  - **Set direction for future technologies**
  - **Influence supply base to develop solutions that will support product roadmap needs**
  - **Drive standardization to reduce cost and complexity through collaboration**
- **iNEMI consists of industry leaders, scientists and technologists with broad expertise**
  - **Senior people with 20+ years experience in the industry**

Why iNEMI

- **Strong Global Membership**
  - Depth and Breadth of Supply Chain Leaders
  - Strong set of Universities & Research Institutes
- **iNEMI Reputation**
  - Track record of sustainability leadership
  - In demand for knowledge/science input
  - Results oriented workshops
- **10 year Technology | Business Roadmap**
  - Delivered every two years
  - Unique Gap Analysis
  - Technical/Business Evolution Details
- **Proven Collaborative R&D Methodology**
  - Time tested over 20 years
  - 20-25 active collaborative R&D projects

iNEMI Member Testimonials

Flextronics depends on roadmaps coming from iNEMI. We need that level of support and visibility from a consortium like iNEMI that has a lot more visibility into the industry. — *Murad Kurwa, Flextronics*

These are the type of projects that not one company can do or drive it on its own. It really requires a collaborative effort across the entire supply chain.
— *Mostafa Aghazadeh, Intel*

iNEMI is providing me an incredible window into the industry and the opportunity to be connected at a very low cost with everybody in the industry.
— *Jean-Luc Pelissier, Universal Instruments*

Opportunities to Get Engaged

- **Engage in roadmap activities**
- **Purchase the iNEMI Roadmap at:**

www.inemi.org

***Become involved in collaborative projects:**

1. **Engage in existing projects**
2. **Participate in projects being planned and defined**
3. **Develop own proposal for project, which can be reviewed with iNEMI membership and technical committee (TC)**

***Project involvement requires iNEMI membership**

Completing the 2015 iNEMI Roadmap Cycle

- **2015 iNEMI Roadmap Development Cycle is wrapped up!**
- **2015 iNEMI Technology Plan Development Closed**
- **2015 iNEMI Research Priorities Document Development Closing and Available at www.inemi.org in late June**
- **2015 Roadmap Available to Industry Now:**
  - **Order the 2015 iNEMI Roadmap flash drive at www.inemi.org**
  - **Individual roadmap chapters are also available as a PDF document at www.inemi.org**
- **2017 iNEMI Roadmap moving forward with 7 product sectors and 21 technology chapters**
  - **Contact Chuck Richardson for more details at crichardson@inemi.org**
- **Get Involved in iNEMI – An organization with an Eye to the Future and a Means to Get There**

Thank You
For Your Time & Attention

iNEMI®
Advancing manufacturing technology




www.inemi.org

Bill Bader
bill.bader@inemi.org

Grace O'Malley
gomalley@inemi.org

Chuck Richardson
crichardson@inemi.org

iNEMI®
Advancing manufacturing technology

Back-up
Collaborative Project Examples

Advancing manufacturing technology

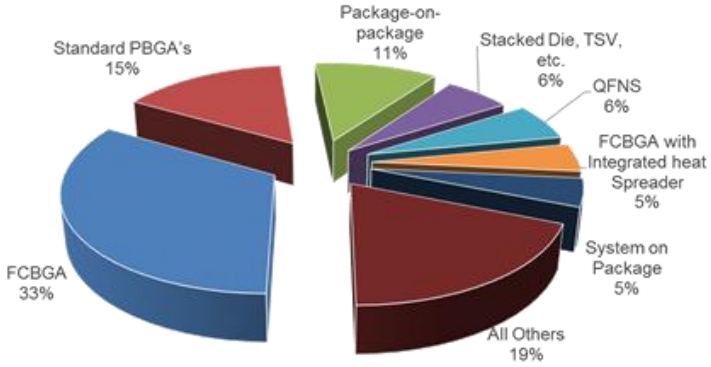
Warpage Characteristics of Organic Packages

Chair:
Wei Keat Loh, Intel
Ron Kulterman, Flextronics
Tim Purdie, Akrometrix

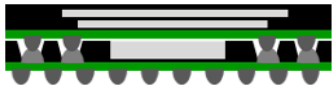
iNEMI®
Advancing manufacturing technology

Packaging Technology Considered in Project Phase 2

Interested Packaging Technology based on field survey



Generous Donation of Samples from Industry

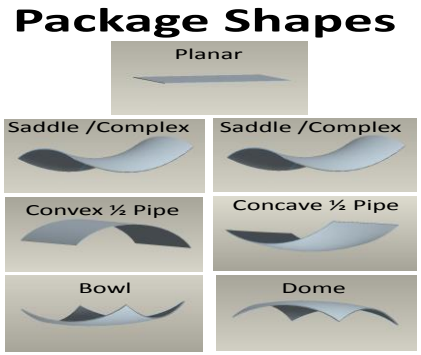
Package Type	*Design*	*Schematic drawing of package construction*
POP	Overmold TMV®	
	Expose Die TMV®	
	Bare Die POP	
	Interposer POP	
	Pre-stack POP package	
	MCeP®	
	POP Memories	
FCBGA	17x17-35x35mm	
FCBGA with Lid	Organic and ceramic substrate	
PBGA	Ranges	

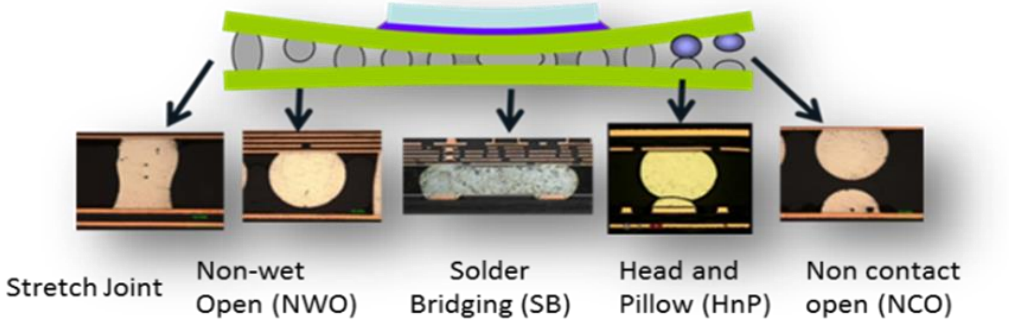
Objective:

1) To characterize the package warpage with respect to existing warpage allowable
2) To understand the impact of bake and moisture exposure

** Paper published at ICEP 2015 conference in Japan.*

Warpage Characteristics of Organic Packages
Phase 3 started in October 2015





- **Benchmark or fingerprint package warpage characteristics to develop a better understanding of the current trends of warpage behavior for different package constructions.**
  - **Small BGA Packages:**
    - **Interposer, 2.5D, 3D stack packages, through via silicon (TSV); Memory technology (High Band Width Memory, DDR)**
  - **Large BGA Packages**
    - **Package stiffeners – picture frame stiffener, different stiffener attachment method, shapes and sizes**
    - **Either organic substrate or ceramic substrate**
  - **System In Package/Multi Chip Package (BGA)**
    - **Stack Die or multiple die**
    - **Die on interposer and/or with asymmetrical layout.**
  - **Embedded Package (embedded silicon, actives and passives)**
- **The measurement will be done at respective tool manufacturer.**
- **Identify measurement methods and protocols based on the different measurement techniques and technology such as below:**
  - **Confocal techniques**
  - **Projection moiré techniques**
  - **Thermo moiré techniques with or without convective reflow**
  - **3D Digital Image Correlations (DIC)**
- **Other packaging materials and design evaluation if provided.**

QFN Package Board Level Reliability Project

Project Chairs：
Richard Coyle, Alcatel-Lucent
David Ihms, Delphi

iNEMI®
Advancing manufacturing technology

QFN Board Level Reliability Project

Problem Statement:	**Published QFN thermal cycling data are lacking for characterizing longer product lifetimes, in more aggressive use environments, particularly using thicker printed circuit boards typical of higher reliability applications**

Project Leader(s):	**Richard Coyle – Nokia** **David Ihms - Delphi**	**Project Start:**	**Aug 5, 2015**
		Estimated End:	**Feb, 2017**

Purpose and Scope of Project

- **Provide QFN BLR data as a function of three printed circuit board thicknesses and two different thermal cycles. This will provide guidance for translating data from one board thickness or one temperature cycle to another.**
- **Compare the reliability performance of non-wettable and wettable surfaces on the QFN board attachments. Wettable side surfaces are being proposed to generate side fillets for increasing the thermal fatigue resistance.**
- **Industry standard testing protocols based on IPC-9701 will be used to evaluate the board level reliability.**

Project Tasks

- **Material Selection**
- **Design of Experiment**
- **Test Board Design**
- **Board and Device Properties Characterization**
- **QFN Assembly, Test board fabrication, Stencil fabrication**
- **SMT**
- **Test and Data Collection**
- **Report**

Status Update

Two QFN suppliers, six unique QFNs; 10x10 and 9x9 designs
Rigid board designed and under fabrication
Flex board design delayed
Stencils provided by LaserJob
All necessary "in-kind" resources identified
The iNEMI variant molding compound CTE project is supported by this TIG; test board, assembly, and thermal cycle testing

Team Members

Stencil Fab:

QFN Packages

	Wettable (Dimple)	STD1	w/ FLK (step cut)	Wettable1 AOZG V766 (A): Dimple	A02L VFQFPN w/o Wet FLK	A02L VFQFPN w/ Wet FLK
PKG Size (mm)	10 x 10	10 x 10	10 x 10	9 x 9	9 x 9	9 x 9
PKG Height	0.9	0.9	0.9	1.0?	1.0	1.0
Lead Count	68	68	68	64	64	64
Lead Pitch (mm)	0.5	0.5	0.5	0.5	0.5	0.5
Flag Size (mm) (Pad to PKG ratio)	7.7x7.7 (59.3%)	7.7x7.7 (59.3%)	7.7x7.7 (59.3%)	6.9 x 6.9 (58.8%)	4.55 x 5.25 (29.2%)	4.55 x 5.25 (29.2%)
Die Size (mm) (DTP ratio)	MAX 6.5x6.5 (42.3%)	MAX 6.5x6.5 (42.3%)	MAX 6.5x6.5 (42.3%)	5.0 x 4.2 (25.9%)	4.0 x 3.0 (14.8%)	5.0 x 4.2 (25.9%)
Leadframe Thick	0.2mm	0.2mm	0.2mm	0.2mm	0.2mm	0.2mm
Leadframe Material	C194	C194	C194	CuFe2P etched	CuFe2P etched	CuFe2P etched
Surface Finish	Ni/Pd/Au	Ni/Pd/An	Sn	Ni/Pd/Au	Ni/Pd/Au	Ni/Pd/Au
Singulation Method	Saw	Saw	Saw	Saw	Saw	Saw
Mold Compound Type	High Rel EMC	High Rel EMC	High Rel EMC	High Rel EMC	High Rel EMC	High Rel EMC
Mold Compound Name	G700	G700	G700	CEL9220	CEL9220	CEL9220
CTE 1	10ppm	10ppm	10ppm	8 ppm	8 ppm	8 ppm
CET 2	39ppm	39ppm	39ppm			
Bonding Wire	Au	Au	Au	Au/Cu	Au/Cu	Au/Cu
Dia.	0.8mil	0.8mil	0.8mil	1.0mil	1.0mil	1.0mil

iNEMI Project
BiSn Based Low Temperature Soldering Process and Reliability

Co-Chairs:
Raiyo Aspandiar, Intel
Scott Mokler, Intel

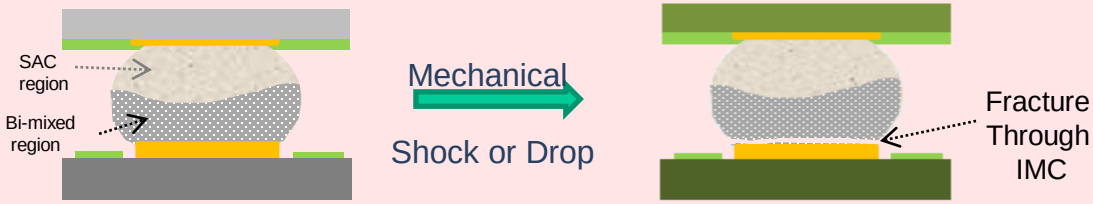
iNEMI®
Advancing manufacturing technology

Project Purpose

❖ **To assess the surface mount processibility and reliability of the solder joints formed when enhanced low temperature Bi-Sn based solder pastes are used for assembling electronic components on printed circuit boards.**

Problem Statement for low temperature Bi-Sn Solders

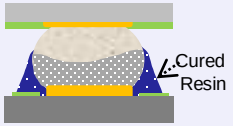
- **Bi causes hardening of the solder joints which are prone to brittle fractures under mechanical shock and drop forces**



Two Solution Paths to be Evaluated

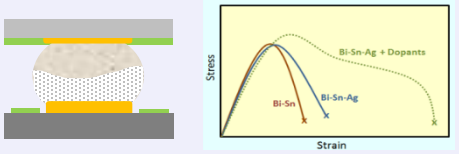
Resin Reinforcement

Resin added to the solder paste cures during reflow and provides reinforcement under mechanical stresses



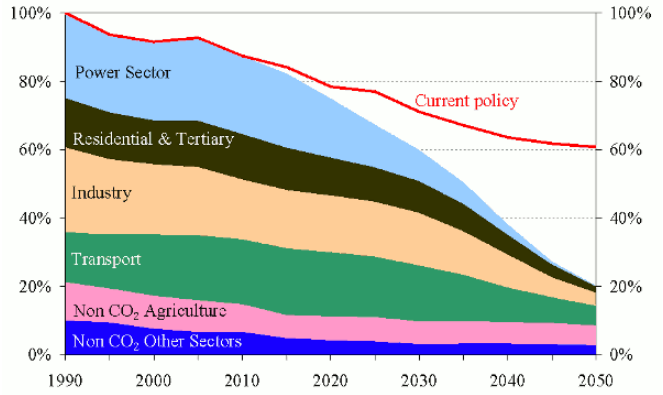
Ductile Bi-Sn Metallurgy

Addition of Elemental Dopants increases ductility of BiSn solder by modifying microstructure and Intermetallic compound morphology

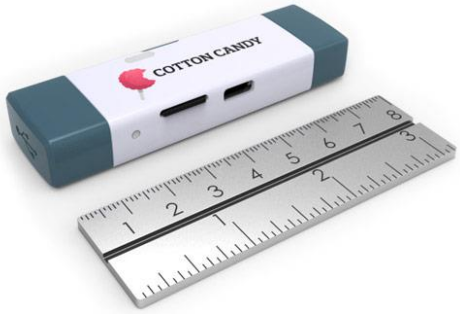


Drivers for Low Temperature Soldering

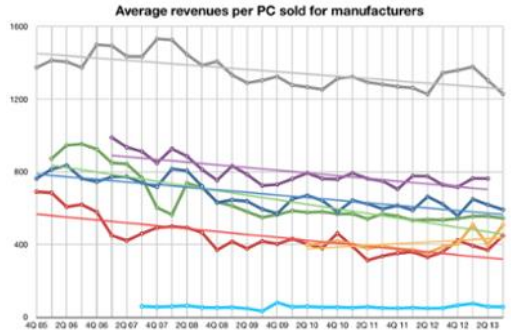
Green House Gas Reduction



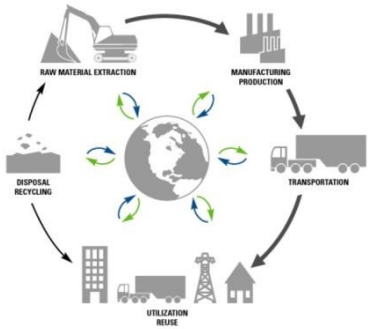
SMT Margin for Thin Designs



Lower Electricity Usage Reduces Cost



Reduced PLC Environmental Impact

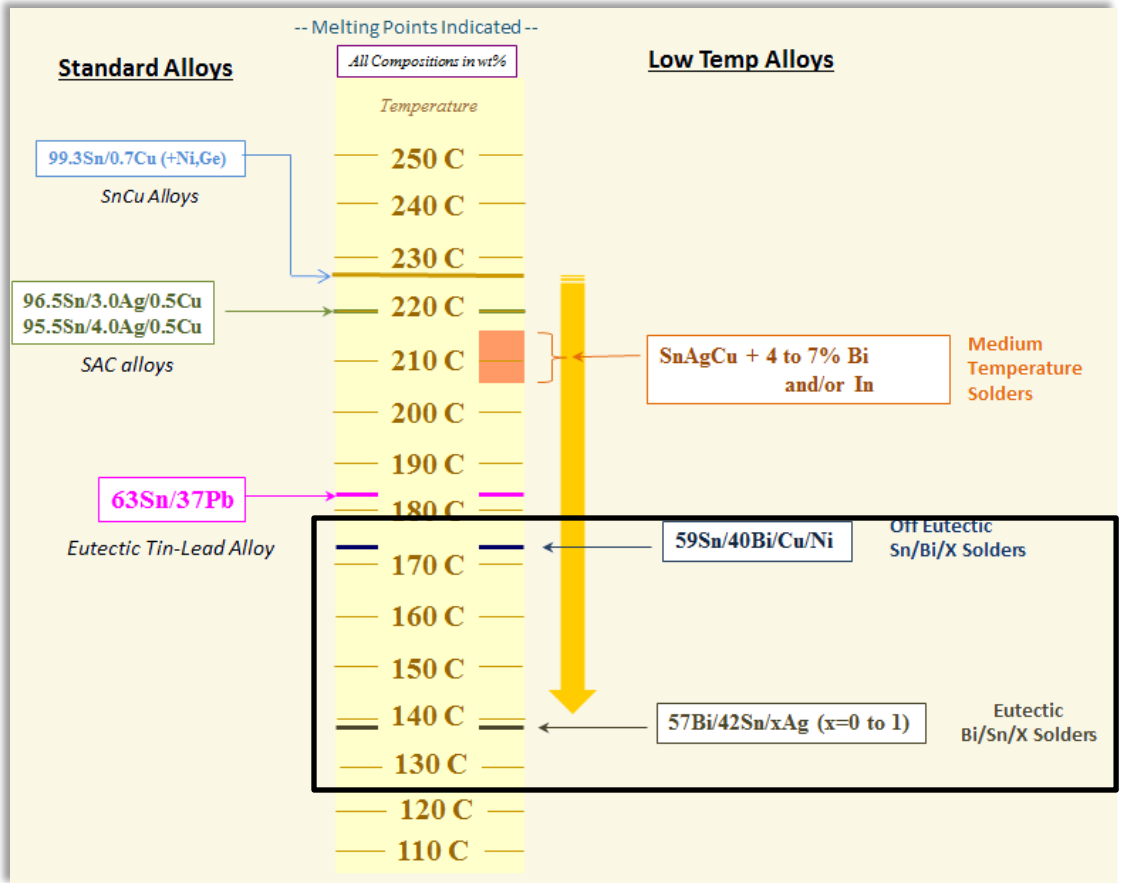


➢ **Low Temp Solders Provide Benefit to Each of These Challenges**

iNEMI

Low Temperature Solders

- There are a variety of compositions and melting ranges for Potential Low Temperature Solders in Electronics Manufacturing



Medium Temperature Solders [SnAgCu+Bi,In]

- melt in the 210 to 220C range

Low Temperature Solders [Bi/Sn/X, X=Ag,Cu,Ni]

- melt in the 139 to 175C range

- **Bi-Sn system solders are being proposed for this Project**
  - **More processing and economic benefits than Medium Temperature Solders**

Project Plan

- **Objective:**
  - **To assess the two solution paths available for mitigating mechanical drop / shock risks associated with Bi-Sn based solder pastes for SMT assembly**

- **Scope**
  - **Solder Pastes**
    - ductile Bi-Sn metallurgy
    - Resin Reinforced Bi-Sn based
    - SAC305 (for comparison)
    - standard BiSnAg (for comparison)
  - **Components**
    - High density BGAs
    - BTCs (such as QFNs)
    - Chip components
    - Other Non-IC (Switches, Connectors)
  - **Board Surface Finishes**
    - OSP
    - ENIG
    - ENEPIG
    - Other
  - **SMT Process Development**
    - Stencil Printing
    - Reflow Soldering
    - Rework Process
  - **Shock/Drop Evaluation using Test Vehicle Designs**
    - Per JEDEC or other standards
  - **Thermal cycling**
    - 2nd phase
  - **Product Validation**
    - Boards Assembled with Best performing solder pastes from each category
    - Subjected to selected Product level functional and mechanical shock/drop tests
    - 2nd phase