Study of the Impedance of the Bypassing Network of a Switching Cell – Influence of the Positioning of the Decoupling Capacitors

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Parasitic elements induce:
- HF oscillations leading to Common and Diff. Modes currents ⇒ expensive & bulky filtering required
- Overvoltages at switches turn-on force to oversize components ⇒ cost, increased losses, reduced performances

- Effects worsen by the use of Wide-BandGap semiconductors

- Minimise oscillations and overshoots:
  ⇒ Minimise parasitic inductances
  ⇒ Maximise compactness

- Good thermal performances:
  • Improves reliability, efficiency, derating
  • Low thermal coupling between components
  ⇒ Space components

Trade-off between electrical and thermal performances

+ Modularity, shared heatsink and bypass capacitors for multi-cellular converters

- Study the effects of parasitic inductances on a switching cell
- Quantify the trade-off between electrical and thermal performances
Agenda

1. Introduction
2. Oscillation mechanisms in a switching cell
3. Influence of the distance between a switching cell and its bypassing network
4. Conclusion
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Bypassing network impedance diagram

Schematic with parasitic elements:
(mutual inductances and resistances neglected)

Circuit under study:

DC-link cap.

Local bypass cap.

Switching Node Voltage

\[ f_{osc,1-3} = \begin{cases} 
30 \text{ kHz} \\
1.5 \text{ MHz} \\
187 \text{ MHz} 
\end{cases} \]
Bypassing network impedance diagram

**Schematic with parasitic elements:**
(mutual inductances and resistances neglected)

**Impedance seen from the load:**
(Q\textsubscript{HS} on, Q\textsubscript{LS} off)

**Assume:**
\begin{align*}
C\textsubscript{out} & \ll C\textsubscript{X7R} \ll C\textsubscript{bulk} & L_1 & \ll L_2 \ll L_3
\end{align*}

\[ f\text{res}_1 \gg f\text{res}_2 \gg f\text{res}_3, \quad f\text{res}_i = \left(2\pi \sqrt{L_i C_i}\right)^{-1} \]

\Rightarrow \quad \text{Decoupled loops}

**Increasing oscillation frequency**
Model

- Neglect damping
- Assume high switching speed
  (hard to estimate a priori)

**Δ** = $I_{ld} \sqrt{\frac{L}{C}}$

$\Delta V = V_{bus} = $ DC-link voltage
Oscillation mechanisms: synthesis

Current step

- HF overvoltage: \( \Delta V = I_{ld} \cdot Z_c \), \( Z_c = \sqrt{L_1/C_{out}} \)
- LF overvoltage: \( \Delta V = I_{ld} \cdot Z_c \), \( Z_c = \sqrt{L_2/C_{X7R}} \)
- VLF overvoltage: \( \Delta V = I_{ld} \cdot Z_c \), \( Z_c = \sqrt{L_3/C_{bulk}} \)

Voltage step

- HF overvoltage: \( \Delta V = V_{bus}e^{-\pi/\sqrt{4Q^2-1}} \approx V_{bus} \)
- LF overvoltage: \( \Delta V = V_{bus} \cdot \left| \frac{c_1}{c_{out}} - \frac{L_1}{L_2} \right|^{-1} \approx 0 \)
- VLF overvoltage: \( \Delta V \approx 0 \)

- The overall overvoltage should consider interferences between spectral components
- Hypothesis valid for fast edges: \( t_r \approx 0 \), ie. \( \frac{1}{\pi t_r} > f_{res} \)

\( \iff \) edge fast enough to stimulate the mode
- Simplified equations: unknown damping
- Worst-case scenario
Model experimental validation

\[ V_{bus} \approx 30 \text{ V} \Rightarrow q_1 \approx 6 \]

Fast edges assumption:

\[ \frac{1}{\pi t_r} > f_{res} \Leftrightarrow t_r < 2\sqrt{C_{out} \cdot L_1} \]

<table>
<thead>
<tr>
<th>( C_{out} )</th>
<th>( L_1 )</th>
<th>Related devices</th>
<th>( 2\sqrt{C_{out} \cdot L_1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 pF</td>
<td>1 nH</td>
<td>GaN</td>
<td>0,63 ns</td>
</tr>
<tr>
<td>1 nF</td>
<td>1 nH</td>
<td>GaN / SiC / Si</td>
<td>2 ns</td>
</tr>
<tr>
<td>1 nF</td>
<td>10 nH</td>
<td>SiC / Si</td>
<td>6,3 ns</td>
</tr>
<tr>
<td>10 nF</td>
<td>100 nH</td>
<td>Si</td>
<td>63 ns</td>
</tr>
</tbody>
</table>

- Strong assumption for silicon devices
- Reasonable assumption for low voltage GaN
- Designers therefore need:
  - 50 % \( V_{ds} \) -derating
  - Artificially decrease slew-rates
  - Increase \( C_{out} \)
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Circuit under study (1)

Bulk capacitor
\( C_{\text{bulk}}: \text{MKP, 875 V} - 15 \, \mu\text{F} \)

Local bypassing
\( C_{X7R}: X7R \)
1 kV – 470 nF @0 Vdc
Package 2220

Integrated GaN switching cell & driver
TI’s LMG5200
80 V – 10 A – 15 mΩ

24/06/2019
Yoann Pascal
Circuit under study (2)

Switching cell

+ floating copper plane, 400 µm below
Measurements & inductance estimation

- Measured switching node voltage fitted with:

\[
V_{sw}^* = V_{dc} + \sum_{k=1}^{k=3} \hat{V}_k \cdot \sin(\omega_k t + \phi_k) \cdot e^{-t/\tau_k}
\]

Optim. vector: \( \beta = [V_{dc}, \hat{V}_k, \omega_k, \phi_k, \tau_k] \)

\[ \Rightarrow L_k = \frac{1}{\omega_k^2 \cdot C_k} \]
Inductance vs. distance

- Low impact of $d_x$ on $L_x$
- Slow inductance increase: 300 pH/cm
- Predominance of the bulk capacitor ESL on the loop inductance
- Moderate inductance, even for $d_{X7R} = 300$ mm

Small signal measurements yields similar results
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Conclusion

Oscillation mechanisms in a switching cell:

- For fast enough devices, 2 mechanisms are at stakes:
  - Voltage-step induced overvoltage: $\hat{V} = V_{bus}$ regardless of the parasitic inductances
  - Current-step induced overvoltage: $\hat{V} = I_{ld} \cdot Z_c$, for each loop $\Rightarrow$ minimise parasitic inductances

Influence of the distance between a switching cell and its bypassing network:

- Low impact of the distance on the inductance thanks to:
  - Simple but effective layout (edge-coupled micro-strip)
  - Bottom side copper plane
  - Thin (400µm) substrate

Given the layout under study:

- Moderate inductance, even at high distances (11 nH @30 cm)
- Degree of liberty on the components positioning:
  - Improved performances
  - Simplified cooling & mechanical design/layout
  - Component sharing: heatsink, bypass capacitors
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