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Study of the Impedance of the Bypassing Network of a Switching Cell – Influence of the Positioning of the Decoupling Capacitors

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Introduction

- Parasitic elements induce:
  - HF oscillations leading to Common and Diff. Modes currents ⇒ expensive & bulky filtering required
  - Overvoltages at switches turn-on force to oversize components ⇒ cost, increased losses, reduced performances
- Effects worsen by the use of Wide-BandGap semiconductors

- Minimise oscillations and overshoots:
  - ⇒ Minimise parasitic inductances
  - ⇒ Maximise compactness

- Good thermal performances:
  - Improves reliability, efficiency, derating
  - Low thermal coupling between components
  - ⇒ Space components

Trade-off between electrical and thermal performances

\+ Modularity, shared heatsink and bypass capacitors for multi-cellular converters

- Study the effects of parasitic inductances on a switching cell
- Quantify the trade-off between electrical and thermal performances

Agenda

1. Introduction
2. Oscillation mechanisms in a switching cell
3. Influence of the distance between a switching cell and its bypassing network
4. Conclusion

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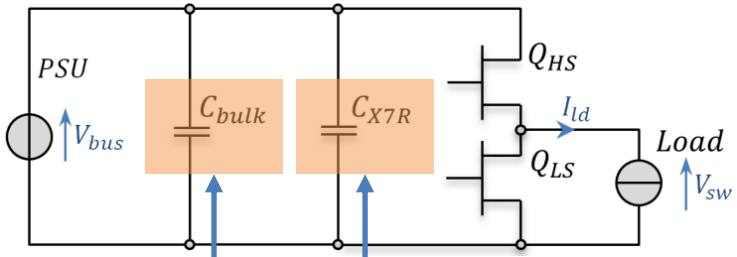
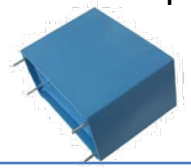
Bypassing network impedance diagram

Circuit under study:



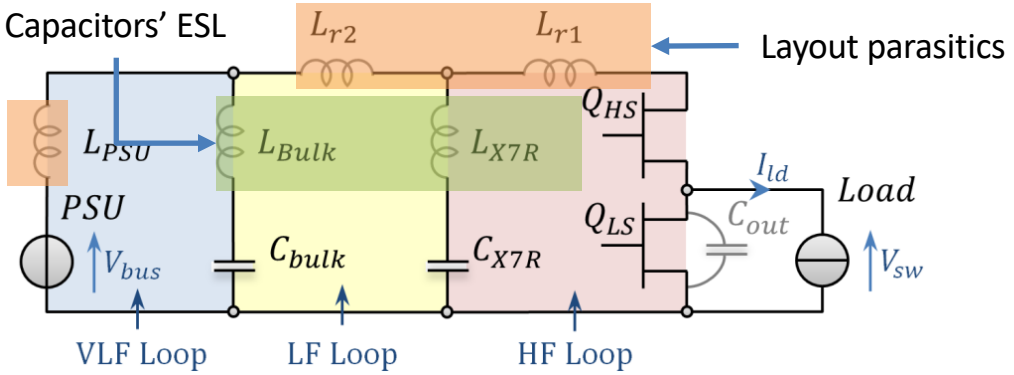
DC-link cap.

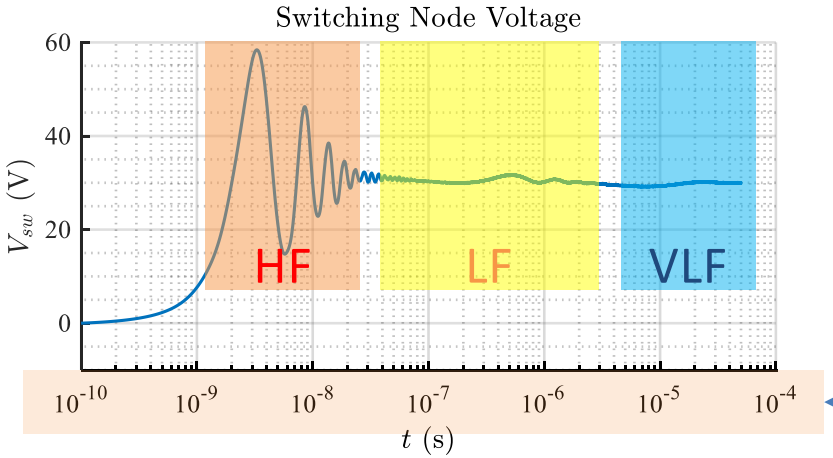


Local bypass cap.

Schematic with parasitic elements:

(mutual inductances and resistances neglected)





Log-time-scale

$$f_{osc,1-3} = \begin{Bmatrix} 30\ \text{kHz} \\ 1.5\ \text{MHz} \\ 187\ \text{MHz} \end{Bmatrix}$$

Bypassing network impedance diagram

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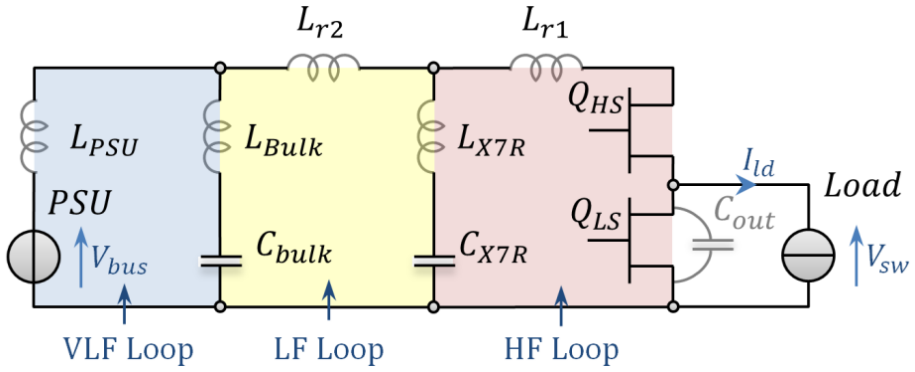
(mutual inductances and resistances neglected)



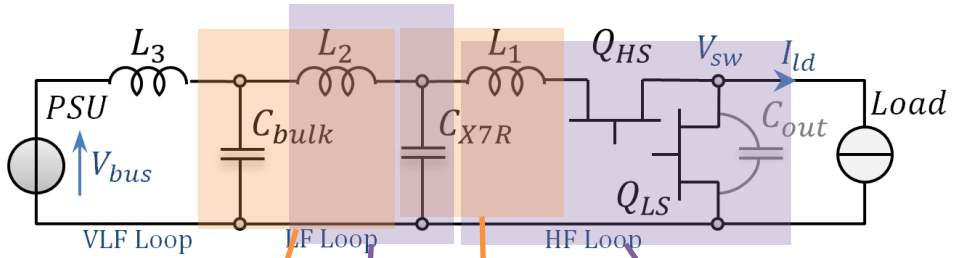
Increasing oscillation frequency

Simplified model:

- Assume: $C_{out} \ll C_{X7R} \ll C_{bulk}$ & $L_1 \ll L_2 \ll L_3$

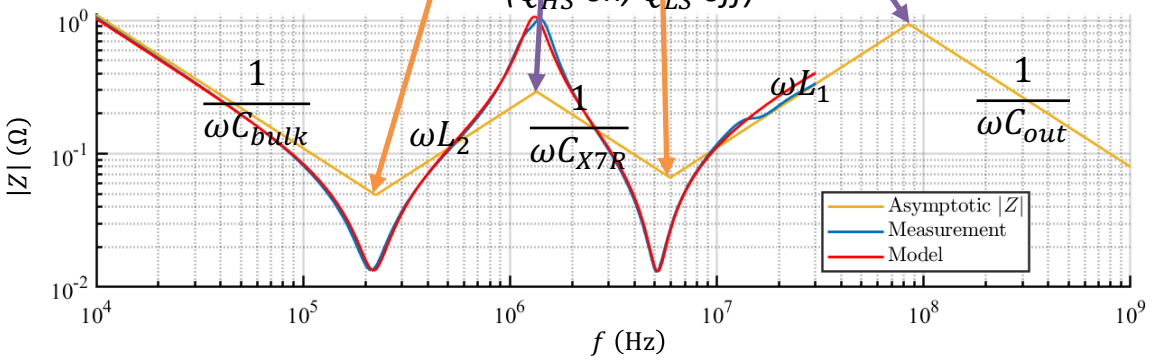
  $\Rightarrow \quad f_{res_1} \gg f_{res_2} \gg f_{res_3}, \quad f_{res_i} = \left(2\pi\sqrt{L_i C_i}\right)^{-1}$

  $\Rightarrow$ Decoupled loops

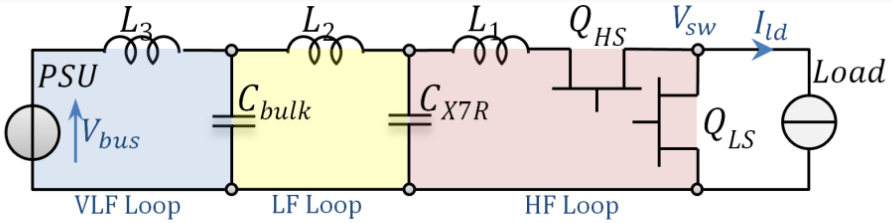


Impedance seen from the load:

(Q_{HS} on, Q_{LS} off)



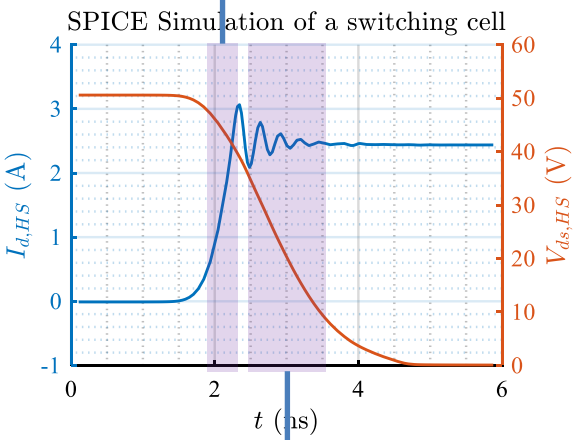
Model



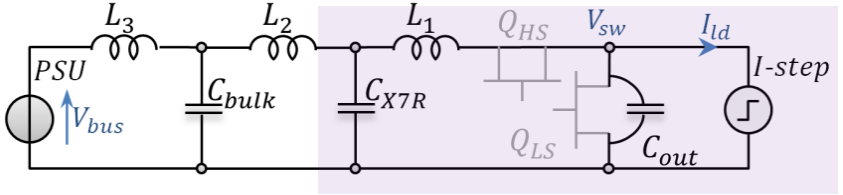
- Neglect damping
- Assume high switching speed

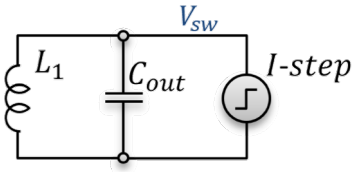
  (hard to estimate a priori)

I-step:

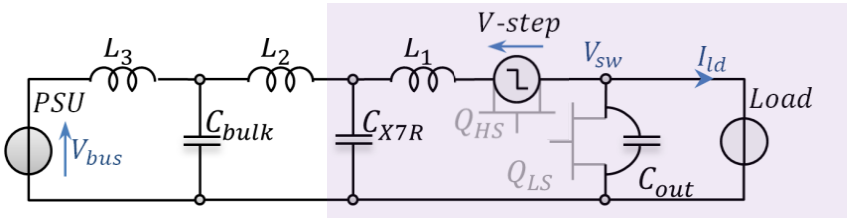


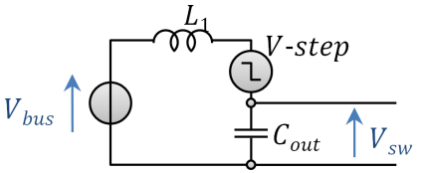
V- step:





$$\Delta V = I_{ld}\sqrt{\frac{L}{C}}$$





$$\Delta V = V_{bus}$$

= DC-link voltage

Oscillation mecanisms: synthesis

Current step

- HF overvoltage: $\Delta V = I_{ld} \cdot Z_c, \quad Z_c = \sqrt{L_1/C_{out}}$
- LF overvoltage: $\Delta V = I_{ld} \cdot Z_c, \quad Z_c = \sqrt{L_2/C_{X7R}}$
- VLF overvoltage: $\Delta V = I_{ld} \cdot Z_c, \quad Z_c = \sqrt{L_3/C_{bulk}}$

Voltage step

- HF overvoltage: $\Delta V = V_{bus} e^{-\pi/\sqrt{4Q^2-1}} \approx V_{bus},$

LF overvoltage: $\Delta V = V_{bus} \cdot \left| \frac{C_1}{C_{out}} - \frac{L_1}{L_2} \right|^{-1} \approx 0$

- VLF overvoltage: $\Delta V \approx 0$

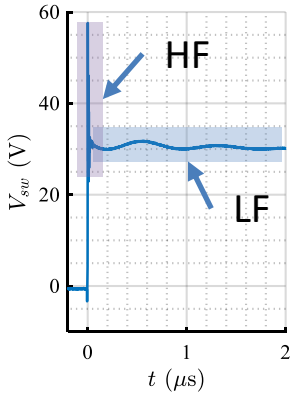
- The overall overvoltage should consider interferences between spectral components
- Hypothesis valid for fast edges:

$$t_r \approx 0\,, \qquad ie.\ \frac{1}{\pi t_r} > f_{res}$$

⇔ edge fast enough to stimulate the mode

- Simplified equations: unknown damping
- Worst-case scenario

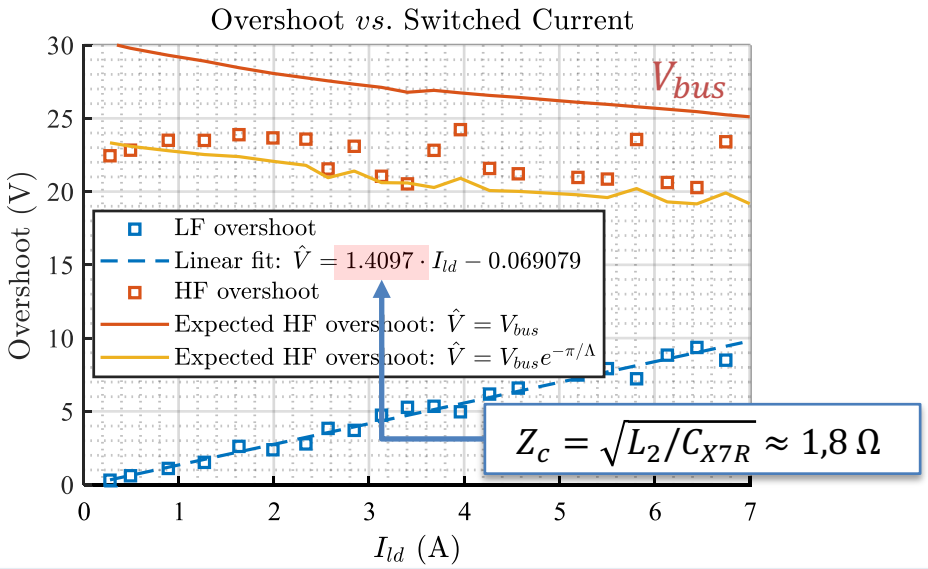
Model experimental validation



GaN switching cell

$V_{bus} \approx 30$ V

$\Rightarrow Q_1 \approx 6$



Fast edges assumption:

$$\frac{1}{\pi t_r} > f_{res} \Leftrightarrow t_r < 2\sqrt{C_{out} \cdot L_1}$$

C_{out}	L_1	Related devices	$2\sqrt{C_{out} \cdot L_1}$
100 pF	1 nH	GaN	0,63 ns
1 nF	1 nH	GaN / SiC / Si	2 ns
1 nF	10 nH	SiC / Si	6,3 ns
10 nF	100 nH	Si	63 ns

Max t_r so that the asumption holds

- Strong assumption for silicon devices
- Reasonable assumption for low voltage GaN
- Designers therefore need:
  - 50 % V_{ds} -derating
  - Artificially decrease slew-rates
  - Increase C_{out}

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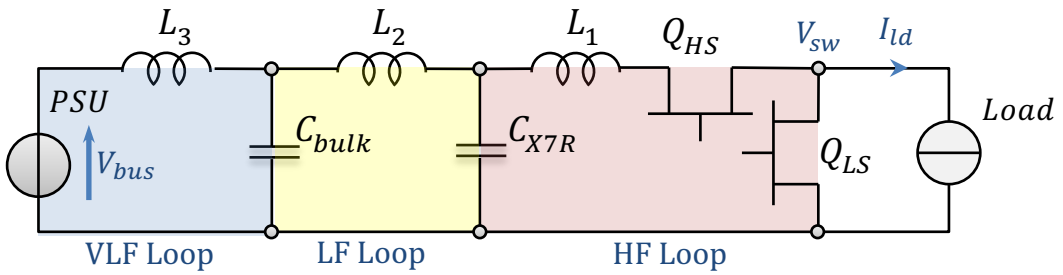
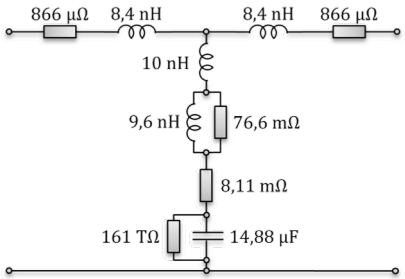
Circuit under study (1)



Bulk capacitor

C_{bulk} : MKP, 875 V – 15 µF



Local bypassing

C_{X7R} : X7R

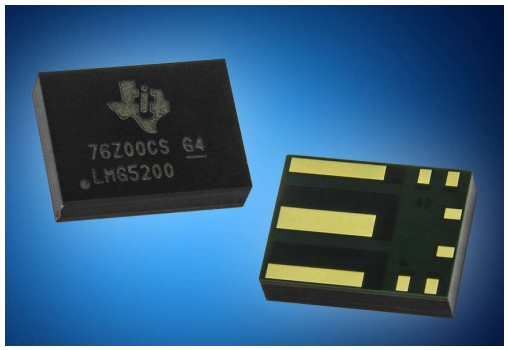
1 kV – 470 nF @0 V_{dc}

Package 2220

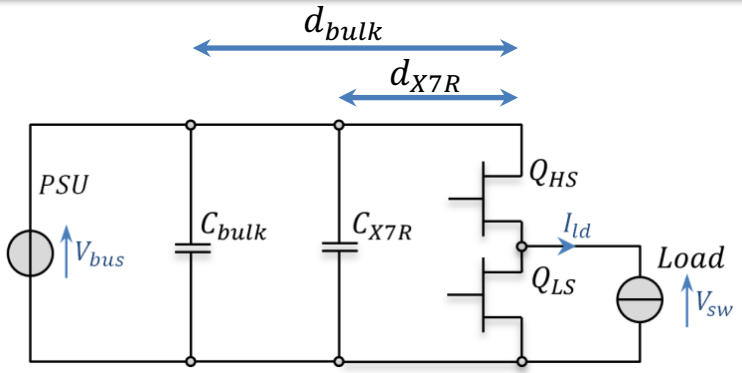
Integrated GaN switching cell & driver

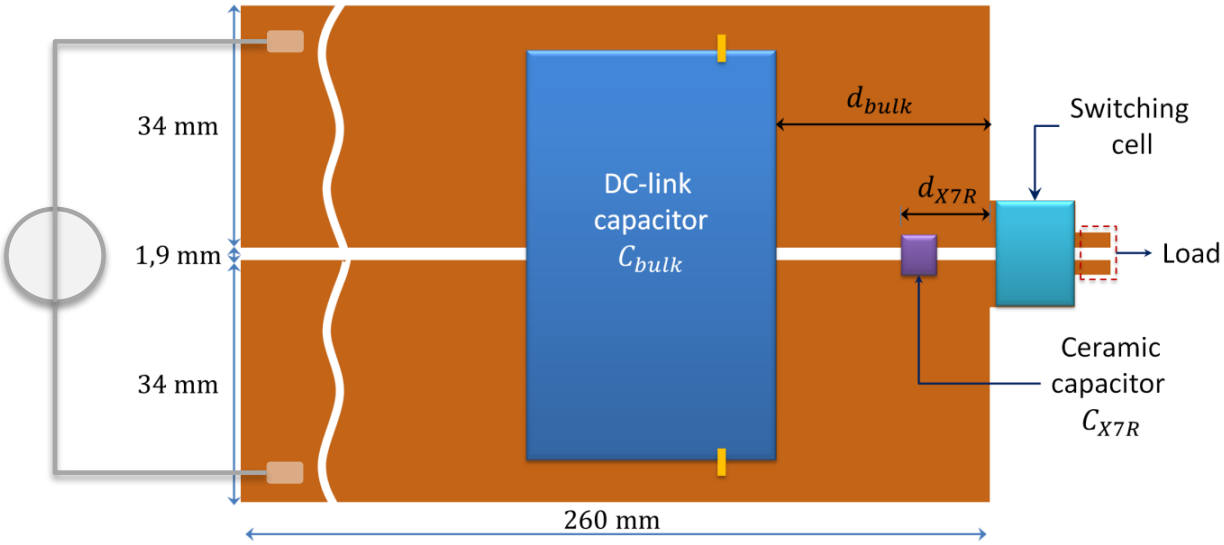
TI's LMG5200

80 V – 10 A – 15 $m\Omega_{typ}$

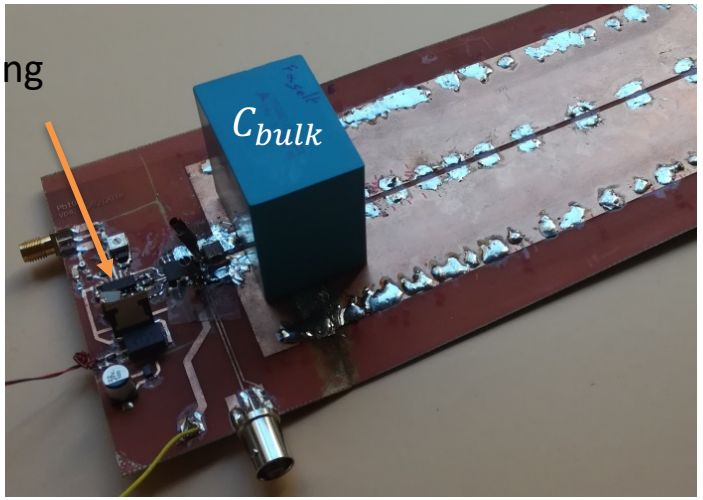


Circuit under study (2)





Switching cell



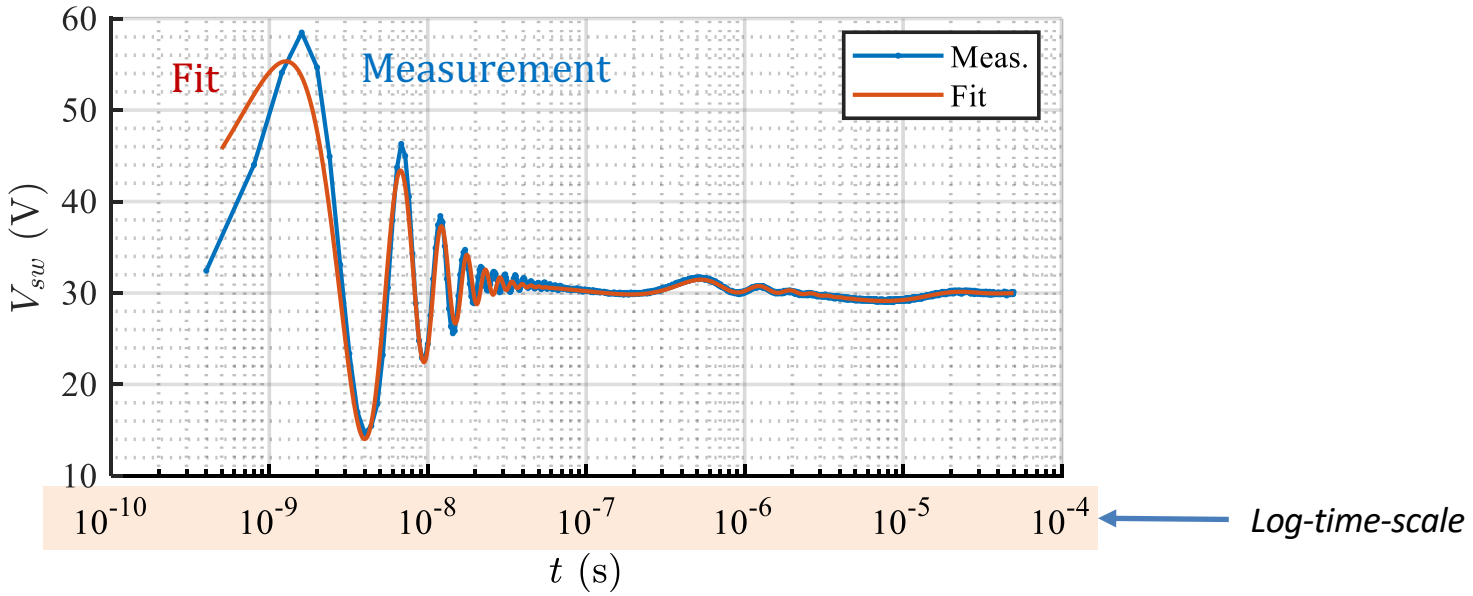
+ floating copper plane, 400 µm below

Measurements & inductance estimation

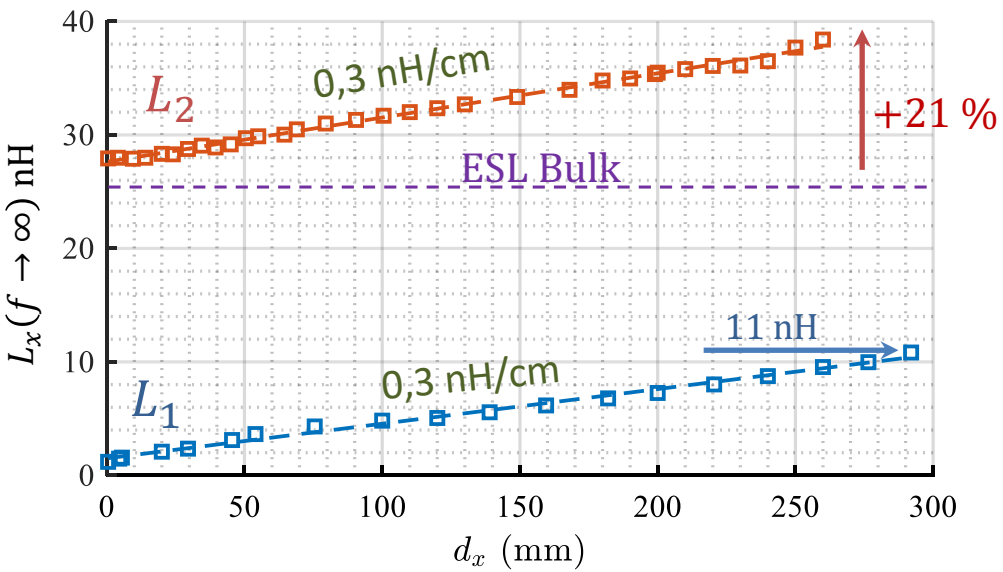
- Measured switching node voltage fitted with:

$$V_{sw}^{*} = V_{dc} + \sum_{k=1}^{k=3} \hat{V}_k \cdot sin(\omega_k t + \phi_k) \cdot e^{-t/\tau_k} \qquad \Rightarrow \; L_k = \frac{1}{\omega_k^2 \cdot C_k}$$

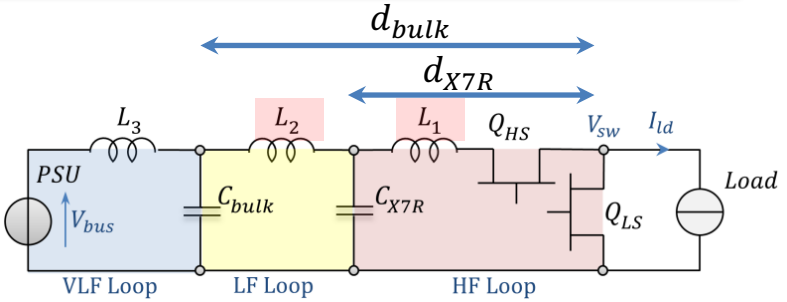
Optim. vector: $\beta = [V_{dc}, \hat{V}_k, \omega_k, \phi_k, \tau_k]_k$



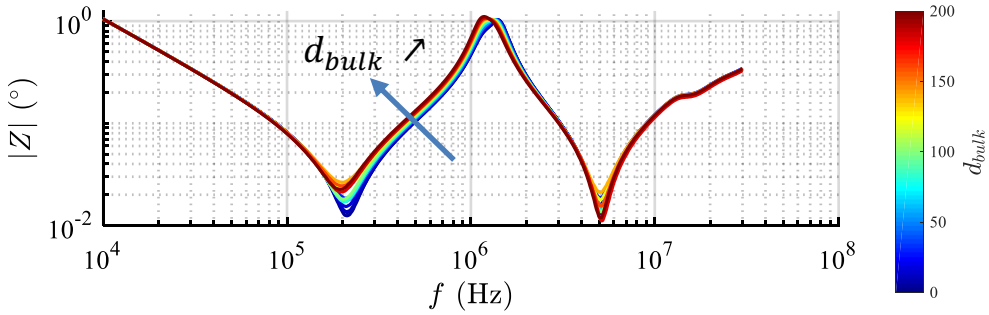
Inductance $vs.$ distance



- Low impact of d_x on L_x
- Slow inductance increase: 300 pH/cm
- Predominance of the bulk capacitor ESL on the loop inductance
- Moderate inductance, even for $d_{X7R} = 300$ mm



Power network impedance diagram:
(Q_{HS} on, Q_{LS} off, output connected to a Z-analyser)



Small signal measurements yields similar results

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Conclusion

Oscillation mechanisms in a switching cell:

- For fast enough devices, 2 mechanisms are at stakes:
  - Voltage-step induced overvoltage: $\widehat{V} = V_{bus}$ *regardless of the parasitic inductances*
  - Curent-step induced overvoltage: $\widehat{V} = I_{ld} \cdot Z_c,$ for each loop ⇒ *minimise parasitic inductances*

Influence of the distance between a switching cell and its bypassing network:

- Low impact of the distance on the inductance thanks to:
  - Simple but effective layout (edge-coupled micro-strip)
  - Bottom side copper plane
  - Thin (400µm) subtrate

Given the layout under study:

- Moderate inductance, even at high distances (11 nH @30 cm)
- Degree of liberty on the components positionning:
  - Improved performances
  - Simplified cooling & mechanical design/layout
  - Component sharing: heatsink, bypass capacitors

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