Stacked DBC Cavitated Substrate for a 15-kV Half-bridge Power Module

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Outline

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- Literature Review: High Voltage Substrate Design
- Proposed Substrate Design
  - Parametric E-field Map
  - Parametric Thermal and Stress Map
  - PCM Integration
  - Stacking Procedure
- Conclusion and Future Work
Motivation

Medium Voltage Applications:
- High voltage circuit breakers
- Solid-state transformers
- Power conversion for shipboards and railroads

Simplification of the Systems:
- LV WBG devices: Multi-level topologies required
- HV (≥10 kV) SiC devices: Simpler topologies

Packaging of HV SiC Devices:
- High power-density
HV Substrate Design Considerations

- High voltage isolation
  - Alumina & AlN DBC/DBA
    - DC: 20 kV/mm
    - AC: 16 kV/mm

- Electric field (E-field) mitigation
  - Triple points
  - Partial-discharge control

- Low parasitic capacitance
  - Low conducted EMI emissions

- High thermal conductivity

- Low parasitic inductances (power-loop)
  - High switching speeds SiC devices
  - Ensure low voltage stress


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Change E-field distribution

- Linear Resistive Material (conductivity not dependent on field)
- Non-linear Resistive Material (ZnO-Polyimide)
- Insulation/Passivation Material (PAI/BCB)
- Refractive Grading Materials
  - Polymeric matrix filled with high permittivity particles (BaTiO$_3$)
Modify substrate structure and edge

Conventional
MESA structures/ Protruding ceramics
Stacked substrates

Field plate

- Modify substrate structure and edge
- Conventional
- MESA structures/ Protruding ceramics
- Stacked substrates

References:

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Stacked Substrate

Cross-section of a conventional DBC substrate for LV-HB power module

Cross-section of a stacked DBC substrate for HV-HB power module


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Proposed Stacked DBCs Cavitated Substrate

- Replicate the top surface metallization pattern on each interlayer and the bottom surface metallization

- Formation of independent series-connected capacitors under DC+, DC- and AC top surface metallization

For $n = 5$, 80% reduction in the common-mode capacitance
Table: Mesh Independent Measurement

<table>
<thead>
<tr>
<th>Total ceramic thickness (mm)</th>
<th>No. of ceramic layers</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
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</table>
E-field Parametric Map

IWIPP 2019

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Voltage Distribution in DBC Stack

Parasitic Network

-20% & +20% capacitance on $C_4$ and $C_5$

$L_s = 50$ pH
$C = 149.74$ pF
$R_i = 905.3$ GΩ

Trapezoidal waveform on the AC pad

$t_{rise} = 50$ ns
$t_{fall} = 50$ ns
$f_{sw} = 2$ kHz
$D = 0.5$
Voltage Distribution in DBC Stack

Parasitic Network

<table>
<thead>
<tr>
<th></th>
<th>E-field @ Measurement Point 1 (kV/mm)</th>
<th>E-field @ Measurement Point 2 (kV/mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Perfect Voltage Distribution</td>
<td>7.368</td>
<td>3</td>
</tr>
<tr>
<td>Voltage distribution for ±20% case</td>
<td>7.368</td>
<td>3.688</td>
</tr>
</tbody>
</table>

-20% & +20% capacitance on $C_4$ and $C_5$
$L_s = 50$ pH
$C = 149.74$ pF
$R_i = 905.3$ GΩ

- The e-field near the TSM triple points is unaffected.
- Only the bulk e-field in the stressed ceramic will be affected.
Capacitance Measurement: Single Layers

- **4 patterned samples**
  - Singulated from a single DBC master card
  - 0.3 mm Cu/ 0.64 mm Al₂O₃/ 0.3 mm Cu

- Measured using Keysight E5061B Network Analyzer

- **< ±2% tolerance in the capacitance for single layer**
  - No voltage clamping is required
  - Avoid drilled vias: a complicated fabrication step
  - Avoid changes in e-field distribution

![Stacked DBC Cavitated Substrate](image_url)

![Capacitance Chart](chart_url)
Capacitance Measurement: Stacks

- Stacked samples
- Measured using Keysight E5061B Network Analyzer

Stacked DBC Cavitated Substrate

<table>
<thead>
<tr>
<th></th>
<th>1+2</th>
<th>3+4</th>
<th>1+2+3</th>
<th>1+2+3+4</th>
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</thead>
<tbody>
<tr>
<td>1 MHz</td>
<td>74.87</td>
<td>76.49</td>
<td>49.91</td>
<td>37.43</td>
</tr>
<tr>
<td>10 MHz</td>
<td>76.54</td>
<td>76.65</td>
<td>53.251</td>
<td>39.415</td>
</tr>
</tbody>
</table>

Calculated Value  Measured Value @ 1 MHz  Measured Value @ 10 MHz
ARL ParaPower

- Co-design-Parametric analysis tool
- Fast run-times (>100x) for analyzing large multi-disciplinary parameter space
- Reasonable accuracy
- Compact 3D thermal resistance and stress network model


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Environmental conditions/ Stress conditions:
- Process temperature: 200 °C
- Initial node temperature: 20 °C
- Power dissipation per die: 200 W
- Convective heat coefficient: 10000 W/m²K

Conclusions:
- Min $T_j$ and E-field mitigation trade-offs
PCM Integration in Cavities

- Phase-change material (PCM) integration in the cavities
  - Mitigate transient loads by passive means
  - Sugar-alcohol based PCMs: Erythritol, Xylitol
  - Transient analysis and power cycling results

Transient analysis results

Power cycling results
Stack and Attach Procedure

Double-sided patterned DBC layers

Screen-printed silver-epoxy on DBCs

Vacuum oven curing:
150 °C/ 1 hour
200 °C/ 1 hour

Final Stacked DBC substrate after epoxy curing

Full stack-up of DBCs in the alignment jig

4 DBCs in the alignment jig
Conclusions:

- More scalability with voltage to a stacked substrate solution
- High voltage isolation
- Reduction in PD due to E-field mitigation
- Simple fabrication
- E-field mitigation and thermal performance trade-offs
- Cavities could be utilized for passive cooling with PCM integration

Future Work:

- DC and AC breakdown tests
- PD inception and extinction voltage tests
- Thermal resistance measurements
- High-voltage breakdown strength nano-particle infused PCMs
Acknowledgement

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Thank You!

Questions?