Significant Developments and Trends in Embedded Substrate and Component Technologies for Power Applications

Presented by

PSMA Packaging Committee

Brian Narveson and Ernie Parker, Co-Chairmen

3D-PEIM

PSMA Power Sources Manufacturers Association
The Multinational Power Electronics Association

PSMA and 3D Power Packaging

- Phase 1 Technology Report " 3D Power Packaging" (authored by Tyndall National Institute) determined the power industry was interested in and beginning to manufacture Embedded Substrate power products (published Feb. 2014)
- Phase 2 Technology Report "Current Developments in 3D Power Packaging with Focus on Embedded Substrate Technology" (authored Ltec Corporation) was published in March 2015, determined power supplies can be made now with embedded technology, but a lot more needs to be done.
  - Researched 740 published articles from industry, government and academia
  - Interviewed 30 Industry and Academic Experts
  - Attended 10 trade shows, conferences and seminars
- Phase 3 Technology report on 3D Power Packaging planned for 2017
- PSMA primary financial sponsor of 3D-PEIM Symposium
- Packaging Committee has sponsored 3 Industry Sessions at APEC on 3D Packaging

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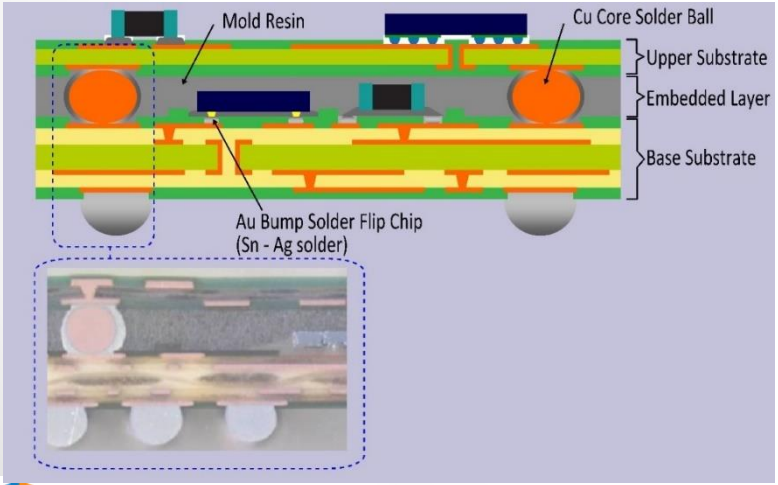
What is 3D Power Packaging

- Power supply products derived from the use of the z axis
- Incorporation of a variety of technologies to reduce footprint
- Solutions that increase power density (W/cm^3)
- Manufacturing solutions that can print or construct interconnects or circuit layers



Embedding Actives or Passives in Substrate

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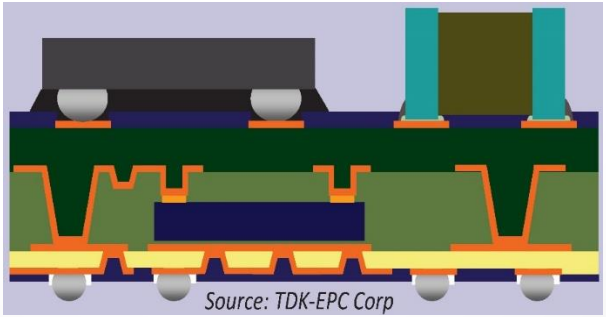
What is Embedded Substrate Technology

- A *3D Embedded Power Module* is a "systems that use a combination of at least one controller/driver IC, at least one active component in the power train, and associated interconnect means, embedded in a single package."
- *Component embedding* is "the inclusion of at least one active or passive electrical component within the top and bottom conductive layers of a substrate."
- A *substrate* is defined for this study as "a planar structure having multiple conductive and insulating layers."

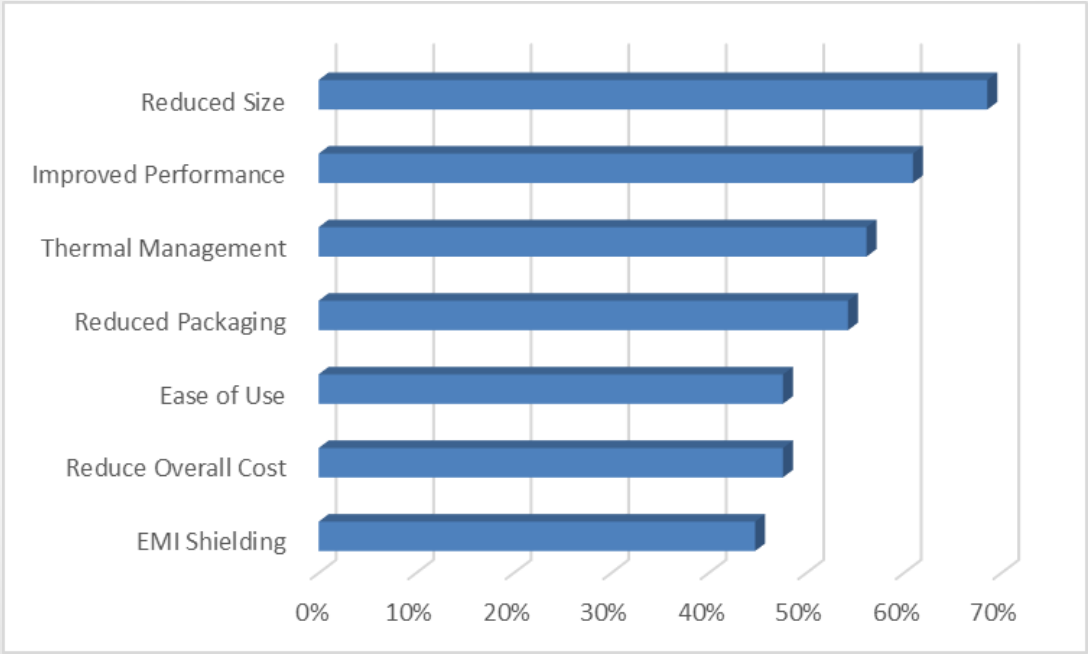


Embedded Power Market Drivers

- Digital functionality and power consumption increasing at a rate of “More than Moore”
  - CMOS has hit the wall, transistor efficiency is not increasing, and processor clock speeds are stagnating.
  - Advanced deep submicron semiconductor technology has hit a cost barrier
  - Barrier overcome with a paradigm shift in digital semiconductor packaging
  - Leading technologies are wafer thinning, through-silicon vias (TSV) and 2.5D and 3D integration
  - Power requirements increasing 2 to 5 times, within the same footprint, in one generation
- Power density and efficiency improvement with wide bandgap gallium-nitride (GaN), silicon-carbide (SiC), and gallium-arsenic (GaAs) are facing a “construction barrier”
  - Optimum performance can only be achieved with packaging free of bond wires
  - Embedded substrate technology is a disruptive technology that can lead to large increases in power density and efficiency, plus higher performance from wide bandgap devices

Why is Embedded 3D Packaging Important

- **What you told us: Motivation for using embedded packaging.**



% of Available Score

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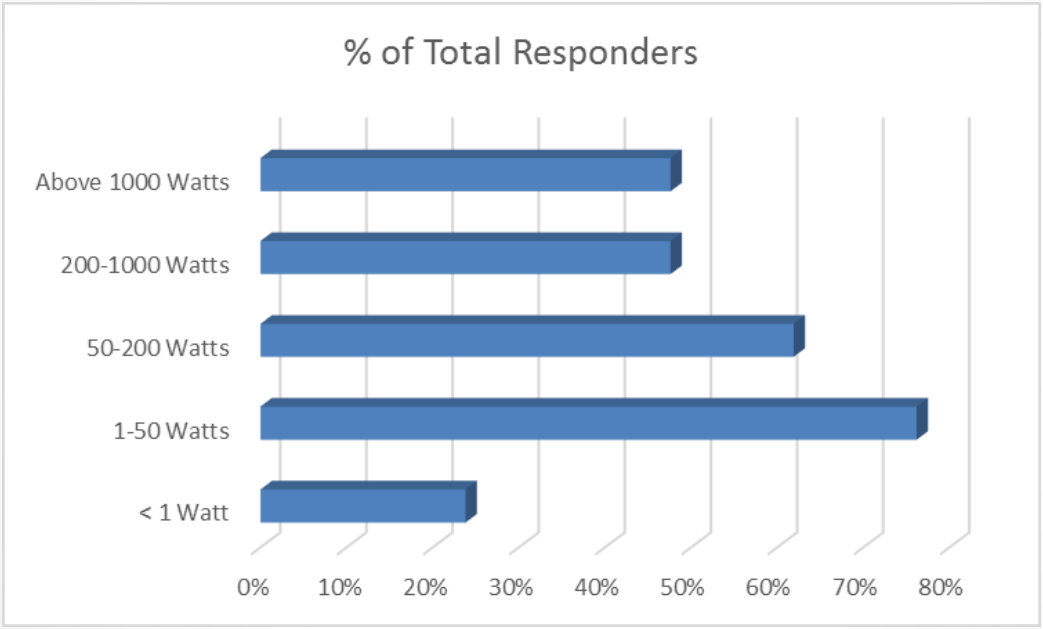
At what Power Levels are you Interested?

- **What you told us:**



Technology Areas Studied

- ***PCB's and Inorganic Substrates***
- ***Semiconductors including High Temperature Die Attach and High-lead Solder Substitution***
- ***Passives***
  - ***Resistors***
  - ***Capacitors***
  - ***Magnetics***
- Interposers
- Packaging Technologies
- Thermal Management
- Additive Manufacturing
- The phase 2 report is 10 Chapters, 335 pages, with 394 Publications cited and 172 links provided

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Benefits of Embedded Substrate Technology

- Performance
- Reliability
- Ease of use
- Solution size
- Thermal management
- EMI shielding
- Reduced need for product-specific tooling
- Reduced need for additional packaging
- Fastp time to market
- **Cost?**

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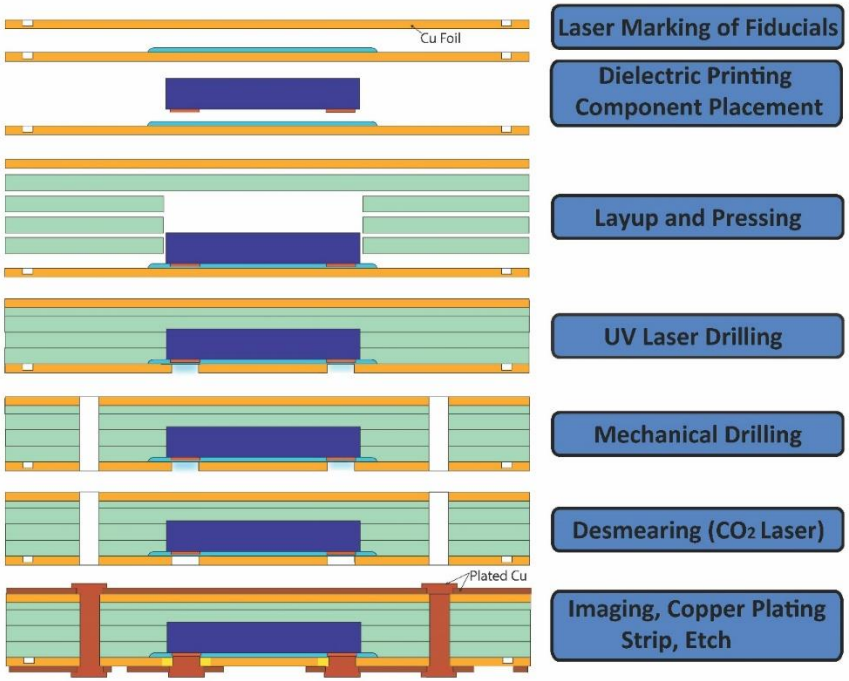
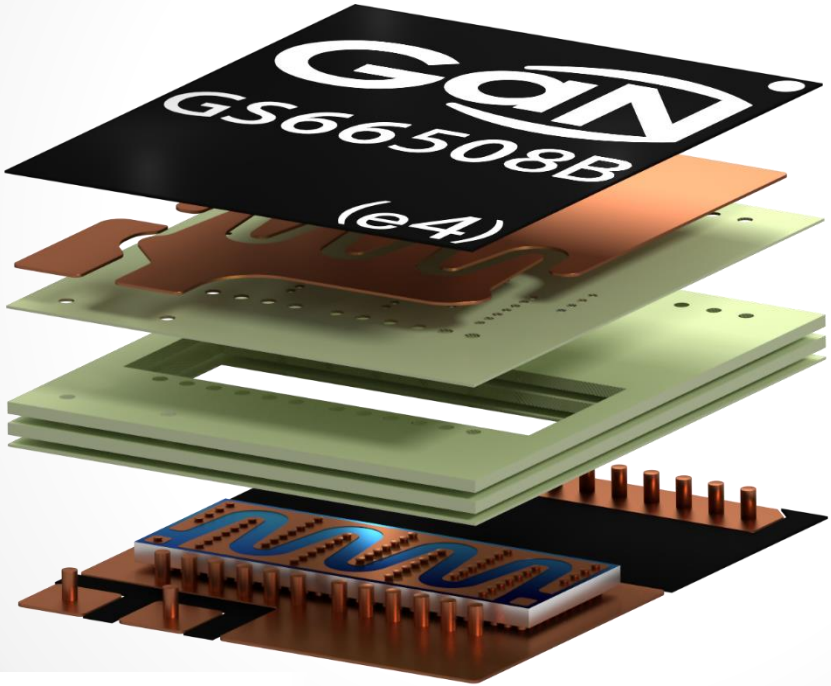
Standards for Embedded Substrate Technology

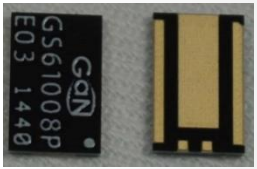
- Substrates and Components
  - **IPC-2316:** Design Guide for Embedded Passive Device Printed Boards
  - **IPC-4811:** Specification for Embedded Passive Device Resistor Materials for Rigid and Multilayer Printed Boards
  - **IPC-4821:** Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards.
  - **IPC-4101:** Specification for Base Materials for Rigid and Multilayer Printed Boards
  - **IPC-6012:** Qualification and Performance Specification for Rigid Printed Boards
  - **IPC-7092:** Design and Assembly Process Implementation for Embedded Components
  - **JCPA – EB01-2013:** Parts Built-in Electronic Circuit Board (Component Built-in Board) Data Format Design Guide – 2nd Edition
  - **JPCA – EB02-2013:** Standard on Device Embedded Substrate Terminology / Reliability / Test / Design Guide 4th Edition

AT&S Embedded Component Packaging (ECP™) Process Flow



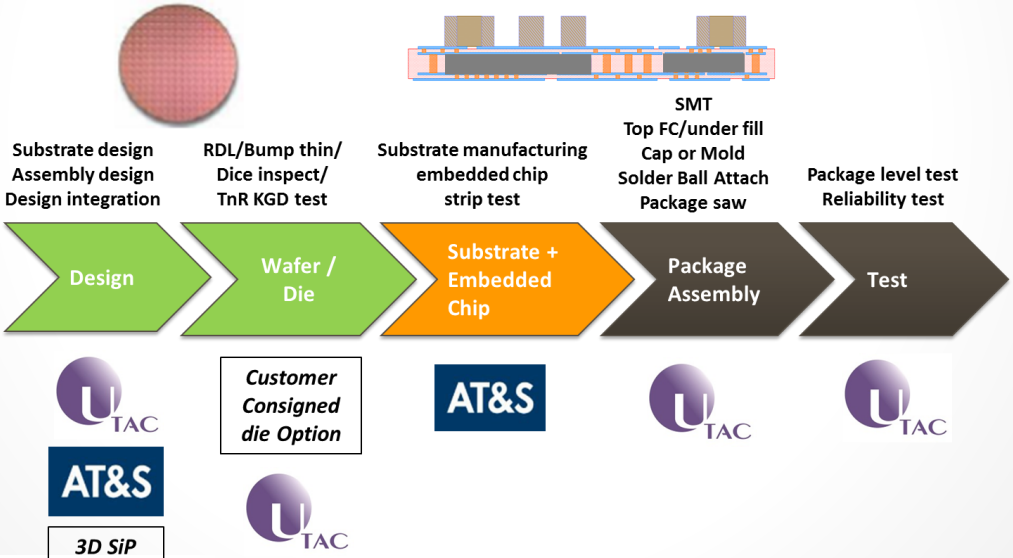
GaN devices of GaN Systems Inc. embedded in AT&S (ECP™) process



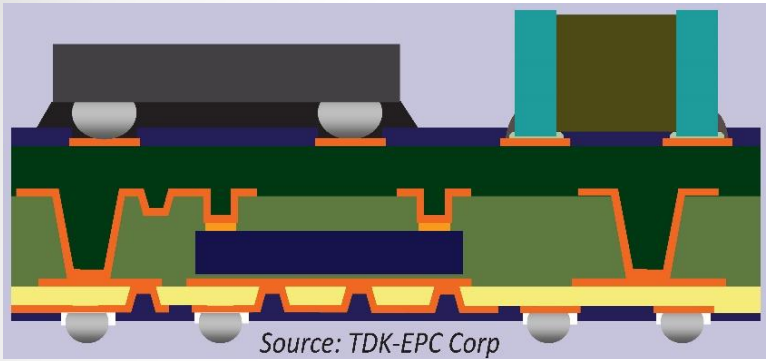


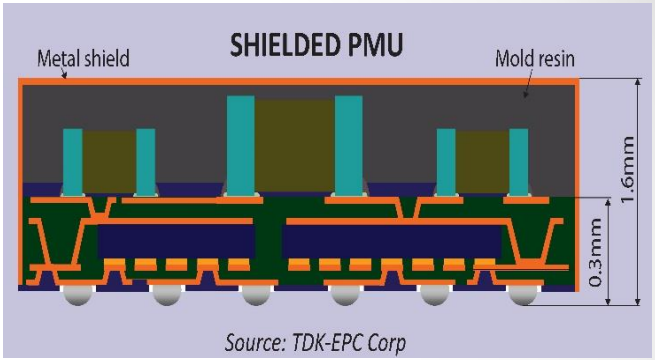
UTAC and AT&S Collaborate on Turnkey Supply Embedded Chip in Substrate Technology

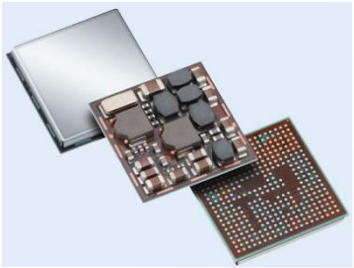
Collaborative 3D SiP Supply Chain Flow



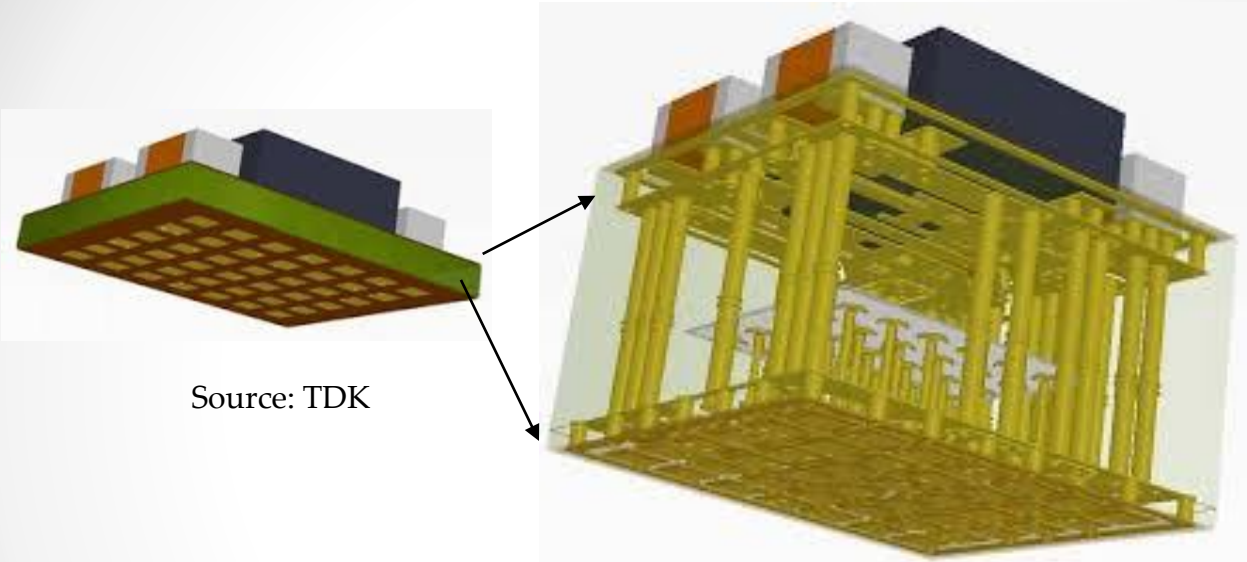
TDK SESUB Process







3D Pattern Routing in SESUB



Source: TDK

-Connection among IC and passives all within the module
-PGND plane can be isolated from other GND plane
-Switching energy can be routed in internal PGND return path
-Switcher noise may be reduced by PGND isolation

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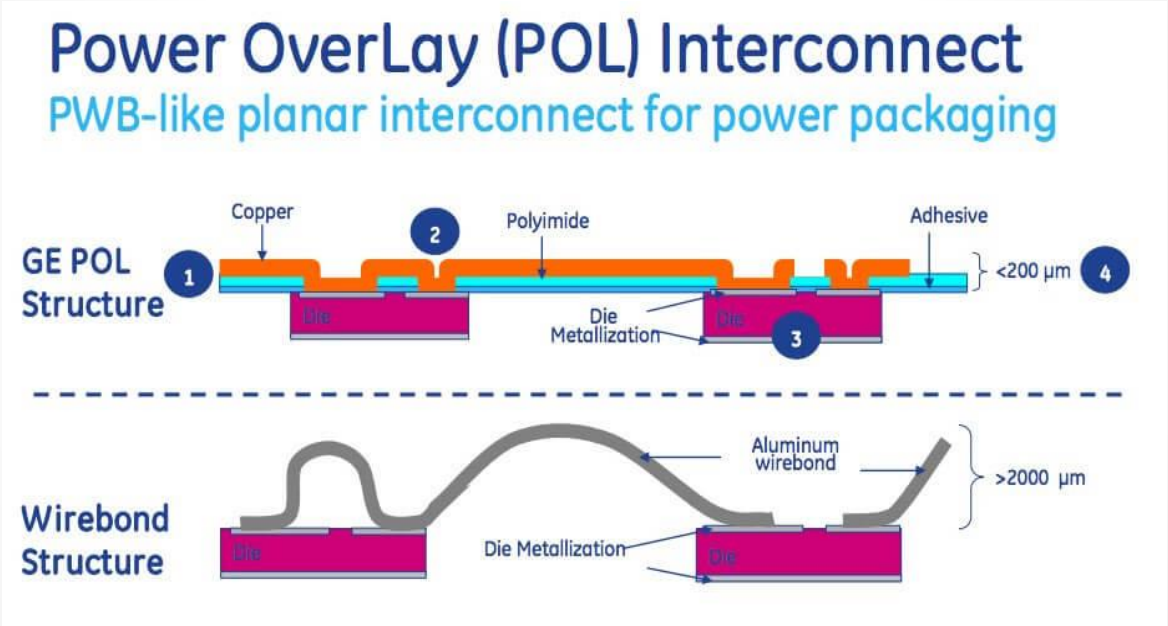
General Electric's Power Overlay Technology



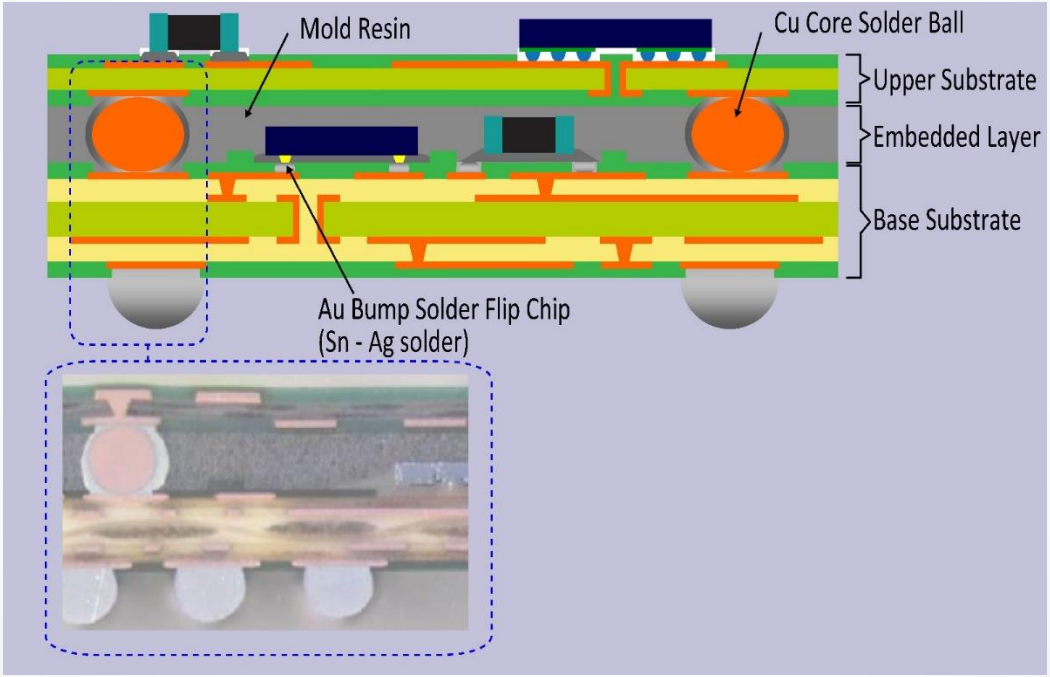

	ePOL	WPOL	POL-MCM	POL-kW
DESCRIPTION	Low-cost embedded package leveraging high volume PCB technologies	Fanout WLP using GE POL and component packaging technologies	MCM SIP & integrated passive SMT or leaded conectors with integrated DBC for thermals	Ultra high power module with leaded connectors and advanced thermal management
FEATURES, BENEFITS	Low I/O <300 single and SIP applications, with min. L/S 25/25um, 30+ Volt	Low to medium I/O, 400 single & MCM applications with min. L/S 10/10um 30+ Volt - Large sized POL frame processing, enabling excellent routing capability - Ultra thin, low	Medium Voltage ,1200V - Multiple pwr devices and ICs (10+) - Multiple passives (30+) - Low parasitics - Heterogeneous die integration combining both power and logic	Higher power 1200V+ - Lowest possible parasitics fast switching, low losses - Double sided cooling, superior thermal management
APPLICATIONS	Mobile, computing, telecom - Wireless - RF FEM - Power management	Mobile, computing, telecom - Wireless - RF FEM - power management	Computing, telecom, industrial - DC-DC converter - Intelligent power modules	Automotive, aerospace, - Motor drives - Renewables - High power conversion

GE licensed its Power Overlay Technology to Shinko Electric in 2015

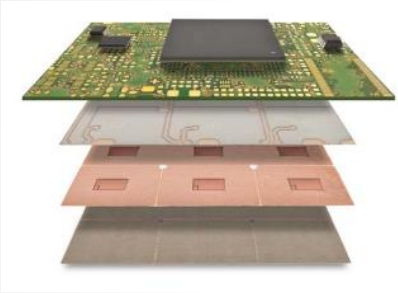


1. Low and Matched Parasitics
2. Eliminate Bond Wires
3. Ability to Array Multiple Die
4. Reduction in Size and Weight

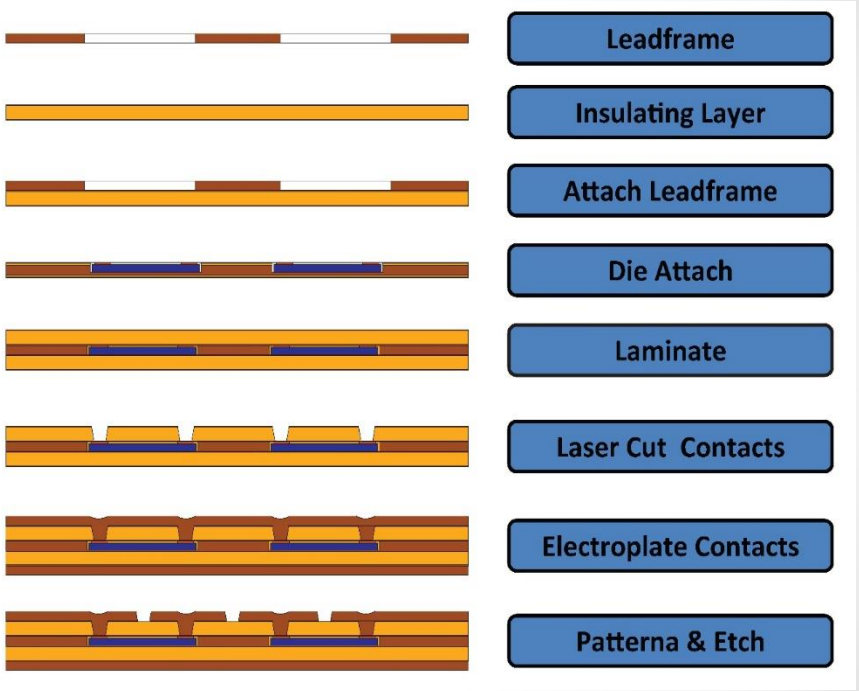
Shinko Electric's Molded Core Embedded Package (MceP®)



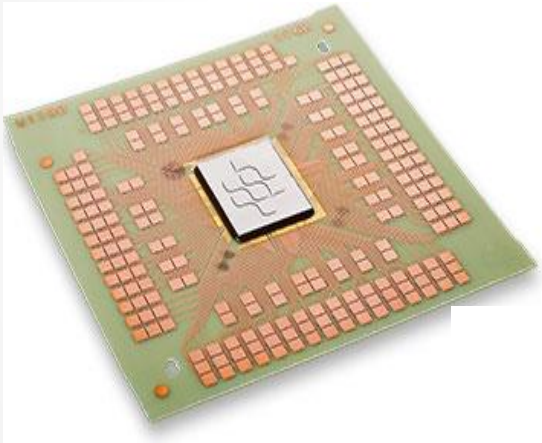
Schweizer's P²-PAK approach



p² Pack® module assembly with logic PCB

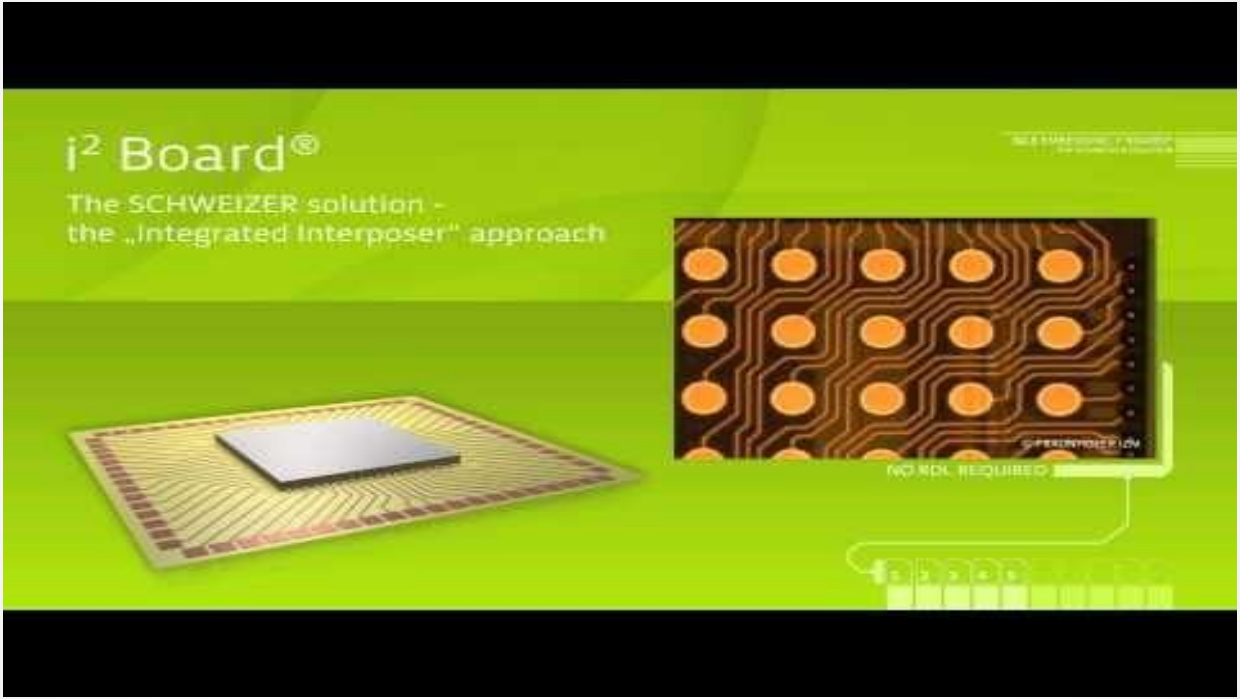


Schweizer's i² Board® approach

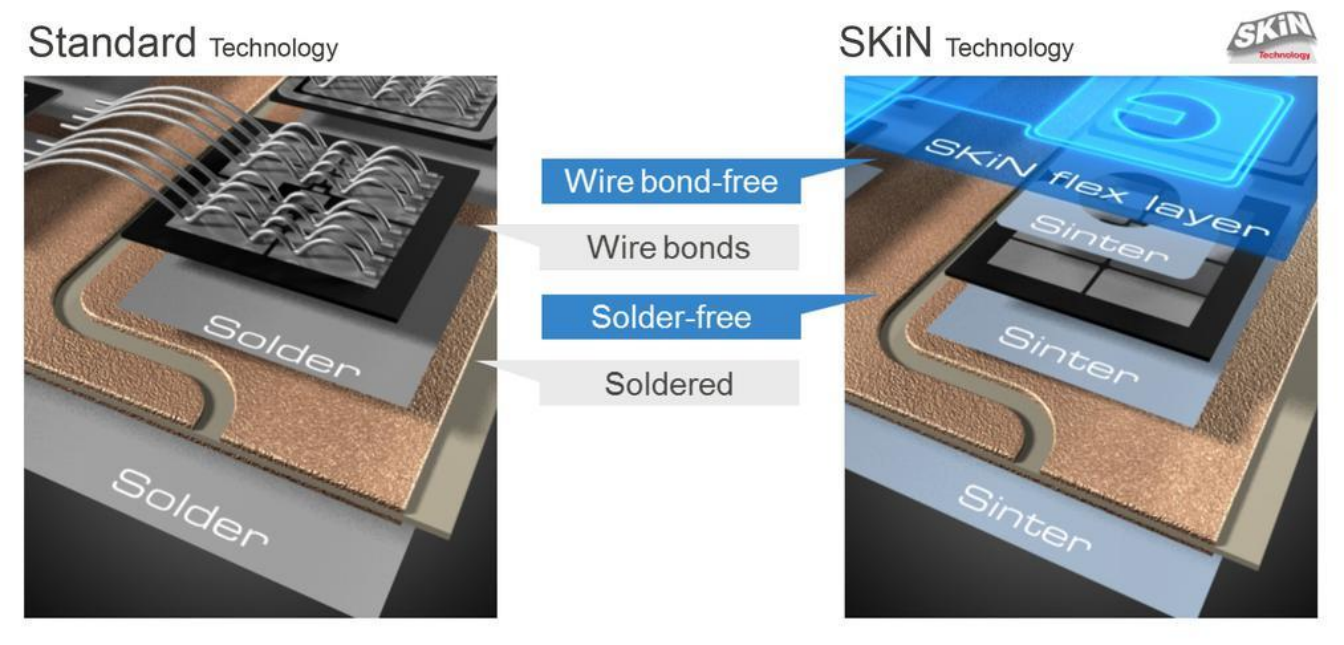


-Design an interposer board for embedding in host PCB
-Interposer can contain both passives and actives
-Conventional surface mount components can be embedded using the interposer

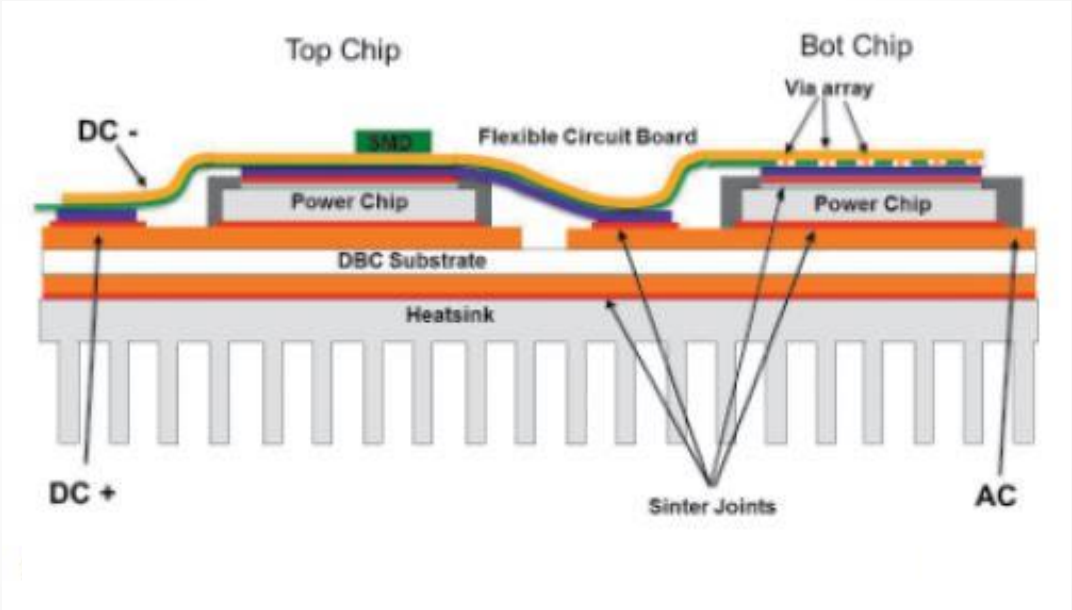
Schweizer's i² Board® approach



Semikron's Sintered SKiN™ Process

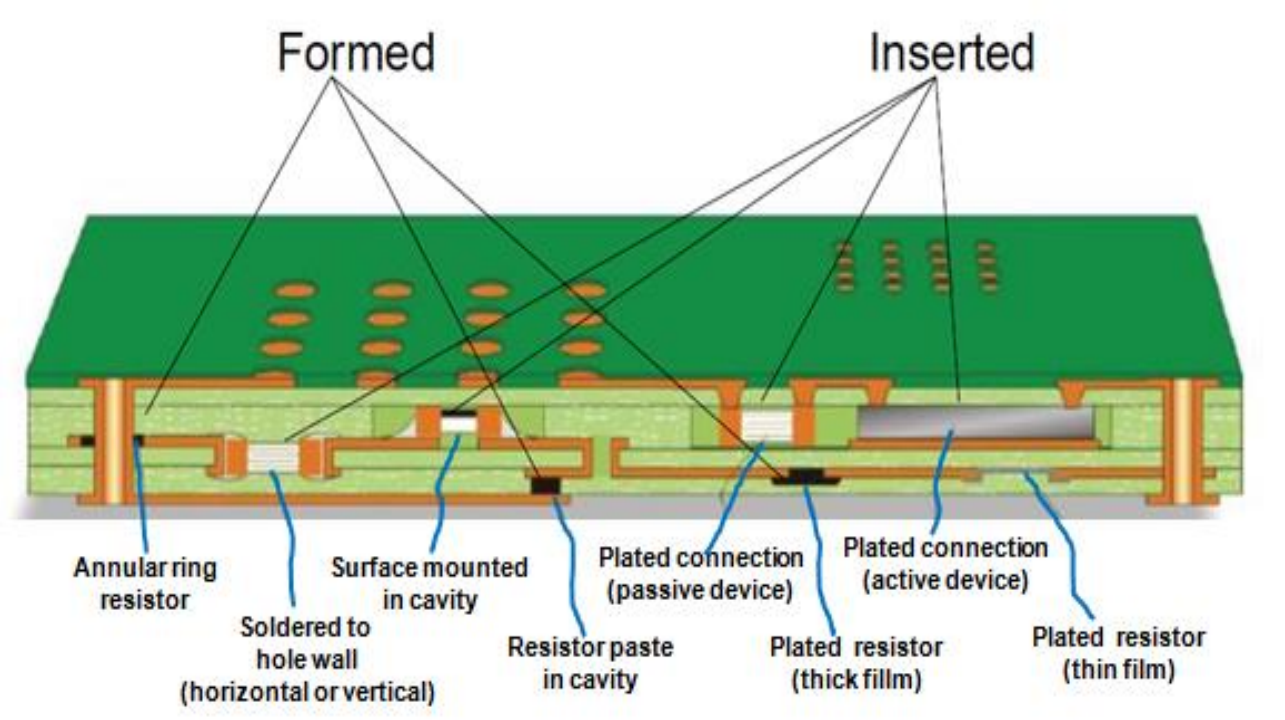


Semikron's Sintered SKiN™ Process



Cross Section of 3D SKiN® Power Module with Sintered Joints

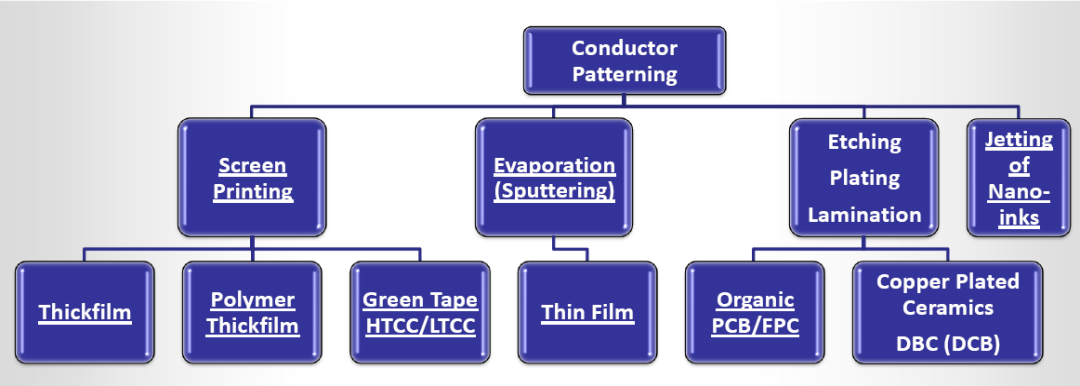
Component Types and Processes



Example of an embedded assembly Source: IPC International Technology Roadmap

Resistors

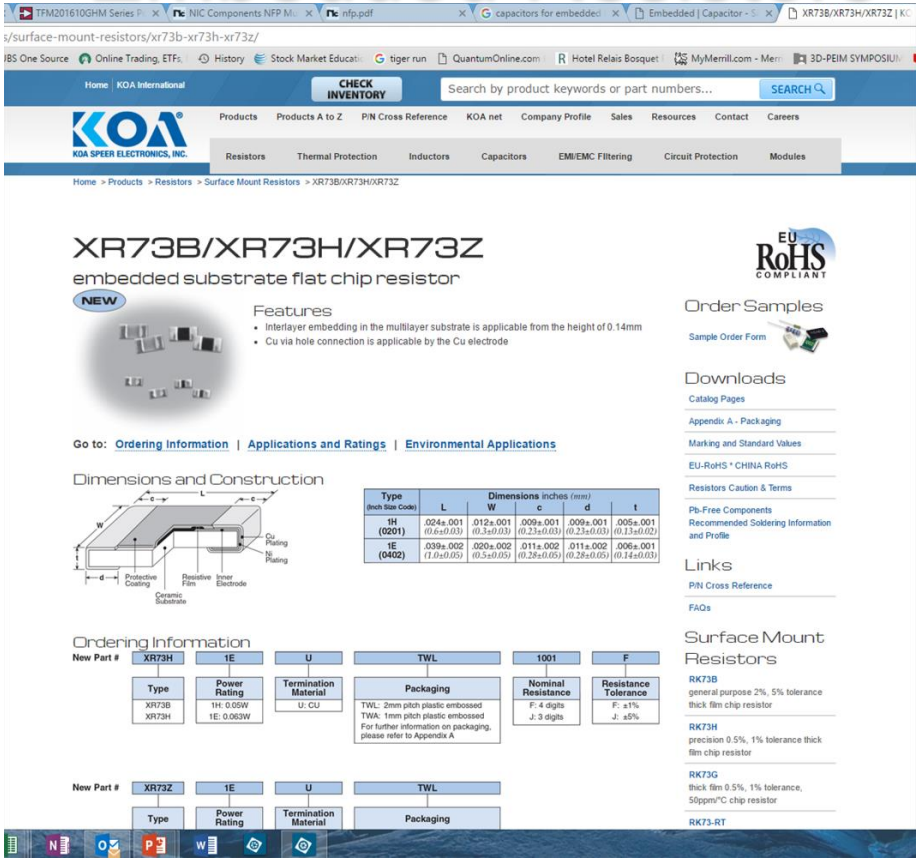
- **Formed Technologies**



Source: Micro Consulting Services

- Inserted-Suppliers of embeddable resistors
  - KOA Speer Electronics, Inc
  - Aeroflex (A Cobham Company)
  - Panasonic
  - Stackpole Electronics, Inc.
  - Vishay Intertechnology, Inc
  - Ohmega Technologies, Inc.

Embedded Resistors



TFM201610GHM Series P | NIC Components NFP Mu | nfp.pdf | capacitors for embedded | Embedded | Capacitor - Si | XR73B/XR73H/XR73Z | KC

s/surface-mount-resistors/xr73b-xr73h-xr73z/

BS One Source | Online Trading, ETFs | History | Stock Market Educati | tiger run | QuantumOnline.com | Hotel Relais Bosquet | MyMerrill.com - Merri | 3D-PEIM SYMPOSIUM

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Resistors | Thermal Protection | Inductors | Capacitors | EMI/EMC Filtering | Circuit Protection | Modules

Home > Products > Resistors > Surface Mount Resistors > XR73B/XR73H/XR73Z

XR73B/XR73H/XR73Z

embedded substrate flat chip resistor

EU RoHS COMPLIANT

NEW

Features

- Interlayer embedding in the multilayer substrate is applicable from the height of 0.14mm
- Cu via hole connection is applicable by the Cu electrode

Go to: Ordering Information | Applications and Ratings | Environmental Applications

Dimensions and Construction

W, L, c, d, t; Cu Plating; Ni Plating; Protective Coating; Resistive Film; Inner Electrode; Ceramic Substrate

Type (Inch Size Code)	Dimensions inches (mm) L	W	c	d	t
1H (0201)	.024±.001 (0.6±0.03)	.012±.001 (0.3±0.03)	.009±.001 (0.23±0.03)	.009±.001 (0.23±0.03)	.005±.001 (0.13±0.02)
1E (0402)	.039±.002 (1.0±0.05)	.020±.002 (0.5±0.05)	.011±.002 (0.28±0.05)	.011±.002 (0.28±0.05)	.006±.001 (0.14±0.03)

Ordering Information

New Part #	XR73H	1E	U	TWL	1001	F
	Type: XR73B, XR73H	Power Rating: 1H: 0.05W, 1E: 0.063W	Termination Material: U: CU	Packaging: TWL: 2mm pitch plastic embossed; TWA: 1mm pitch plastic embossed; For further information on packaging, please refer to Appendix A	Nominal Resistance: F: 4 digits, J: 3 digits	Resistance Tolerance: F: ±1%, J: ±5%

New Part #	XR73Z	1E	U	TWL
	Type	Power Rating	Termination Material	Packaging

Order Samples

Sample Order Form

Downloads

Catalog Pages
Appendix A - Packaging
Marking and Standard Values
EU-RoHS * CHINA RoHS
Resistors Caution & Terms
Pb-Free Components Recommended Soldering Information and Profile

Links

P/N Cross Reference
FAQs

Surface Mount Resistors

RK73B
general purpose 2%, 5% tolerance thick film chip resistor

RK73H
precision 0.5%, 1% tolerance thick film chip resistor

RK73G
thick film 0.5%, 1% tolerance, 50ppm/°C chip resistor

RK73-RT

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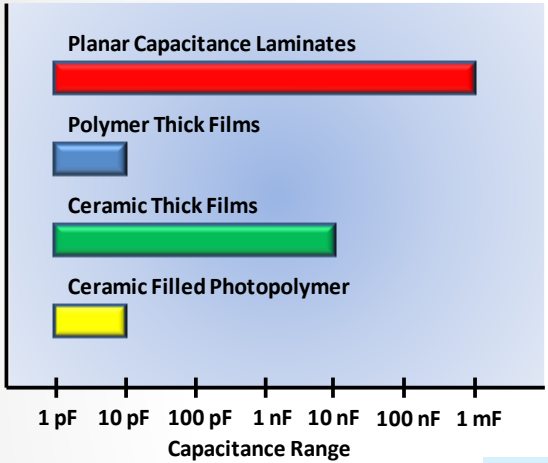
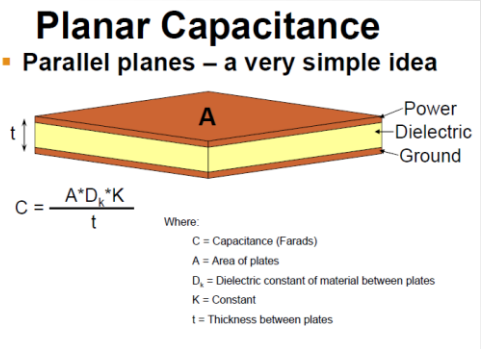
Capacitors

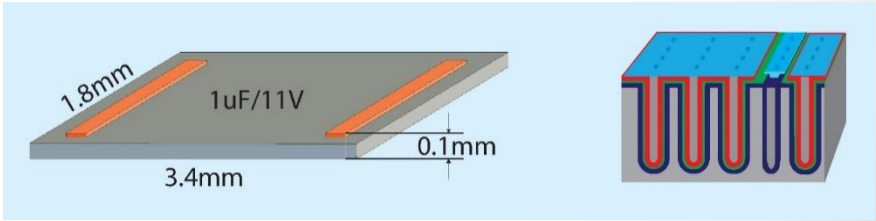
- **Formed Technologies**



Capacitance range for formed capacitor materials Source: IPC-2316



- **Inserted-Suppliers**
  - AVX Corporation
  - Murata Electronics
  - Kemet Corporation
  - IPDiA
  - Taiyo-Yuden Company
  - TDK
  - Samsung



-IPDiA's deep trench silicon capacitor
-Up to 1206 package just .1mm high

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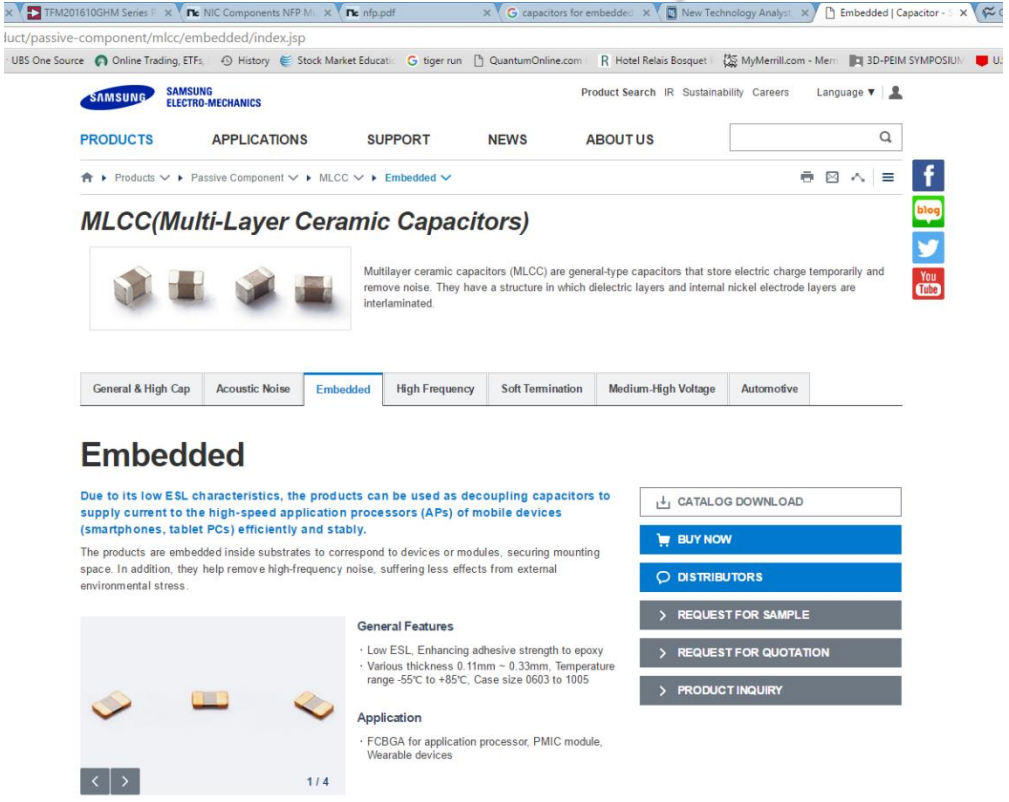
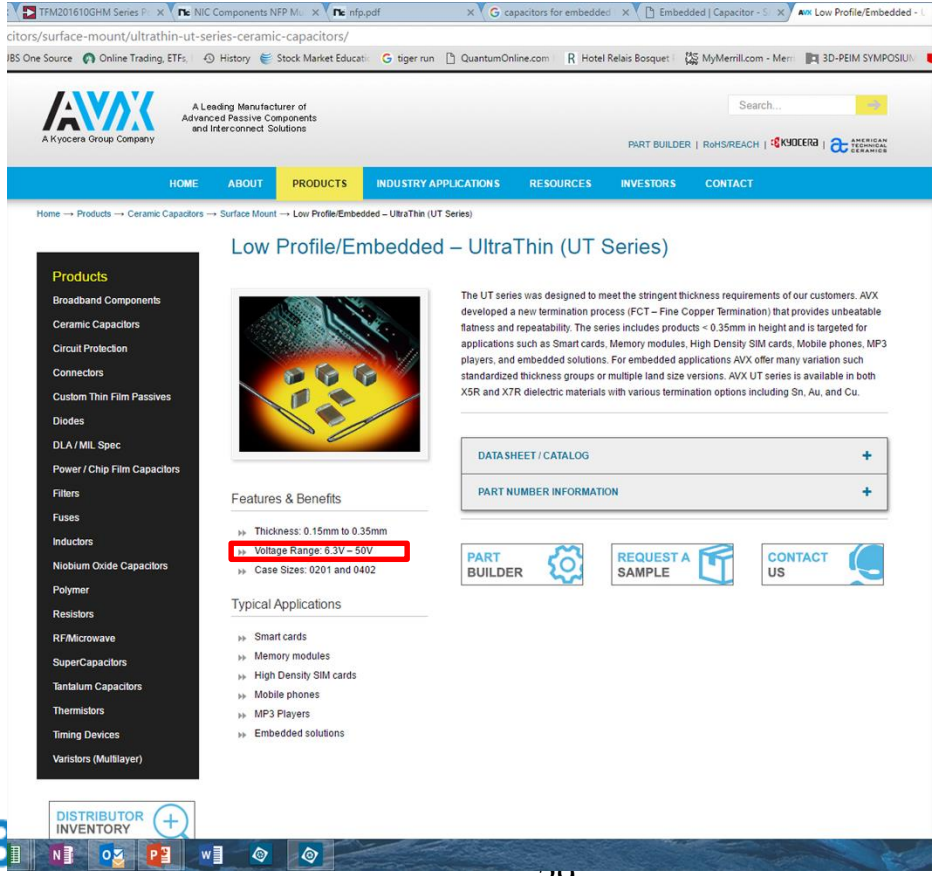
Embedded Capacitors

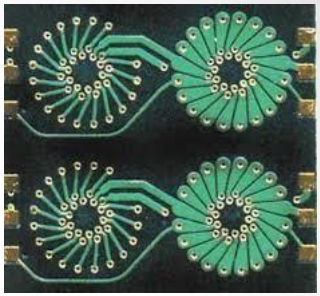


Embedded Capacitors



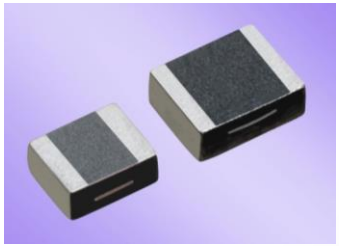
Inductors

- **Formed Technologies**
  - -NEC-Tokin flake magnetic material
  - -Bel Fuse embedded transformers
  - -Planar Magnetics



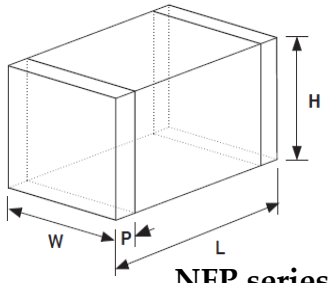
Bel Fuse Internal **embedded** multiple transformer construction

- **Inserted-Suppliers of embeddable inductors**
  - –Taiyo Yuden Co., Ltd
  - –Coilcraft, Inc.
  - –NTI Components Corporation
  - –TDK-EPC
  - –Kemet Electronics, Inc.
  - –KOA Speer Electronics, Inc.
  - –NEC-Token



TDK thin film inductor

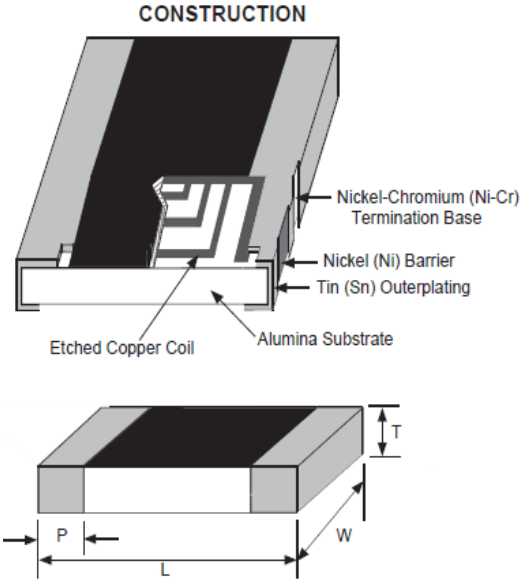
Inductors – Present Devices for Emedding



NFP series inductor outline—
Source: NIC

DIMENSIONS (mm)

Case Size	L	W	H	P
0603	1.6 ± 0.15	0.8 ± 0.15	0.5 ± 0.1	0.3 ± 0.2
			0.8 ± 0.15	
0805	2.0 +0.3/-0.1	1.25 ± 0.2	0.5 ± 0.1	0.5 ± 0.3
			0.9 ± 0.1	
			1.25 ± 0.2	
0806	2.0 +0.3/-0.1	1.6 ± 0.2	0.9 ± 0.1	0.5 ± 0.3
			1.1 ± 0.1	
1008	2.5 ± 0.2	2.0 +0.3/-0.1	0.9 ± 0.1	0.5 ± 0.3
			1.1 ± 0.1	



NTI thin film inductor
construction— Source: NIC

.47µH - 10µH

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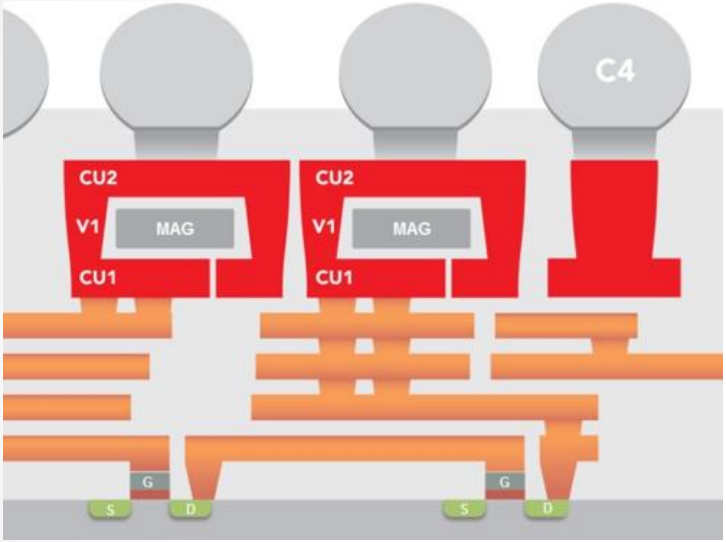
Ferric Inc. Magnetic Core Inductors



-Process and designs are integrated on top of the chip or interposer
- Flexibility in integration and implementation.

Ferric's magnetic core topologies provide
>5A/mm^2 current density and utilization factor near 100%

Challenges

- Electrical Test
- Yield
- Who owns the failure
- How do share the losses
- Passives at rating and values we need

Summary

- The digital world is going 3D to increase capability in the same footprint
- Digital 3D will greatly increase the need for power but not increase the available space to implement it
- Embedded Substrate technology is a viable path to increase power density
- Multiple substrate and semiconductor technologies are available at many power levels
- Both formed and inserted components are available from multiple suppliers
- Multiple power manufactures are shipping product utilizing embedded technology
- Less than 5% of the material in the reports has been presented. Contact PSMA to find out how to get a copy.

Want to Participate or Learn More

- Participate in PSMA Packaging Committee
  - Planning a Phase 3 3D-Packaging Technical Report in 2017
    - Exact content will be discussed this fall
  - Planning 3D Power Packaging Industry session at APEC 2017 in Tampa Florida, March 26-30 2017
    - We are determining topics and recruiting speakers now
  - Discussion of whether to hold another 3D-PEIM.
    - Let us know if you would be interesting in hosting or participating on the organizing or technical committees
  - If you would be interested in participating in committee meetings please contact bcnarveson@gmail.com . (PSMA membership encouraged but not required)

Thank You