Embedding Technologies for Planar Power Electronic Modules

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The Fraunhofer-Gesellschaft

- 66 institutes and research units
- Nearly 24,000 staff
- More than €2 billion annual research budget totaling. Of this sum, around 1.7 billion euros is generated through contract research
Fraunhofer IZM’s Mission:
From Microelectronics and Microsystems towards Smart Systems

System Integration Technologies

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Motivation: Embedding
Embedding for Power
How to make a "perfect" module
Examples
Concept 3D Packaging
Summary
Diversity of Embedded Packaging Technologies (Driver: Fan Out)

Die Embedding in Organic Laminate „Embedded Die”

- Fan-In Type
- Chip-First
- Chip-Last

- ECP (AT&S)
- SESUB (TDK)
- ET Solder, Microvia, Flip-Chip (Wuerth)
- µBoard, µPack, µPack (Schweizer)
- WFOP (Amkor/-Devices)
- BLADE (Infineon)
- eASI (AISE)
- B2D2K, B2DPWB (Da Nippon)
- ChipsetT/Chiplet T 3)
- ECOM (Tokyo Yuden)
- Clover embedded device (Unimicron)
- MCP (Shinko)
- EWLP/3P (Imbera)
- FoWLP LS (Semco)

Die Embedding in Epoxy Moldcompound „Fan-Out WLPIPLP“

- Fan-In Type
- Chip-First
- Chip-Last

- EMAP (GT Pro) 2.5D Cl. (AT&S)
- WLCSP+ (Amkor/NANJU) eWLCSP (JCEC STATS ChipPAC)
- KCP (2)
- nLP (Nepes)
- FOWLP (SPL)
- CHIEFS (PTI)

Face-Down Assembly

- M-Serien (DECA)
- InFO (TSMC)
- ADL (Sinochip, Nantong Fujitsu)
- NTI (SPL)
- FOWWP (Samsung)
- Pie Chip Middle ePK (PTI)

Technology Fusion

- EMIB Si-Bridge (Intel)
- HiSTI CMI (GT int3Dsystems)

Die Embedding in Inorganic Materials „Enlarged Die“

- Fan-In Type
- Chip-First
- Chip-Last

- NA
- eWLB 1)
- eWLP (ASE)
- WLOF (Amkor/NANJU)
- KCP (2)
- nLP (Nepes)
- FOWLP (SPL)
- CHIEFS (PTI)

Face-Up Assembly

- M-Serien (DECA)
- InFO (TSMC)
- ADL (Sinochip, Nantong Fujitsu)
- NTI (SPL)
- FOWWP (Samsung)
- Pie Chip Middle ePK (PTI)

Those solutions can be categorized as Advanced FlipChip Technologies:

- FOCLP (ASE)
- LCCSP (Amkor)
- SWIFT (Amkor)
- SLM (Amkor)
- RDL-First (IME)
- InFO PoP (TSMC)
- SLF (Xilinx, SPL)

In Glass

- NA
- Mold-free FOWLP (MAXIM)
- eSiFO (TSHT)

In Silicon

- NA
- INFOL (GT Pro)

Mainstream – black
Exceptions – brown
Examples – blue
1) Infineon, JCEC STATS ChipPAC, ST Micro
2) Motorola/Freescale/NXP/Qualcomm, Nepes
3) Flipchip International/TSHT, Fujikura

Source: Steffen Kroehnert
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Power Packaging – Established Technology

- power chips soldered to DCB substrate
- top side connection by heavy Al wire bonds

Issues
- limits in miniaturization of packages
- only two wiring layers in modules (DCB + Bond wires)
- lifetime limitation by bond wire reliability
- high inductance of wires → too high for fast switching SiC and GaN chips

There is a need for improvement

EVOLUTION OF POWER ELECTRONICS LANDSCAPE
Evolution of business models?

- Power module manufacturing is an area of tough competition: module-only manufacturers must develop high performance products to stay competitive.
- Additionally, more and more car makers are willing to venture into the market at inverter level to differentiate themselves from competitors.
**Power Chip Embedding - Concept**

Integration of components into organic substrate structures

- Al wire bonded IGBT on DCB
- embedded MOSFET

**Power Embedding - Features**

- Completely planar conductors
  - multiple wiring layers possible
  - SMD assembly on top allows driver integration
  - top side cooling possible
  - **very low parasitic effects**
- Direct connection by Cu conductors / no bond wires
  - high reliability by direct Cu to chip interconnects
  - shielding capability
- Embedding of power chips into Printed Circuit Board structures
  - cost saving by large area process ➔ Panel Level Packaging
**Power Chip Embedding – Manufacturing Process**

- backside contact by conductive die bond
  - conductive adhesive
  - soldering
  - sintering
- very good thermal conductivity
- die attach on thick Cu possible
- compatible to standard Ag backside

- Ag sintered die bond

**current challenges**
- availability of Cu bumps on thin power chips
- precise die bonding of large chips

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**IZM Panel Level Embedding Line**
from Wafer Scale to Panel Scale 610 x 456 mm²/24”x18”

- Placement → Accuracy → Molding → Lamination → Laser Drilling

  - **Datacon evo2200/ASM Siplace CA3**
  - **Mahr OMS 600/IMPEX proX3**
  - **WL:** Towa up to 8”
  - **PL:** APIC up to 18”x24” incl. 12” WL
  - **Lauffer/Bürkle**
  - **Siemens Microbeam/Schmoll Picodrill with HYPER RAPID 50**

- Mech. Drilling → Sputter → Cu Plating → Imaging → Etching

  - **Schmoll MX1**
  - **CREAMET 600 CI 2 S3**
  - **Ramgraber automatic plating line**
  - **Orbotech Paragon Ultra 200**
  - **Schmid**
Application – Infineon Blade Technology

SMD power package
- embedded Si MOSFET / Driver
- manufacturing on PCB format

Products - Today's Embedded Power Packages and Modules

The production of embedded packages is ramping up fast

Smart Phone Market
- DC/DC converters
- Power management units
- Connectivity module

Computer market
- MOSFET packages
- Driver MOS SiPs

PCB Embedding Technology is implemented or will come soon at
- PCB manufacturers
- Semiconductor manufacturers
- OSATS

Schweizer, SEMCO, Thai Nippon, Unimicron/Subtron, …
Challenge Material: Material Selection – Embedded Die Technology

Example: Laminate material
- Two different materials investigated:
  - Low filled RCC (resin coated Cu)
  - Highly filled prepreg material

Findings:
- Clear differences after application relevant stress tests (TC -55 °C/160 °C, HTS 150 °C)
- Prepreg material nearly unchanged after stress, degradation of the RCC material seen
  - Cracks from corners of the redistribution layer towards the chip surface
  - Severe discoloration

Conclusion:
- Lower CTE of filled material strongly reduces the intrinsic stress within material
- Glass fibers can stop an initiated crack before it reaches the chip surface
- Temperature-stable materials are required

Material selection is crucial
High quality materials required

Last 10 years: all package materials changed
Next 10 years: package material change will continue

Power Chip Embedding – Product Types

Power Package
- single chip package
- low thermal & electrical resistance
  ➔ first products available

Power System-in-Package (SiP)
- more chips in one package
- low thermal & electrical resistance
  ➔ first products available

Power Module
- electrical isolation to cooler
- multiple wiring layers
- integration of driver / controller
  ➔ R&D activities
**Power Embedding** – Project Very Fast Switching

Parasitic effects in power packaging

$L_s$ generates negative source feedback
- reduced switching speed
- increased switching losses

$L_g$ increases gate impedance
- risk of oscillations
- risk of parasitic switching

How to make a "perfect" module with strongly reduced parasitics?

(embedded SiC MOSFETS)
Power Embedding – Project Very Fast Switching

How to make a "perfect" module with strongly reduced parasitics?

One SiC MOSFET of the half-bridge is flipped
- out potential on upper Cu layer
- strong reduction of ground coupling

Power Embedding – Project Very Fast Switching

How to make a "perfect" module with strongly reduced parasitics?

Primary DC link capacitors on top of MOSFETs
- reduction of stray inductance
Gate booster close to MOSFETs
- fast switching without parasitic turn-on
Power Embedding – Project Very Fast Switching

Results

- Double pulse test 50 A, 512 V
- 100,000 active power cycles, 20 – 120 °C without defect

Power Embedding – Features

Direct Cu interconnects to chip ➔ High reliability
- Cooling/heat spreading on top ➔ reduced thermal resistance
- SMDs on top ➔ low inductance contact to driver or primary DC link capacitor
- Multiple planar wiring layers ➔ very low inductance
- Polymer laminates ➔ Manufacturing on large panel formats

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### Power Embedding – Potential Configurations

- **3 Phase Motor Inverter**
  - 600V, 200A
  - laminate insulator

- **Solar Inverter**
  - 900 V
  - ceramic insulator

- **Diode Package**
  - double side plated Cu connections

- **50 kW Motor Inverter**
  - Ag sintered bus bars
  - double side cooling

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### Project HI-LEVEL – Targets

Development of planar power modules for 50 kW motor inverter

**Features**

- Reduction of height by 10 mm
- Cost efficient production without expensive packaging
- Integration of control electronics
- Capability for double-side (water) cooling
Project HI-LEVEL – Packaging Construction

Cu pad metallization

laser-drilled and Cu-filled micro-via

400 µm Cu Ag sintered die bond high Tg (185°C)
dielectric high λ dielectric (2 W/mK)

Topics of current investigations
• pressure-less / low-pressure sintering on large panels
• application of 5 µm Cu bumps on thin IGBT wafers
• high voltage isolation of thermally conductive dielectric

Project HI-LEVEL – 50 kW Module

- three phases, 20 – 660 VAC
- 18 IGBTs 200 A
- 18 freewheeling diodes
- DC link < 30 nH expected

press-fit connectors control board

embedded module

frame

heat sink

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Project HI-LEVEL – Embedding vs. Standard DCB

The European EmPower Project
**500 W Demonstrator – Concept**

Embedded-logic Module ILFA

SMD-logic Module ILFA

Passives soldered on Power Core Continental

IMS Top ILFA

MOSFETs ST

Cu Inlays AT&S

Solder process → Conti

Demonstrator-Assembly → Conti

Cu Inlay & MOSFET-Embedding → AT&S

IMS-Sintering → TU Berlin

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**Sinter/Lamination Interconnection – Cross Section**

cross section of IMS/power core/IMS sinter interconnects

sinter connection die area

sinter connection copper inlay area

⇒ no large voids in Ag sinter interconnects

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Sinter Interconnects – X-Ray Inspection

X-ray of sintered top IMS / PowerCore / bottom IMS

➤ good alignment (± 50 µm) of all sintered layers

Concept 3D Stacking

What is a 3D Power Stack?
• Stacking of Functional Layers by combined sinter/lamination technology

controller  driver  I/O

cooler

controller  driver  I/O

cooler

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**Concept 3D Stacking**

**Stacking by combined sinter/lamination ➔ Process Flow**

- Stacking of Functional Layers by combined sinter/lamination technology

1. stencil printing of Ag sinter paste on Functional Layer, paste drying
   ![Image](image1)

2. lay-up of prepreg sheet with opening for paste locations
   ![Image](image2)

3. lay-up of 2. Functional Layer on top, vacuum lamination at 3 MPa, 10 min./230 °C, 60 min./200 °C
   ![Image](image3)

Result: a monolithic stack, thermally and electrically interconnected by high-reliable Ag joints, all gaps are filled by an isolating dielectric

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**Sinter/Lamination Interconnection – FIB Analysis**

- sufficiently low amount of micro voids in sintered Ag (< 30 %)

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**Power Embedding** – Production and R&D

![Graph showing current and voltage with various data points and labels](image)

**Future Perspective** – First a Look Back ...

- **first vacuum tube diode 1908**
- **first transistor 1947**
- **first integrated circuits 1961**
- **Si wafers up to 300 mm**

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Eelectronics Era | Semiconductör Era | Moore’s Law Era
---|---|---
single device manufacturing | highly parallel manufacturing

→ introduction of planar semiconductor technology initiated „Moore’s Law Era“
Future Perspective – Power Electronics Packaging

wire-bonded power chips on DCB

planar module with embedded power chips

Traditional Power modules

Planar Power Packaging

single module manufacturing

large panel manufacturing

- low inductance
- high heat transfer
- high integration level
- high productivity

Thank You