Silver Sintering for Electric Drive Train

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Player across Electronics Value Chain
Global Footprint
Established in every region

Topics

• EV Targets & Approaches
• Die Attach & Silver Sintering
  – Junction Temperature & Thermal Resistance
• Fully Sintered vs Soldered IGBT STO247 - Power Cycling Study
• Silver Sintering in EV Drive Train
EV Targets

How do we get there?

- Module / Inverter Design
  - Higher Power Density
  - Lower loss (Low Parasitics)

- SiC – WBG Semiconductor
  - Cost
  - Packaging for high thermal reliability and low inductance
Power Package – Simple Schematic

3 Levels of Attachment

Solder vs Sintering

- High Thermal
- No Inter-Metallics (20-30X Reliability)

Sintered Interconnects in EV Drivetrain

1. Convey Power
   - Enable High Power Density
   - Reduce thermal resistance & Inductance
   (Lower $/KW, Longer Km Range)

2. Remove Heat
   - Module High Temp Stability
   - Mitigate CTE Mismatch Stress
   - Lower Warranty $ & Longer lifetime

3. Join & Mitigate Stress

Performance + Reliability
Power Device Thermal Resistance

Thermal Resistance Stack from Junction to Ambient

\[ R_{th} = \Delta T/P = (T_{j_{\text{max}}} - T_{\text{amb}})/P = d/\lambda \cdot A \]

Package has smaller area & heat capacity => bottleneck for thermal dissipation
Junction Temperature ($T_j$) Measurement

\[ T_j = \frac{V_{\text{steady}} - V_{\text{transient}}}{k_v} + T_{\text{ambient}} \]

LED Current Switching

LED Thermal Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thermal Conductivity ($W/m \cdot K$)</th>
<th>Layer Thickness (µm)</th>
<th>Cross-sectional Area ($m^2$)</th>
<th>Thermal Resistance $R_{th}(K/W)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED</td>
<td>149</td>
<td>175</td>
<td>$10^{-6}$</td>
<td>1.17</td>
</tr>
<tr>
<td>Die Attach Layer</td>
<td>10 - 250</td>
<td>50</td>
<td>$10^{-6}$</td>
<td>5 - 0.2</td>
</tr>
<tr>
<td>Dielectric (optional)</td>
<td>2.4</td>
<td>25 - 75</td>
<td>$10^{-6}$</td>
<td>10.4 – 31.3</td>
</tr>
<tr>
<td>MCPCB (Cu)</td>
<td>390</td>
<td>1200</td>
<td>$10^{-4}$</td>
<td>0.03</td>
</tr>
<tr>
<td>TIM (Indium)</td>
<td>82</td>
<td>200</td>
<td>$10^{-4}$</td>
<td>0.02</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Die Attach Material</th>
<th>Thermal Conductivity ($W/m \cdot K$)</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>SnBi Solder</td>
<td>20</td>
<td>Low temperature assembly</td>
</tr>
<tr>
<td>80Au/20Sn</td>
<td>57</td>
<td>High reliability</td>
</tr>
<tr>
<td>SAC305 Solder</td>
<td>64</td>
<td>Inexpensive</td>
</tr>
<tr>
<td>Silver Filled Epoxy</td>
<td>149</td>
<td>Electrical insulator, High thermal conductivity</td>
</tr>
<tr>
<td>Sintered Silver</td>
<td>100-250</td>
<td>Electrical conductor, High thermal conductivity</td>
</tr>
</tbody>
</table>
Thermal Resistance Contributions

<table>
<thead>
<tr>
<th></th>
<th>Dielectric</th>
<th>No Dielectric</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Solder</td>
<td>Sintered Ag</td>
</tr>
<tr>
<td></td>
<td>Rth %</td>
<td>Rth %</td>
</tr>
<tr>
<td><strong>Layer Thickness (um)</strong></td>
<td>1x10⁻⁶</td>
<td></td>
</tr>
<tr>
<td><strong>Cross Sectional Area (m²)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Solder</strong></td>
<td>1.2</td>
<td>2.6%</td>
</tr>
<tr>
<td><strong>Sintered Ag</strong></td>
<td>1.2</td>
<td>21%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>2.4</td>
<td>87%</td>
</tr>
<tr>
<td><strong>Substrate (Cu)</strong></td>
<td>390</td>
<td>0.08%</td>
</tr>
<tr>
<td><strong>TIM (Indium)</strong></td>
<td>81.8</td>
<td>0.06%</td>
</tr>
<tr>
<td><strong>Remnant Rth</strong></td>
<td>3.3</td>
<td>7.3%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>45 K/W</td>
<td>43 K/W</td>
</tr>
</tbody>
</table>

A dielectric layer makes measuring die attach bulk thermal resistances difficult

Fast LED Transients

- When the dielectric layer is removed:
  - The experiment doesn’t need to be as precise
  - Voltage measurements must be faster
  - Current stabilization within 30 us versus ms

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Sintered Silver vs SAC305 Solder Tj

- ~20°C lower Tj with Sintered Silver
- Able to sustain high currents at lower forward voltage without failure
- >7W power through 1mm²

Die Attach Materials Comparison

<table>
<thead>
<tr>
<th>Normalized Tj at 3 Watts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder (SAC305)</td>
</tr>
<tr>
<td>Sintered Ag A</td>
</tr>
<tr>
<td>Silver Filled Epoxy</td>
</tr>
<tr>
<td>Sintered Ag B</td>
</tr>
</tbody>
</table>
Thermal Resistance & Design

Real Life Example

Example - IGBT IKNW75N60T

- Power Dissipation = 428W
- $R_{th} = 0.35\text{K/W}$
- $T_{jmax} = 175^\circ\text{C}$ ($R_{th} \times \text{Power} + 25^\circ\text{C}$ margin)
- 15% lower $R_{th}$ with sintered silver reduced $T_j$ by $\sim 25^\circ\text{C}$

- Allow peak current with die area (less $$)
- OR higher reliability at peak current
- OR higher peak current for higher performance

Why Lower Package $R_{th}$?
- Enables higher current density (less die area)
- Enables higher efficiency (by lowering $T_j$)
- Lower Impedance / $R_{th}$ reduces temperature swings at high loads -> longer lifetime

A Simple Comparison - Sintered vs Soldered TO247
Solder vs Sintering – A Comparison

• Problem: Develop the highest power density Silicon based TO247 package

• Approach: Sinter both top and bottom contacts using silver sintered film to Cu lead frame and clip

Comparison to Standard Technology

Double Side Silver Sintered

200 A Package

15.3 x 19.79 mm

Soldered and Wire Bonded

130 A Package

15.10 x 19.80 mm
Package Cross Section

Soldered and wire bonded

Double side sintered

Wire bonding
Soldered IGBT
Soldered Diode
Cu Tab
Mold compound

Top connection sintered
Sintered Diode Sintered IGBT
Cu Tab
Mold compound

Power Cycling Test

- Mentor Graphics MicReD 1500A Power Test Setup
  - 15s on/15s off, Fixed Current and Gate Voltage
  - Failure Criteria: 10% increase in thermal resistance, $V_{CE}$ or $T_{j}$ max

<table>
<thead>
<tr>
<th>Component</th>
<th>Current (A)</th>
<th>Delta T [°C]</th>
<th>Cycles to Failure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard TO247</td>
<td>130</td>
<td>85</td>
<td>12K</td>
</tr>
<tr>
<td>Double Sintered TO247</td>
<td>200</td>
<td>85</td>
<td>150K*</td>
</tr>
<tr>
<td></td>
<td>200</td>
<td>110</td>
<td>350K*</td>
</tr>
</tbody>
</table>

~30X cycles without failure (over solder)
Thermal Resistance Decreases

Double Sided Sintered Package

Effect on Sintered Silver Microstructure

- Coarsening over Power Cycling & Thermal Cycling
- Increasing density around interfaces
Fully Sintered STO247 - Stray Inductance

Stray Inductances => transient voltages at switching events

- Less losses during switching
- Support higher voltage battery
- Safer operation even at higher frequency operation

So how does it translate to EV

- 30-40% higher efficiency (Miles/KW-Kg)
  - Eliminated parasitics
  - Higher power density (with stable $T_j$)

- > 30X lifetime (lower warranty cost – eliminated major failure modes)
  - No wire bond lift-off
  - No inter-metallics
SiC based EV Traction Inverter

SiC is Wide Band Gap Device

- Higher Efficiency
  - Lower Switching loss
- Supports Higher Temperature Operation
  - Less thermal management need
- Ideal for higher switching (>10KHz)
- Higher voltage operation (at thinner die)
  - Reduced losses

Silver Sintering critical for managing both issues!

SiC Yield is an issue – smaller dies – higher Rth

Must manage dV/dT (voltage transients from stray inductance)

Thanks!

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