

**PwrSiP**  
**Power Supply in Package**  
**Power System in Package**

**Prof. Cian O'Mathuna, FIEEE**  
**Tyndall National Institute**  
**University College Cork,**  
**Ireland**

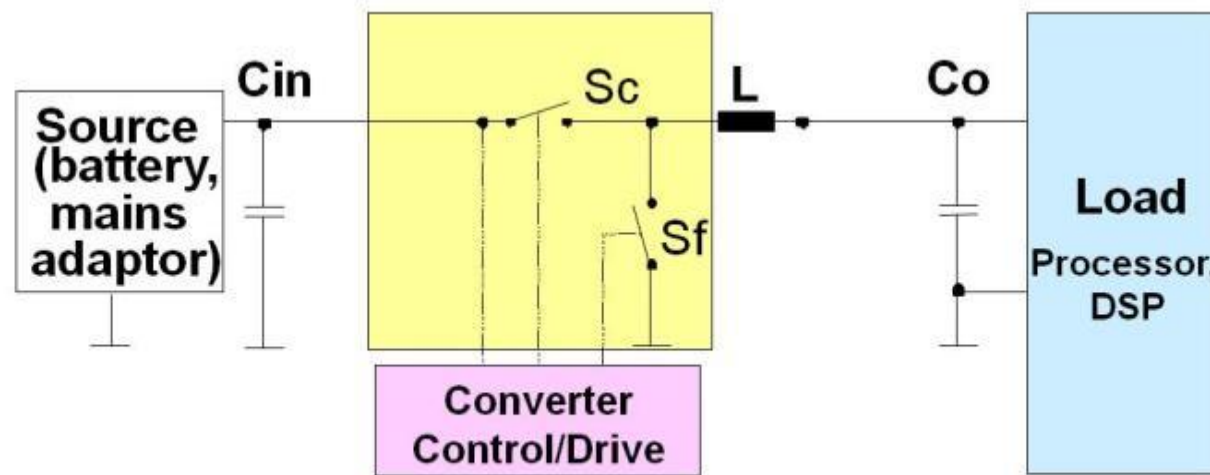
**[www.tyndall.ie](http://www.tyndall.ie)**

**[Cian.omathuna@tyndall.ie](mailto:Cian.omathuna@tyndall.ie)**



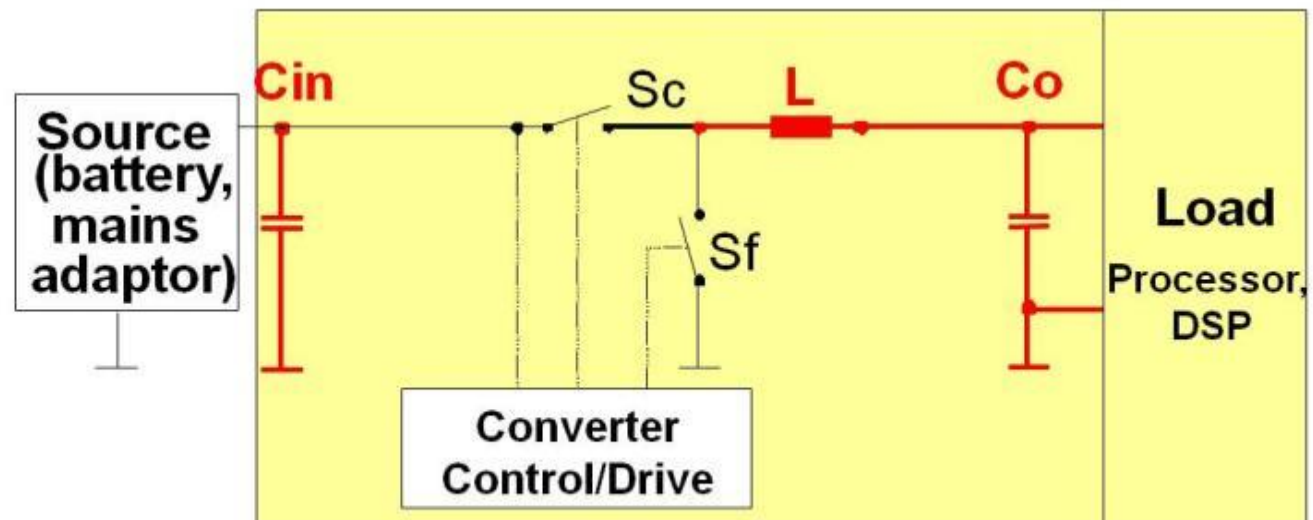
- **Evolution of Power Converters**
- **Integrated Magnetics**
- **Killer Applications?**
- **“Functional Passive” Interposers**
- **Supply Chains**
- **Conclusions**
- **The Magicians!**





**Conventional SMPS**  
Discrete switches,  
control, passives & load

**PwrSoC**  
Integrated power  
with load

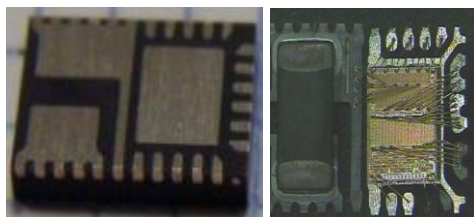


# Power Management - Supply Chain Evolution

**Power Bricks**  
**PSU**  
**Companies**

**PwrSiP**  
**Power Semiconductor**  
**Semiconductor Companies**  
**PCB Companies**

**PwrSoC??**  
**System on Chip**  
**Companies**



MicroSiP™  
Package

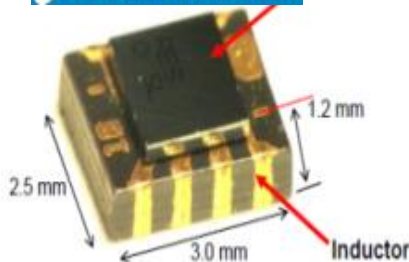


MicroSiP™ cross-sectional view

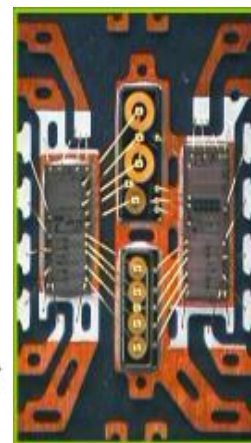


1Q 2011

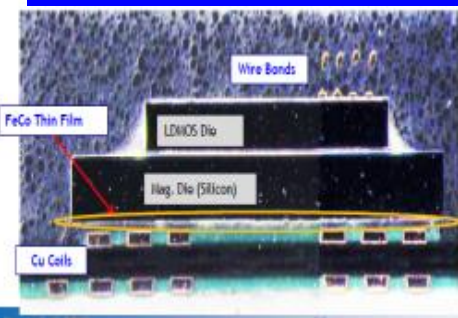
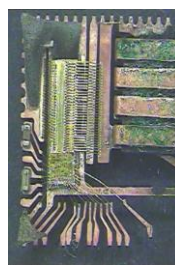
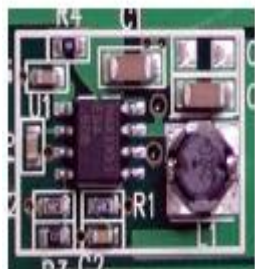
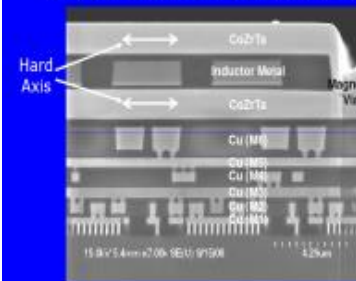
Regulator



Inductor



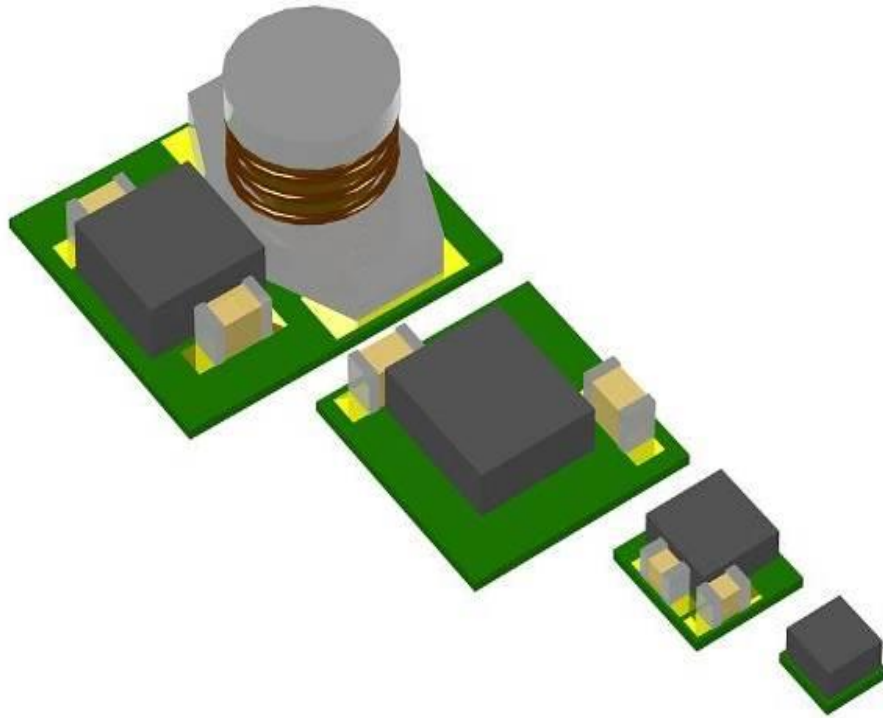
Cross-Sectional Image of Inductor  
in 130 nm 6-level Metal CMOS Process



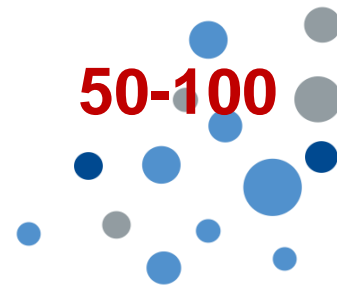
- **Take Up No Space**
- **Cost Nothing**
- **Last Forever**
- **Zero Power Loss**



# Evolution to Power Supply on Chip (PwrSoC)



Footprint (mm <sup>2</sup> )	Volume (mm <sup>3</sup> )	Frequency MHz
50	150	1
30	25	5
7.0	3.5	20
2.0	1.0	50-100



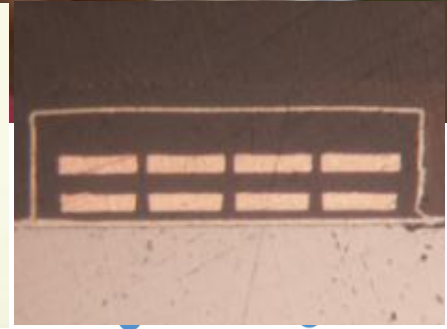
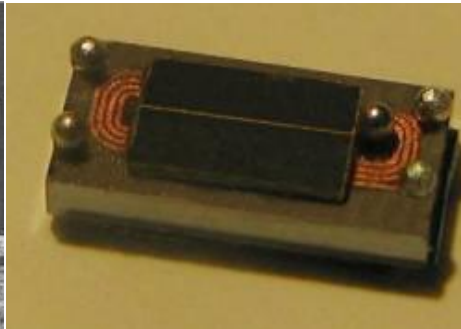
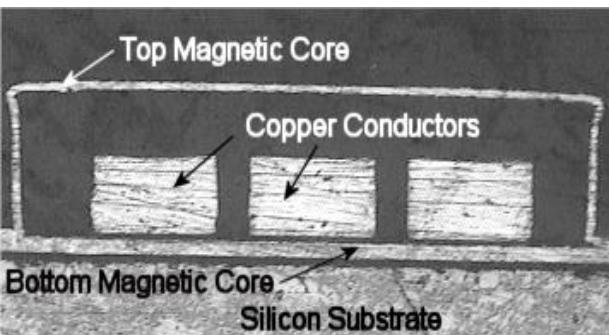
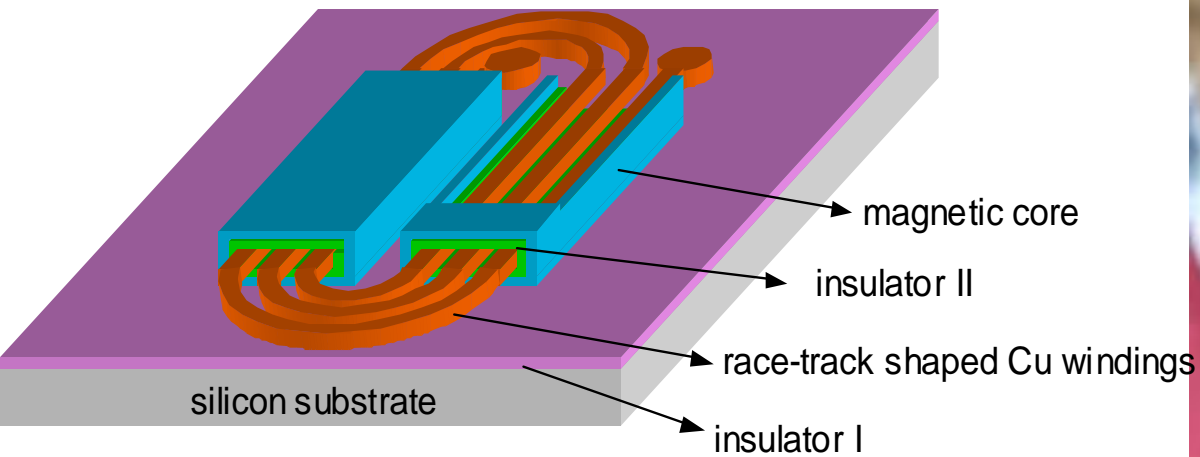
- Evolution of Power Converters
- **Integrated Magnetics**
- Killer Applications?
- “Functional Passive” Interposers
- Supply Chains
- Conclusions
- The Magicians!





## MAGIC

*Making Magnetics Disappear into ICs*





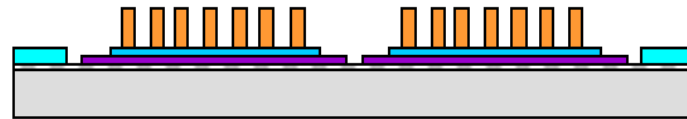
## Magnetic cores wrap around windings



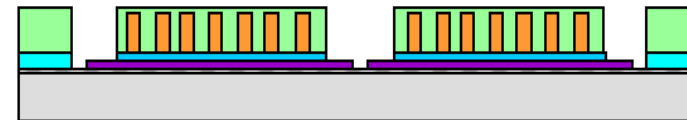
1<sup>st</sup> Metal Layer



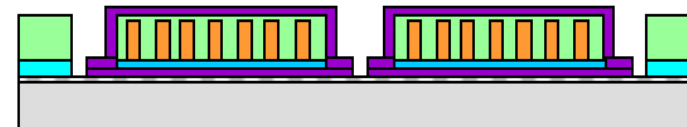
ILD- Insulation  
layer



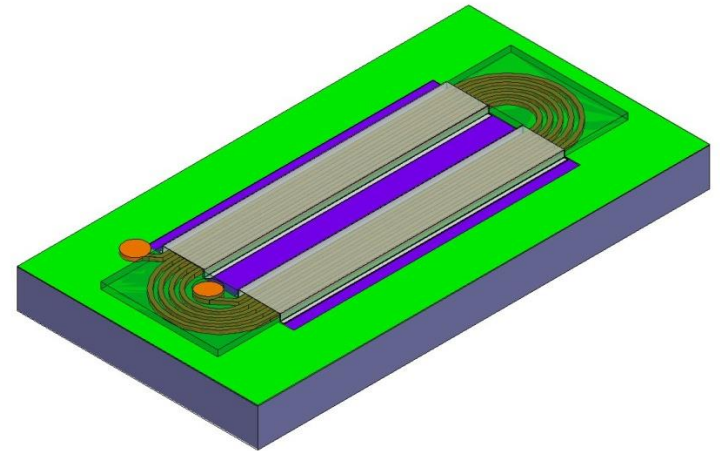
2<sup>nd</sup> Metal Layer



IMD- Insulation  
Layer

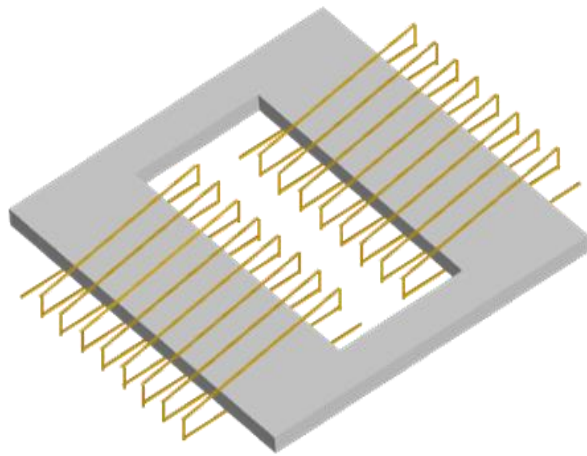


3<sup>rd</sup> Metal Layer



# Micro-magnetics Process (Toroidal structure)

Windings wrap around magnetic core



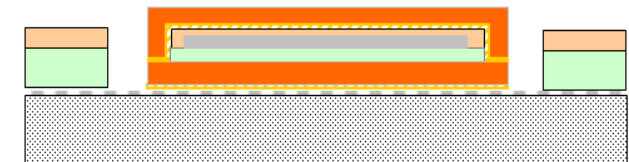
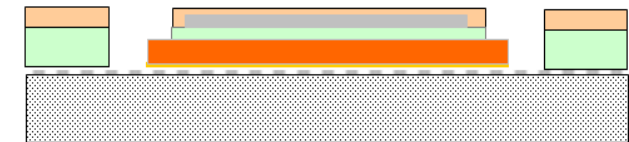
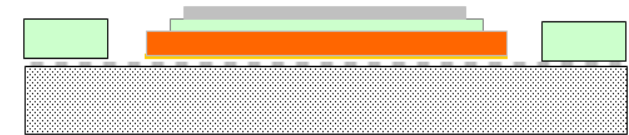
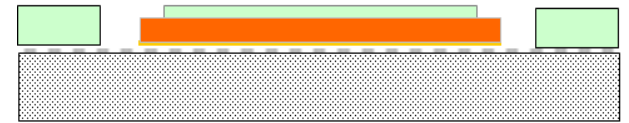
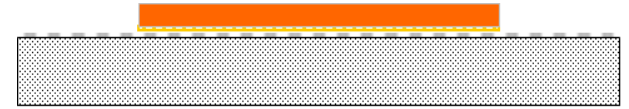
1<sup>st</sup> Metal Layer

ILD- Insulation  
layer

2<sup>nd</sup> Metal Layer

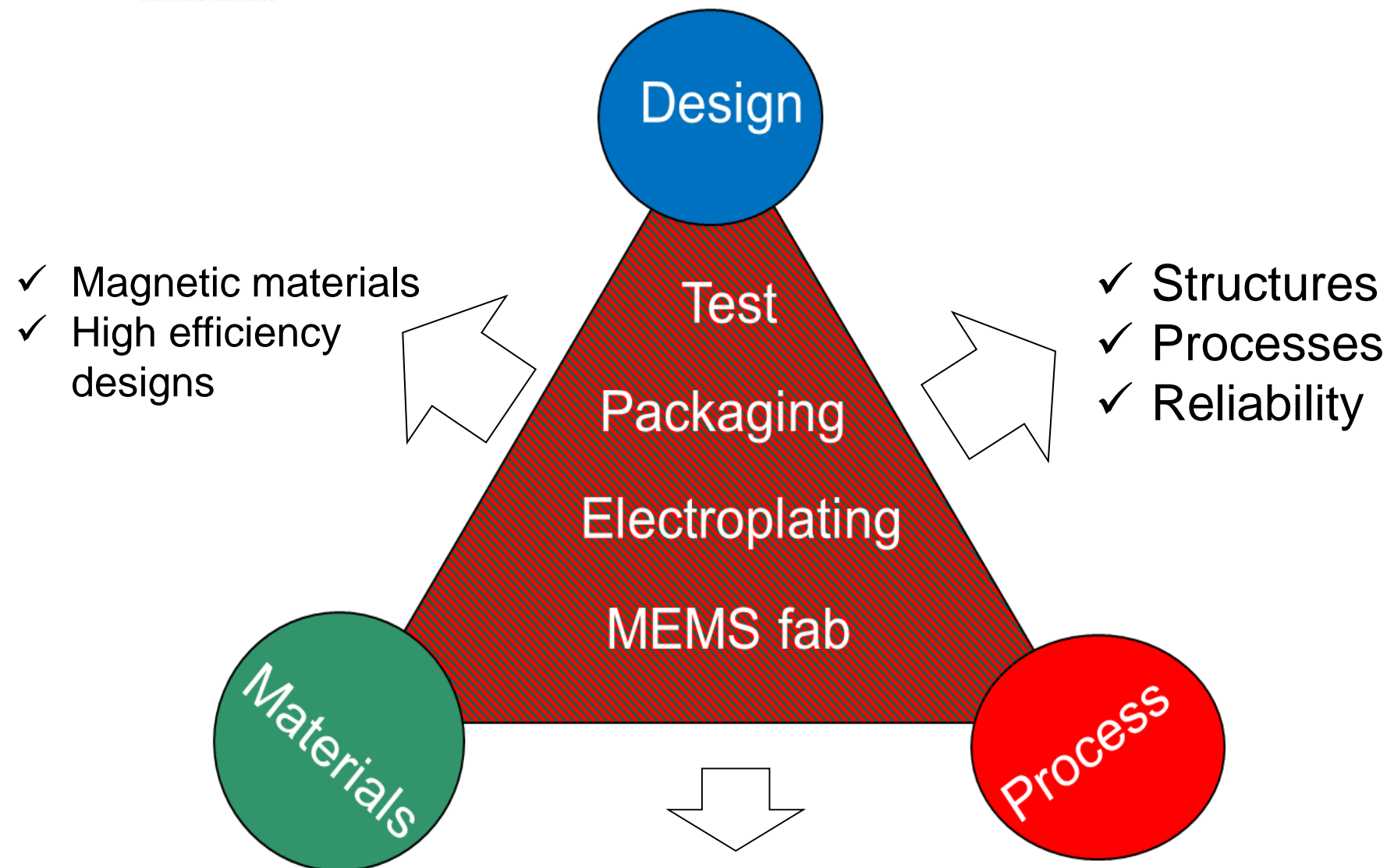
IMD- Insulation  
Layer

3<sup>rd</sup> Metal Layer



# Micro-inductor structures - Summary

Conventional Micro-inductors	Advantages	Disadvantages
<b>Solenoid &amp; Toroid</b>	<ul style="list-style-type: none"> <li>• High saturation currents</li> <li>• Ease of magnetic core deposition and lamination</li> <li>• Uniaxial anisotropy applicable in solenoid cores</li> </ul>	<ul style="list-style-type: none"> <li>• Complex fabrication process for windings</li> <li>• Uniaxial anisotropy for closed core structures difficult to realise for toroidal cores</li> </ul>
<b>Planar/ Spiral</b>	<ul style="list-style-type: none"> <li>• Ease of winding deposition</li> <li>• High inductance densities</li> <li>• Suitable for low-medium current applications</li> </ul>	<ul style="list-style-type: none"> <li>• Higher DC resistance</li> <li>• Low saturation current</li> <li>• Needs two layer magnetic core for higher inductance</li> <li>• Uniaxial anisotropy for closed core structures difficult to realise</li> </ul>
<b>Racetrack</b>	<ul style="list-style-type: none"> <li>• Ease of winding deposition</li> <li>• High inductance densities</li> <li>• Suitable for low-medium current applications</li> <li>• Uniaxial anisotropy applicable in racetrack cores</li> <li>• Higher operational frequency</li> </ul>	<ul style="list-style-type: none"> <li>• Higher DC resistance</li> <li>• Low saturation current (&lt;1 A)</li> <li>• Needs two magnetic layer core</li> <li>• Core laminations is more difficult to realise</li> </ul>
<b>Stripline</b>	<ul style="list-style-type: none"> <li>• High inductance densities</li> <li>• High current handling</li> <li>• Low DC resistance</li> <li>• Easy of winding deposition</li> <li>• Uniaxial anisotropy applicable in stripline cores</li> <li>• High operational frequency</li> </ul>	<ul style="list-style-type: none"> <li>• Needs two magnetic layer core</li> <li>• Core laminations is more difficult to realise</li> <li>• Difficult to achieve high inductance within reasonable aspect ratio structure</li> </ul>



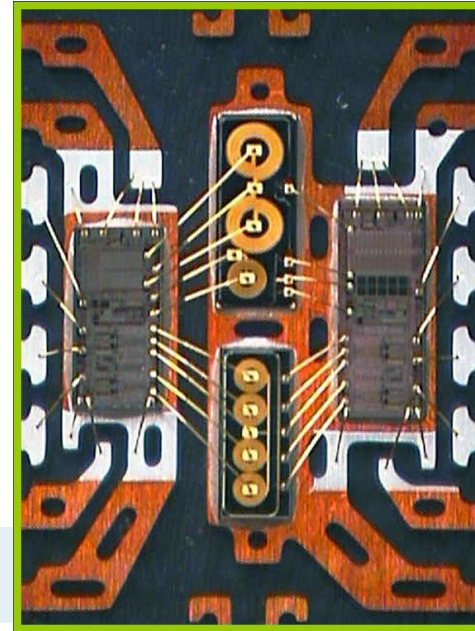
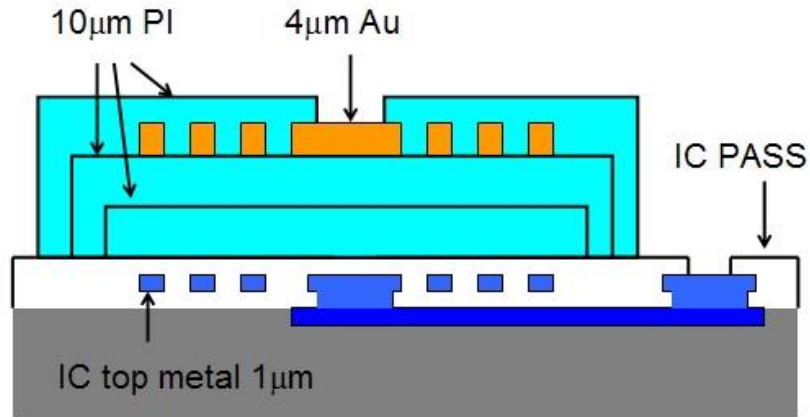
✓ Low loss Magnetics; laminations; high AR windings

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# On-Chip Coreless Transformer for Isolated Power (and Signal Transfer/Communications)

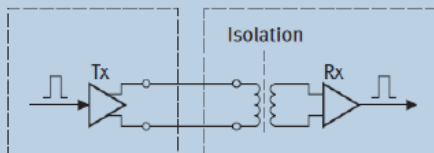
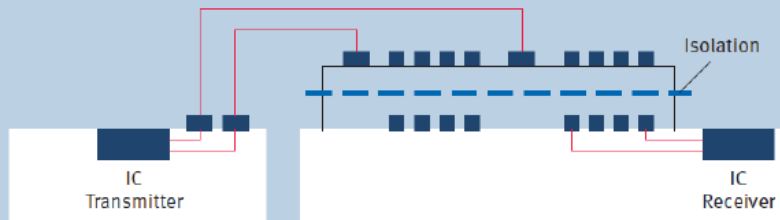


*iCoupler*



## ISOFACE™ PowerSiP

### Coreless Transformer Principle

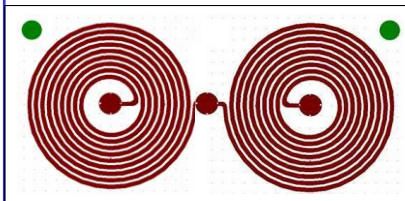
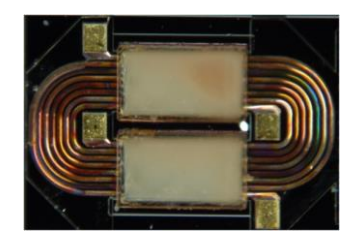
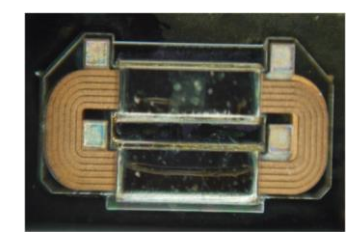
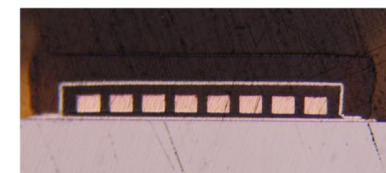



A lot of advantages compared to optocoupler

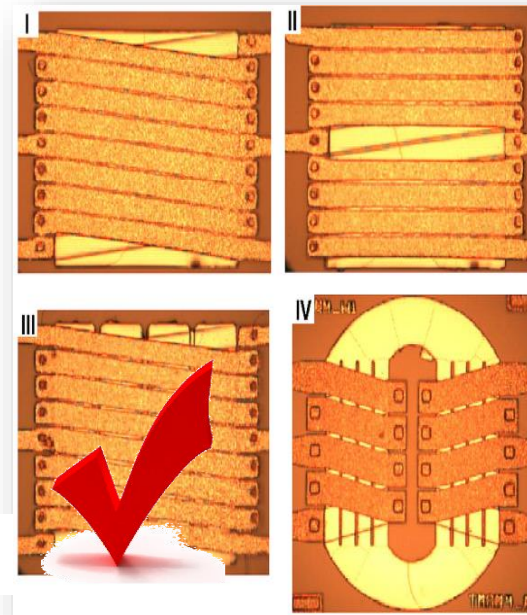
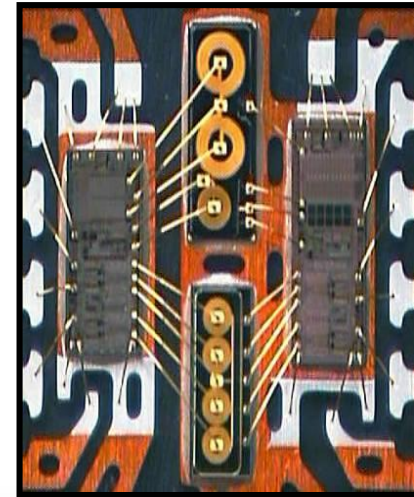
- No degradation over time
- Gain reliability
- High temperature range ... 150°C
- Very fast transmission (10 ... 100MHz)
- Low power consumption



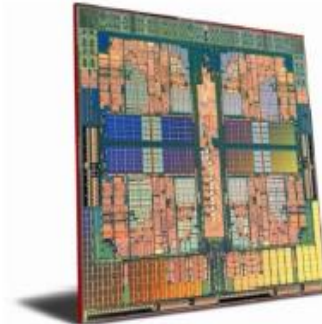


	Air Core	Tyndall Gen1	Tyndall Gen2
			
Technology	Air Core		
Device Size	2mm <sup>2</sup>	24mm <sup>2</sup>	3mm <sup>2</sup>
Frequency	180MHz	10MHz	20MHz
Inductance	8nH	440nH	240nH
L Density	17nH/mm <sup>2</sup>	18nH/mm <sup>2</sup>	80nH/mm <sup>2</sup>
Coupling	0.85	0.93	0.97
DC R	0.46 Ohms	0.5 Ohms	0.96 Ohms
Efficiency	70%	63%	78%

- Today's air-core transformers will be replaced with magnetic-core transformers.
- Multiple and Conflicting Design Constraints:
  - coupling, power loss, open circuit inductance, isolation, physical size.
- Magnetic Core *isoPower* Solenoid:
  - FeCoB multilayer.
  - Better Efficiency & Power.
  - Low Noise Emissions (EMI).



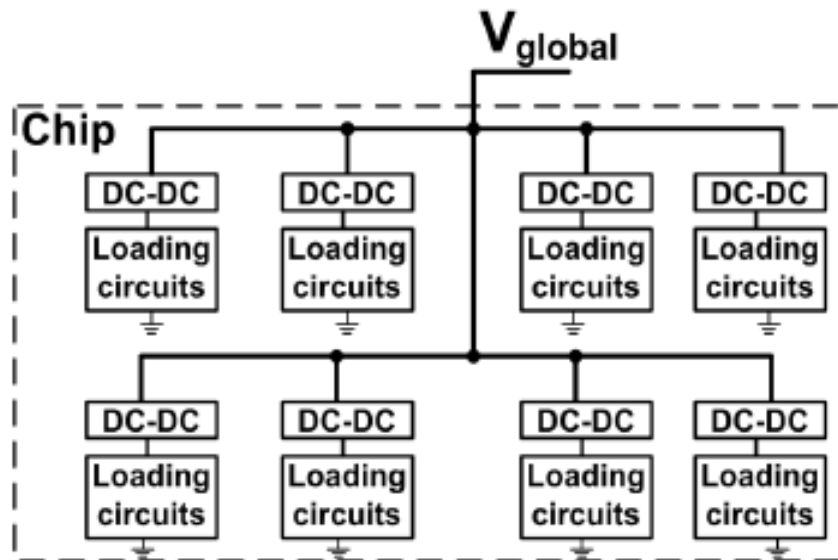
## Ex. 1: Multi-Core On-Die VR Motivation – Power Reduction



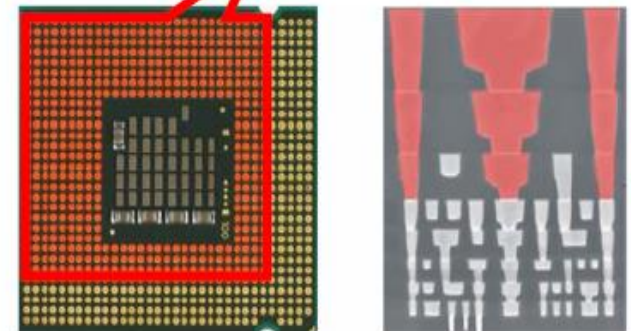
AMD Phenom Quad Core Processor

- Clear need for separate supplies to enable per-core power management.

How to efficiently support multiple voltage rails on the die?



70% of pins just for power



**100W - 1V - 100A - 1mΩ**  
(Power ~ 1W/mm<sup>2</sup>)

Source: PwrSoC 2010

## Endura Technologies and MediaTek Inc. Announce Commercial Partnership

DUBLIN, Ireland and HSINCHU, Taiwan, **May 4, 2016** /PRNewswire/ -- Endura Technologies (International) Ltd. announced a commercial partnership with MediaTek

**Endura Technologies (International) Ltd**, headquarters in Dublin, Ireland

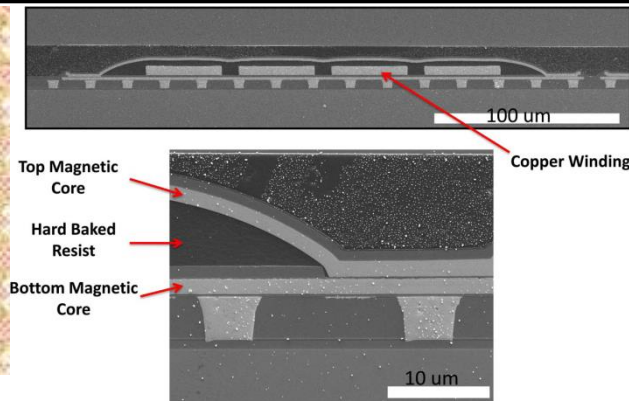
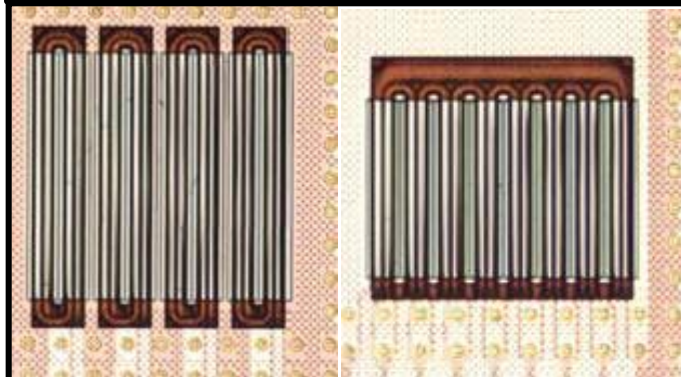
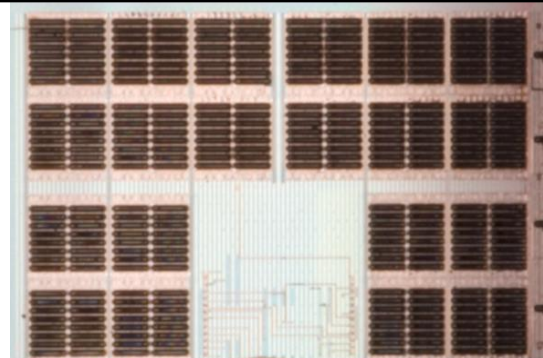
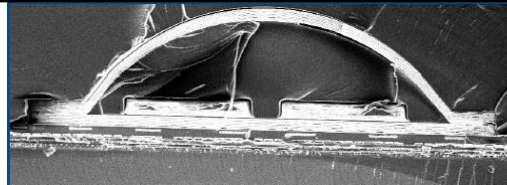
- fabless semiconductor company providing leading edge power management solutions for the microelectronics industry
- two main focus areas are **embedded power management** for very demanding system-on-chip (SoC) CPU type applications, as well as stand-alone power management integrated circuits (PMICs)



# High Frequency IVR with Integrated Magnetics

	Frequency (MHz)	Inductance (nH)	Peak Converter efficiency (%)	topology	Inductor area (mm <sup>2</sup> )	Current density (A/mm <sup>2</sup> )	Inductance density (nH/mm <sup>2</sup> )
Intel	30-140	21	76%	16 phases	2.8	8.93	~170
IBM	30-300	12.5	71%	8 phases	1.96	3.21	50

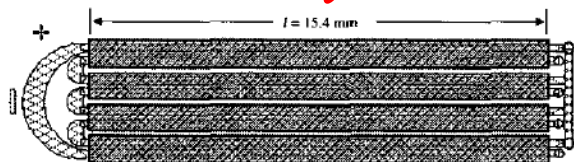
Monolithically integrated multi-phase Buck from Intel(2010)



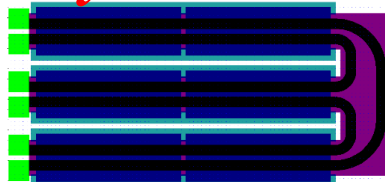
2.5D stacked multi-phase Buck from IBM (2013)

# Device 2 - Integrated coupled inductor

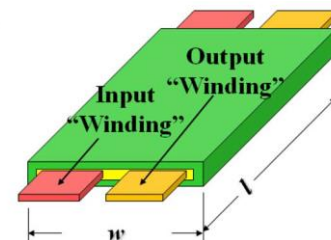
*Dartmouth/Tyndall'04*



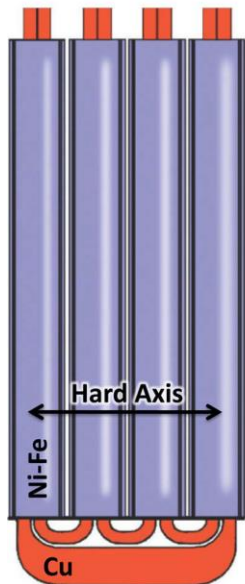
*Tyndall'14*



*INTEL'11*

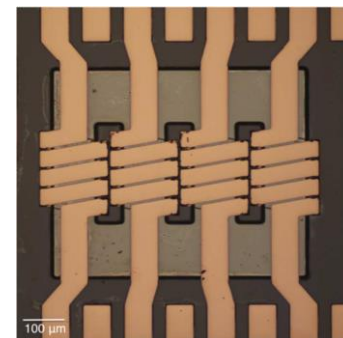


*Columbia/IBM  
/Duke'12*



	L self (nH)	DCR (mΩ)	Foot print (mm <sup>2</sup> )	Freq (MHz)	Convert Effic (%)
Dartmouth/ Tyndall'04	14	40	80	5	50
INTEL'11	25	14	2.8	>60	76
Columbia/ IBM/Ferric'12	7.4	480	10.9	100	71
Columbia/ IBM/Duke'13	12.5	270	2.5	>40	
Tyndall'14	45	27	3	5	
Tyndall/ Powerswipe' 15	35	155	2	100- 200	81 Expect!
NUIG/Tyndall'15	23	71	5	20	55

*Columbia/IBM  
/Ferric'13*

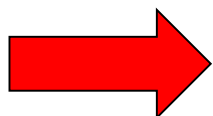




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# Evolution of Power Converters

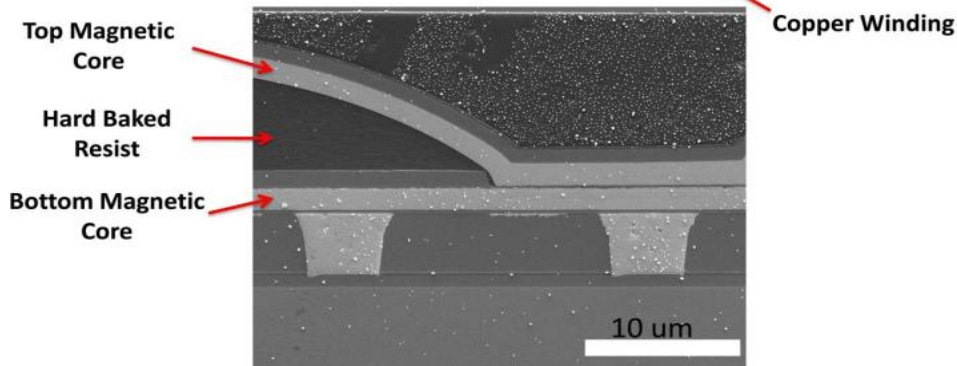
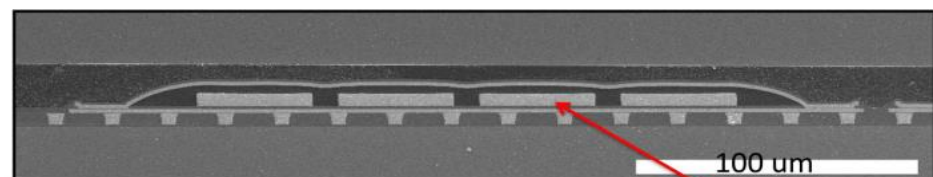
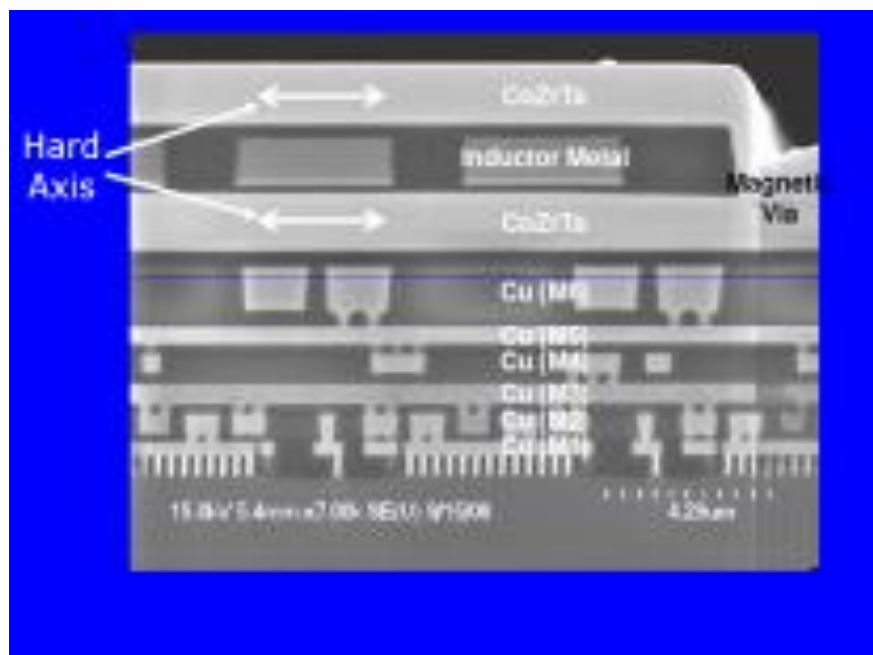


## PwrSoC

Inductor fabricated on Si die, load may also be integrated

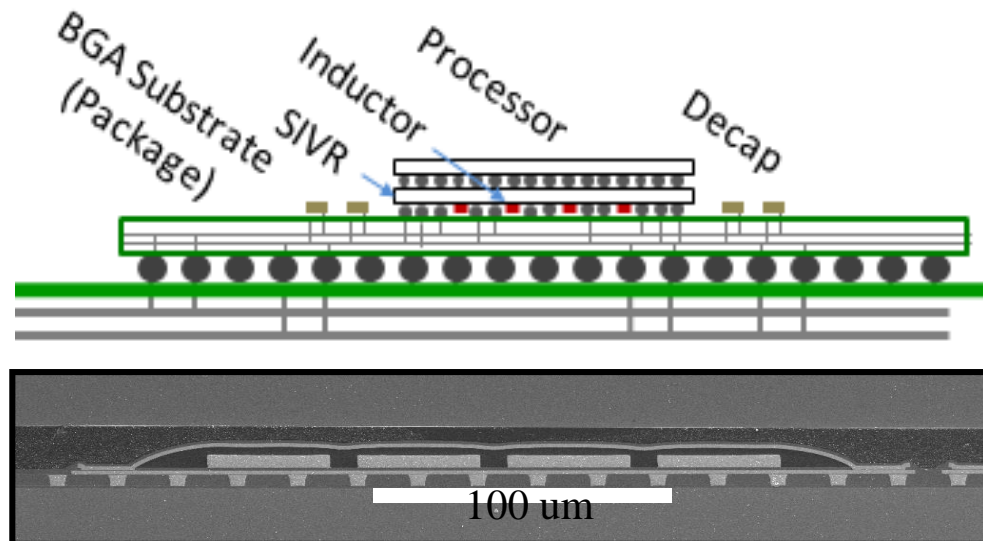


2.5D stacked multi-phase  
Buck from IBM (2013)



- **Increased power density from custom fabricated power inductors:**

- Inductors fabricated on low-cost interposer and integrated with IC via chip-stacking.
- Decap and power switches can be included on interposer design.
- Allows “one-way” current flow improving efficiency.
- Better transient performance due to lower impedance of input supply.
- Step on the way to monolithic integration?



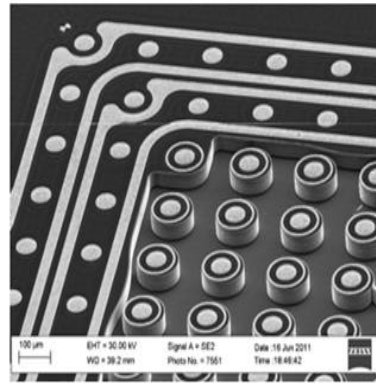
*Ref: Ken Shepard – Columbia University*

- EU FP7 Project: 619488 - Begin: Jan. 2014 - End: Dec. 2016

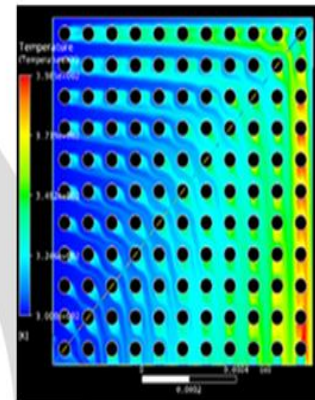


- IBM Research Zurich, Switzerland
- ETH Zurich, Switzerland
- Tyndall National Institute, Ireland
- Fraunhofer, Germany
- TU Chemnitz; Germany
- AMIC, Germany
- IPIDIA, France;
- Optocap, Scotland;

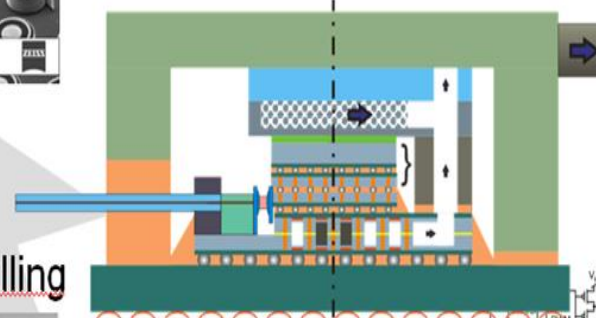
VP5: Interposer platform



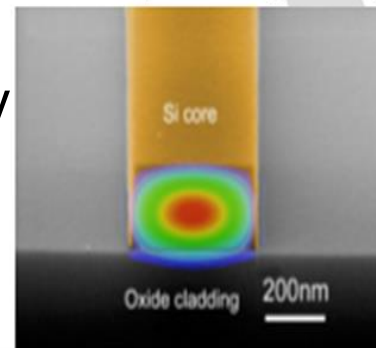
WP2: Heat removal



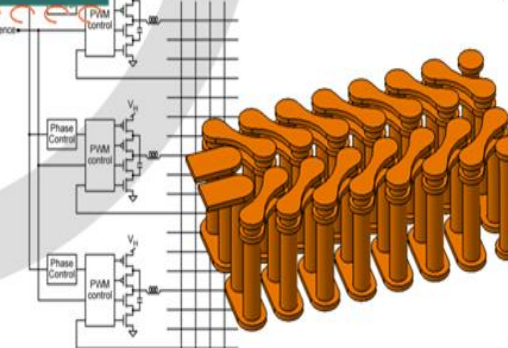
WP6: Demonstrator

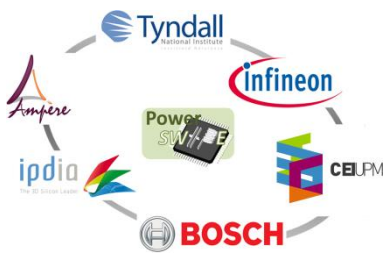


WP4: Optical signalling



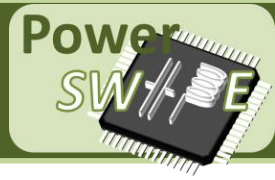
WP3: Power delivery





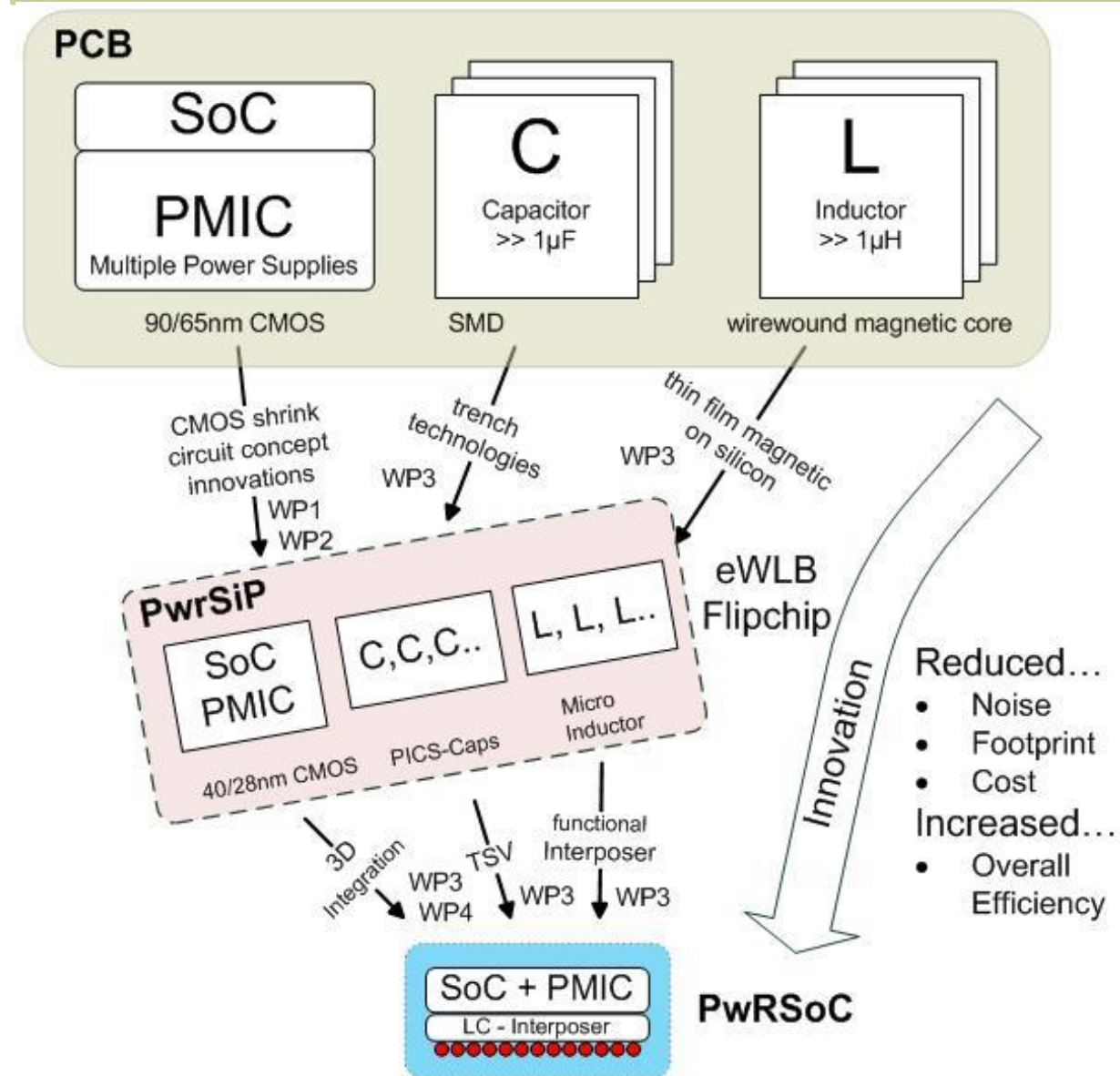
# PowerSwipe

## EU FP7-ICT-2011-8 – Project no.: 318529



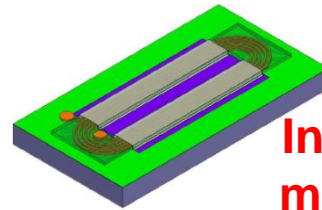
**POWER** SoC **W**ith **I**ntegrated **P**assiv**E**s

First EU-funded Project in Power Supply on Chip





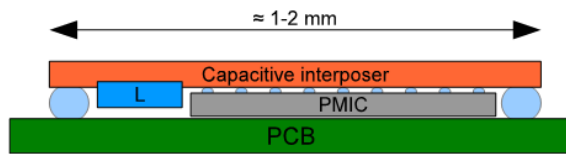
# Consortium Partners



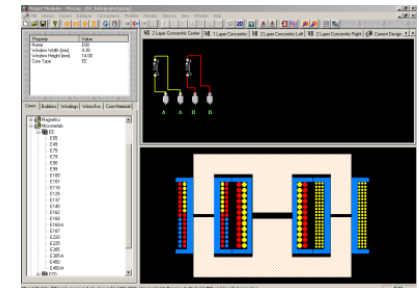
**Integrated  
magnetics**



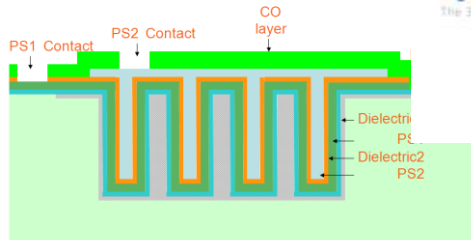
**Multi DC-DC converter**



**High efficiency, high  
frequency converter**



**CAD Tool**



**Trench  
Capacitors**



**$\mu$ C with embedded  
power management**

- **Evolution of Power Converters**
- **Integrated Magnetics**
- **Killer Applications?**
- **“Functional Passive” Interposers**
- **Supply Chains**
- **Conclusions**
- **The Magicians!**



# Intel Haswell packs integrated voltage regulator

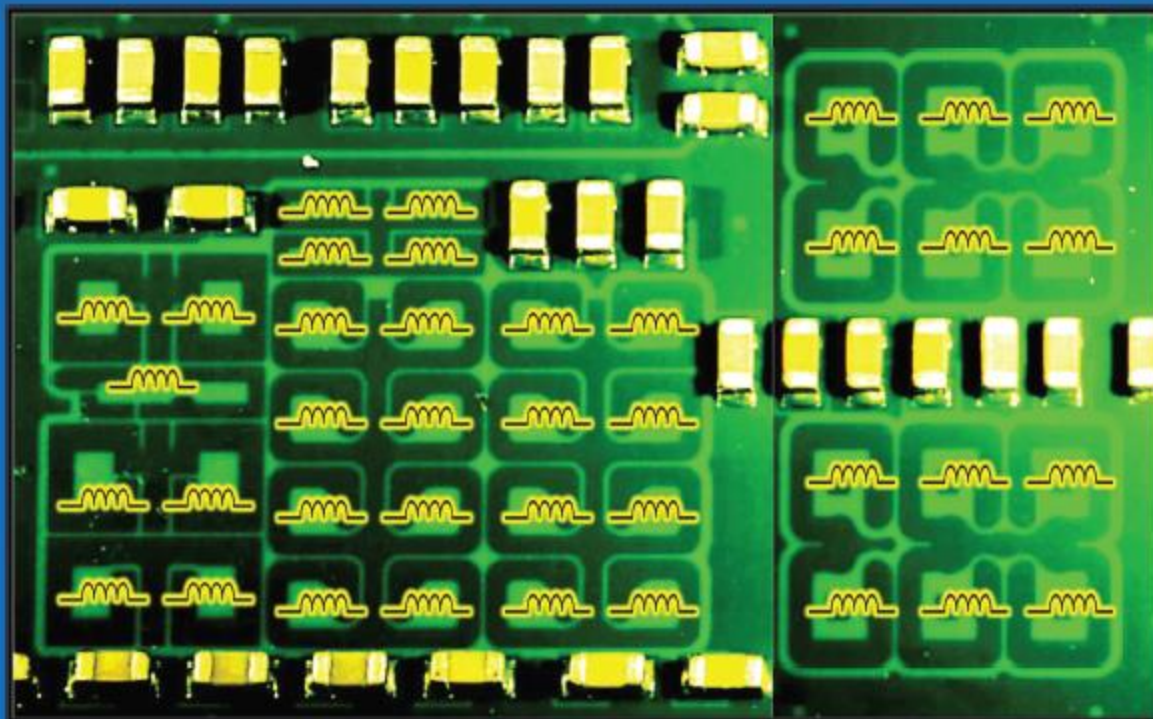
**Rick Merritt**

5/23/2013 06:53 PM ED



- .... seven external voltage regulators made by third parties, lower the bill of materials and motherboard footprint.
- .... deliver about 50 percent better battery life than the prior Ivy Bridge on active workloads while doubling graphics performance.
- Power Chip Vendors: ON Semiconductor, Intersil and Texas Instruments .... Linear Technology, Infineon, Maxim, Volterra and International Rectifier.

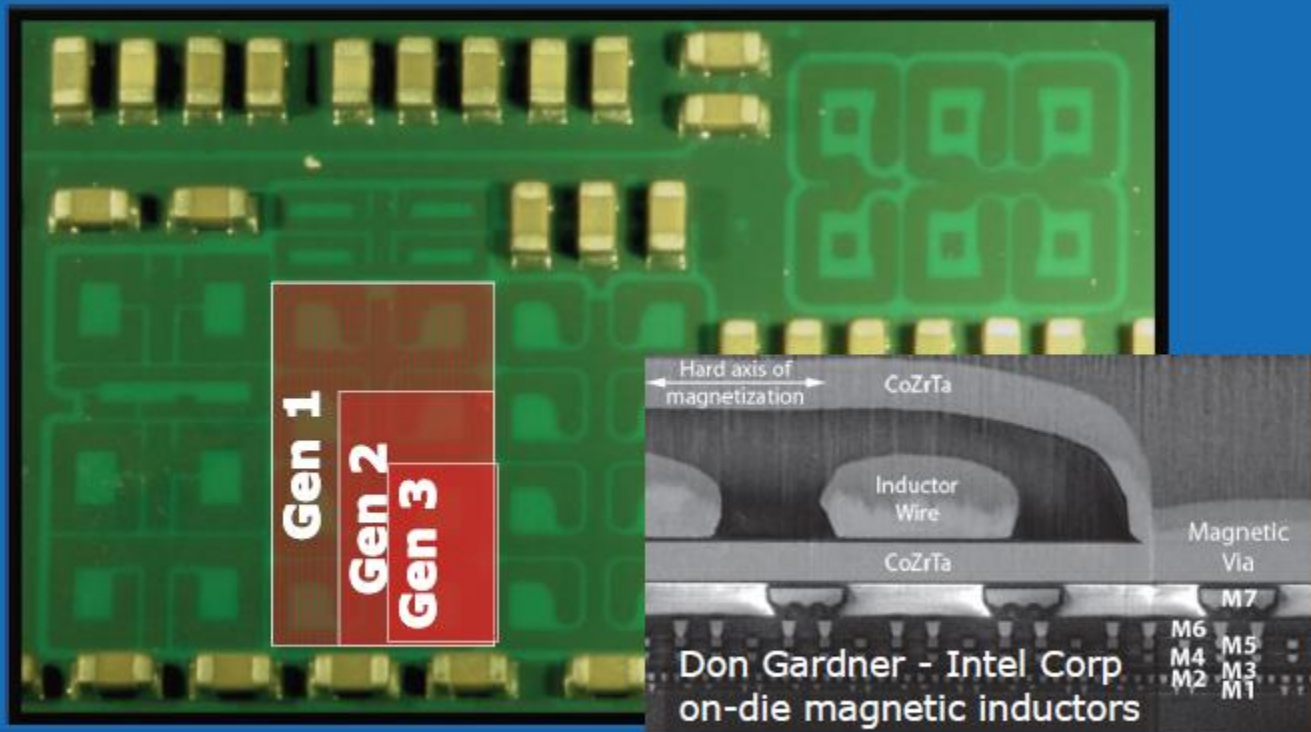
## FIVR Photo - Package Underside



Edward (Ted) Burton – Intel Corporation – APEC 2015

6

# Future Scaling Issue & Solution





PWR'SOC'08

PWR'SOC'10

PWR'SOC'12

PWR'SOC'14



ASE GROUP



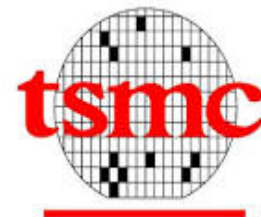
HUAWEI



maxim  
integrated™



TEXAS INSTRUMENTS

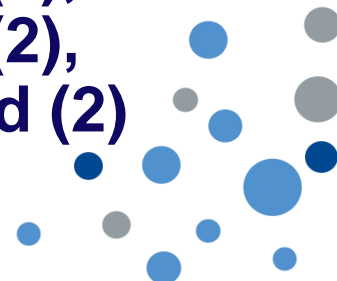




**189 Attendees**  
**50:50 Industry/Academia**  
**Boston, MA, USA – October 2014**

**Altera (2), Anagenesis (2), Analog Devices (6), Apple (2),  
Dell (2), Dialog (3), Fairchild (2), Ferric Semiconductor (2),  
Huawei (7), IBM (6), Infineon (2), Intel (5), IPDIA (2),  
Maxim (9), Mornsun Guangzhou S&T Co., (2), Murata (4),  
NXP (3), Qualcomm (4), Raytheon (2), Silana  
Semiconductor (2), TI (4), Treehouse Design (2), TSMC (2),  
Würth Elektronik (4)**

**Carnegie Mellon (2), Dartmouth College (5), Harvard (6),  
Insa Lyon (3), MIT (10), NCSR Demokritos (2),  
Northeastern (2), Tyndall (3), UC Berkeley (2),  
U. Illinois UC (2), U. of Toronto (6), UP Madrid (2)**



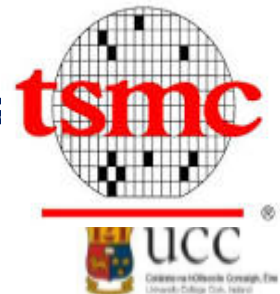
## Highlights

- **Switched Capacitor Vs Inductor Converters**
- **Granular power for multi-voltage rail, multi-core, microprocessors, servers, HPC**
- **High density on-chip, capacitors**
- **Foundry Opportunities – PSiP (including PCB embedded silicon) to PwrSoC**

## Personal Highlights Magnetics on Silicon

- **Ferric Semiconductor:**

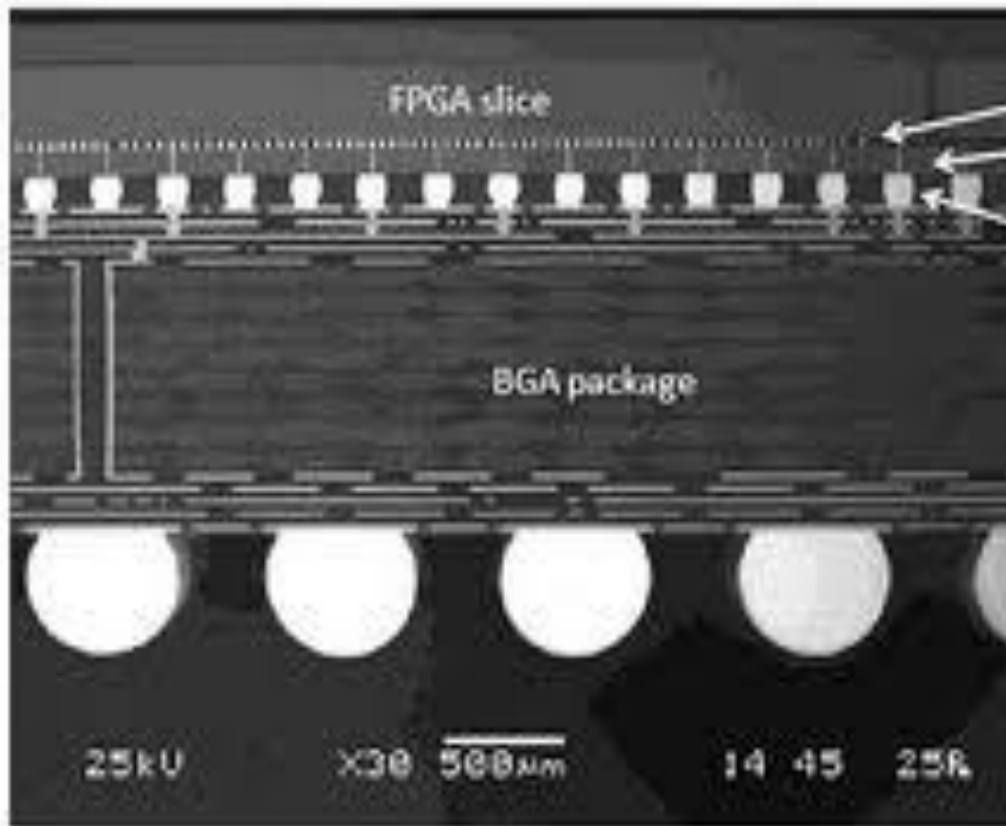
- Fabless Semiconductor Company
- Delivering complete IVR solution
- Package Voltage Regulator / Monolithic Voltage Regulator
- CMOS compatible integrated power inductors
- Integrated power inductor devices will be accessible through High Volume Manufacturing Foundry with standard CMOS design flow support (DRC, LVS, xRC, advanced models).
- Devices will be available as BEOL process option at TSMC s



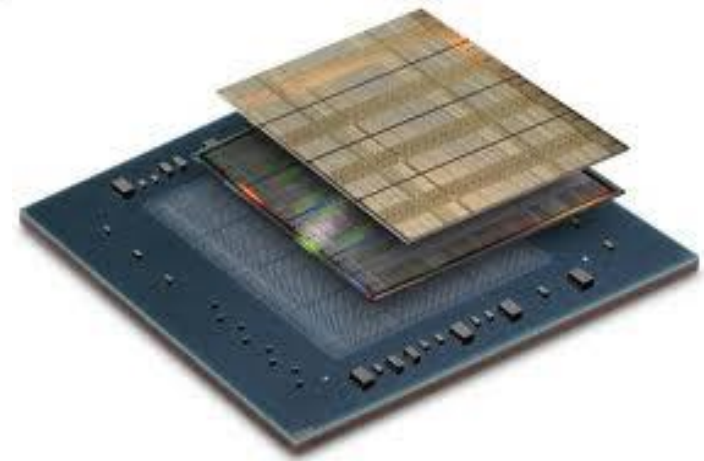
## Product News

**Xilinx ships the world's first heterogeneous 3D FPGA**

**Clive Maxfield 5/30/2012 03:43 PM EDT**

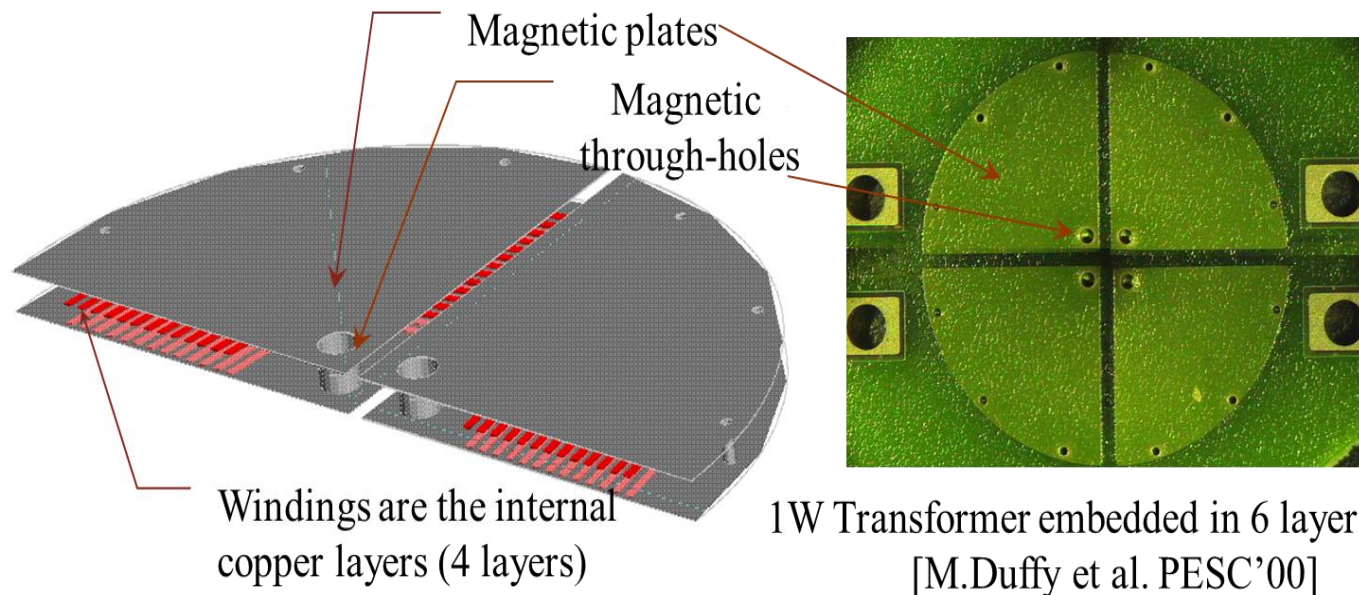


Micro bumps  
SI interposer with TSV  
C4 bumps



## Pot-core transformer structure

[US Patent No. 6.150,915]



1W Transformer embedded in 6 layer PCB,  
[M.Duffy et al. PESC'00]

- Magnetic layers and windings embedded in the printed circuit board
- Magnetic through-holes provide closed magnetic path
- Patterning of magnetic plates reduces eddy-current effects



- **Evolution of Power Converters**
- **Integrated Magnetics**
- **Killer Applications?**
- **“Functional Passive” Interposers**
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Applications

System Integration

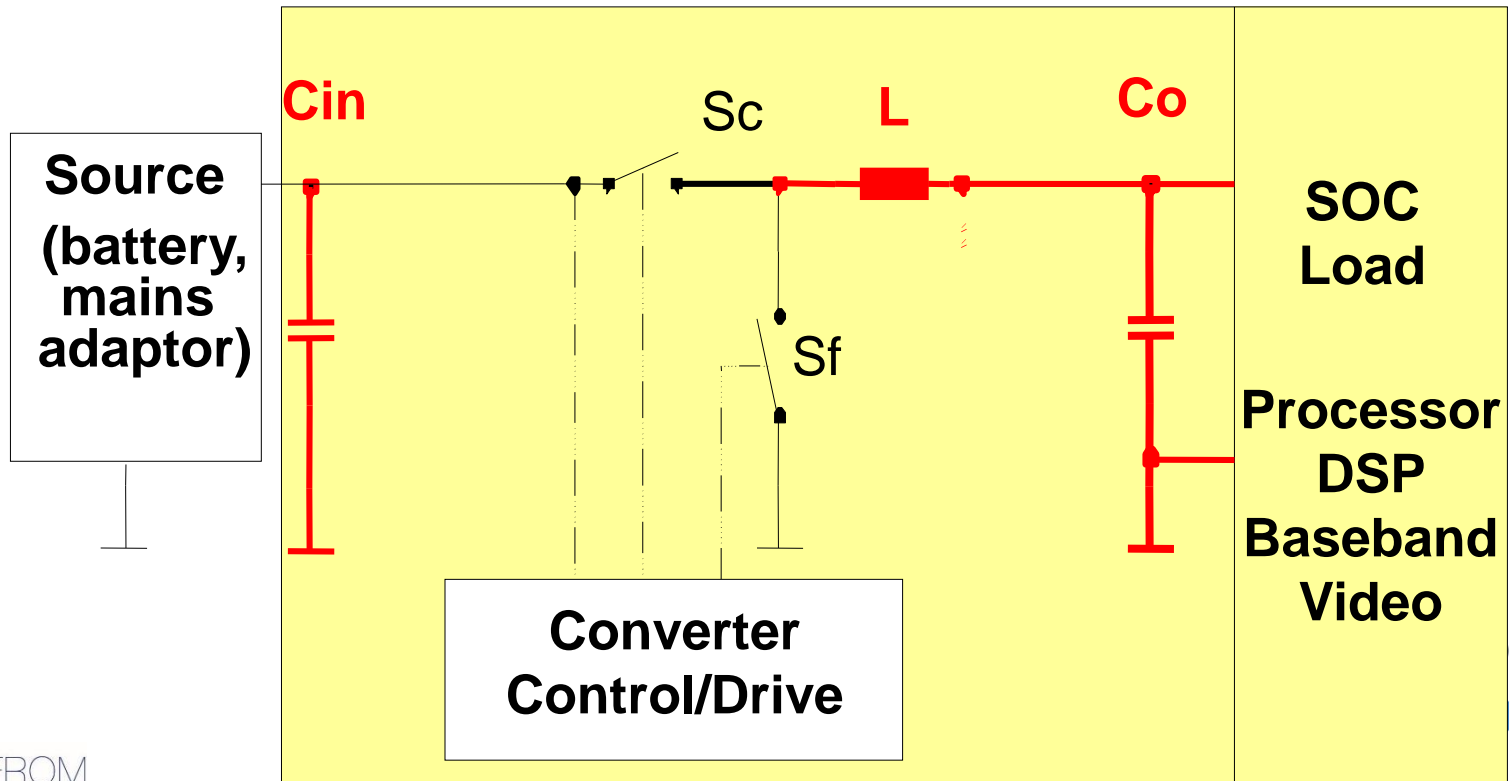
Manufacturing Supply Chain

Magnetics

Capacitors

Topologies &  
Control

Power Switches



- **System-level Solution**
- **Technology Progression:**
  - High frequency operation
  - EMI
  - Wafer-level Test
  - Reliability
- **Manufacturing Supply Chain:**
  - Magnetics on Silicon – BEOL / Foundry / OSAT
  - 2.5D / 3D Integration
  - Passive Interposers with integrated inductors and capacitors
- **Integrated CAD**

## Integrated Power Conversion and Power Management



The 5<sup>th</sup> edition of the International Workshop on Power Supply On Chip will be held at the Universidad Politécnica de Madrid, Spain, provisionally scheduled for October 3-6, 2016. This conference is organized by the Centro de Electrónica Industrial (CEI-UPM).



PwrSoC 2016 is the leading international technical workshop dedicated to advancing important power conversion technologies. The workshop focuses on the integration of both modular and granular commercially successful electronic power converters for multiple applications, by accessing a broad range of leading-edge technologies. Complete on-die integration and integration within package are of prime interest. System performance requirements presented by present day and emerging applications demand ever-greater current density, voltage regulation and optimized control, form factor reduction, efficiency, and cost reduction.

A major challenge on the path to integration and form factor reduction of dc-dc converters is the difficulty of integrating energy handling power passive components with conventional silicon processes. Advanced technologies for the design and manufacture of these passives are focal topics for the workshop. Strategies at circuit and system levels are of fundamental importance.

### Sessions

- Plenary Sessions
- Systems & Applications
- Topologies and Control
- Power Semiconductor Technology
- Magnetics
- Capacitors for Power Electronics
- System Integration, Packaging and Manufacturing
- Granular Power
- Open Forum Discussion

### Conference Site

The site of the conference is the Escuela Técnica Superior de Ingenieros Industriales of the Universidad Politécnica de Madrid. It is located on

- **PSMA**
- **EU PowerSwipe Team**
- **EU Carricool Team**
- **Tyndall Team**
  - **Integrated Magnetics**
  - **MEMS Fabrication**
  - **Electrodeposition**
  - **Test and Characterisation**
  - **Packaging and Integration**
  - **Business Development**
  - **Technology Transfer / Legal**