Silicon Carbide for Power Devices: History, Evolution, Applications, and Prospects.

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GE Global Research Center, Niskayuna, NY, USA.

GE Public

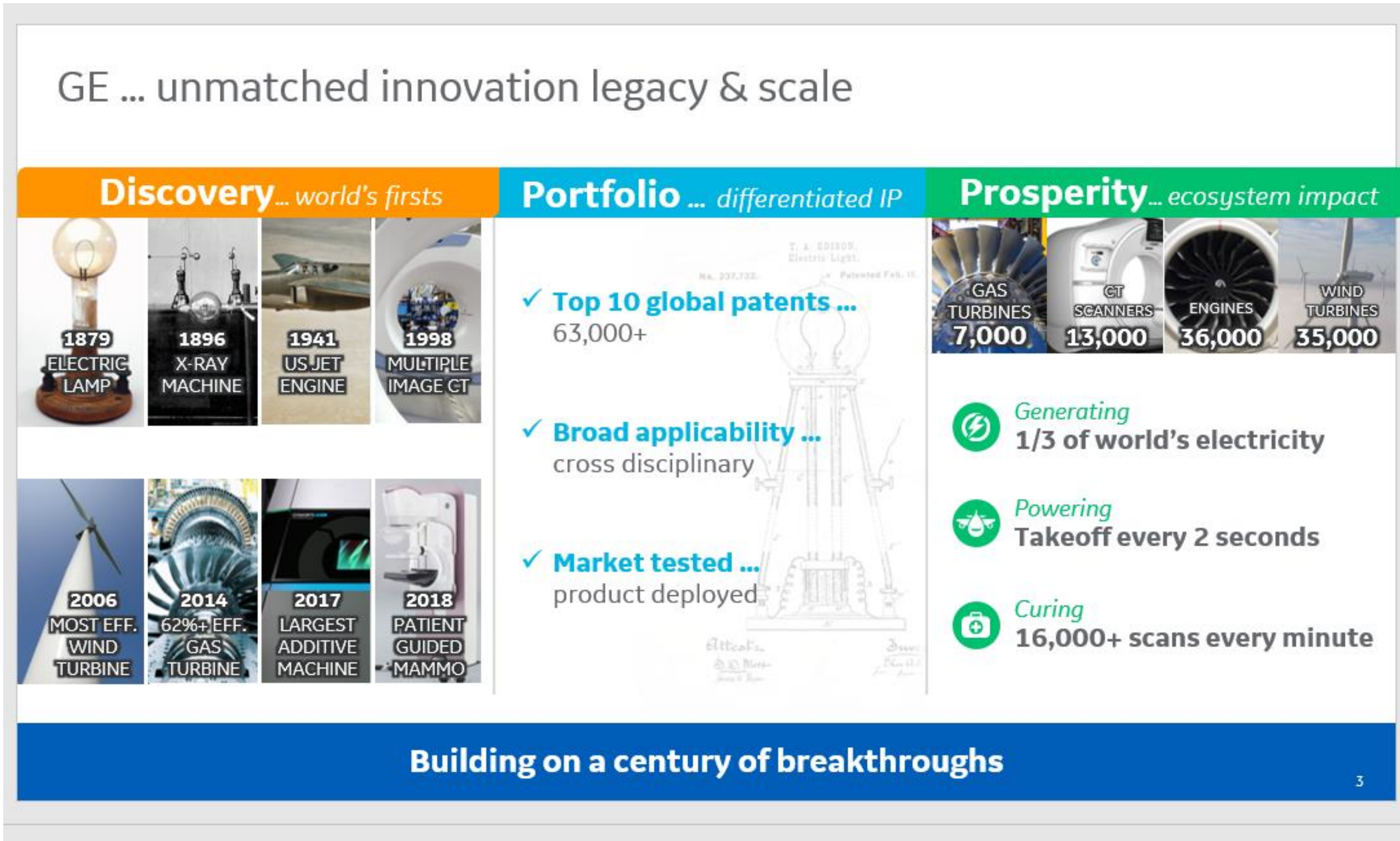
Toulouse, France, Apr. 24th, 2019

Acknowledgment

- GE Global Research Center Semiconductor Device, Cleanroom, High Temperature Electronics, and Packaging Teams.
- GE Global Research Power Electronics, Electrical Machines, and Power Systems Teams.
- Powerex Packaging and Device Teams.
- GE Aviation, Power, Renewables, and Healthcare Power Electronics Teams.
- DARPA, ONR, ARL, AFRL, DoE, ARPA-e, NASA, and many other US agencies that funded GE's SiC efforts.

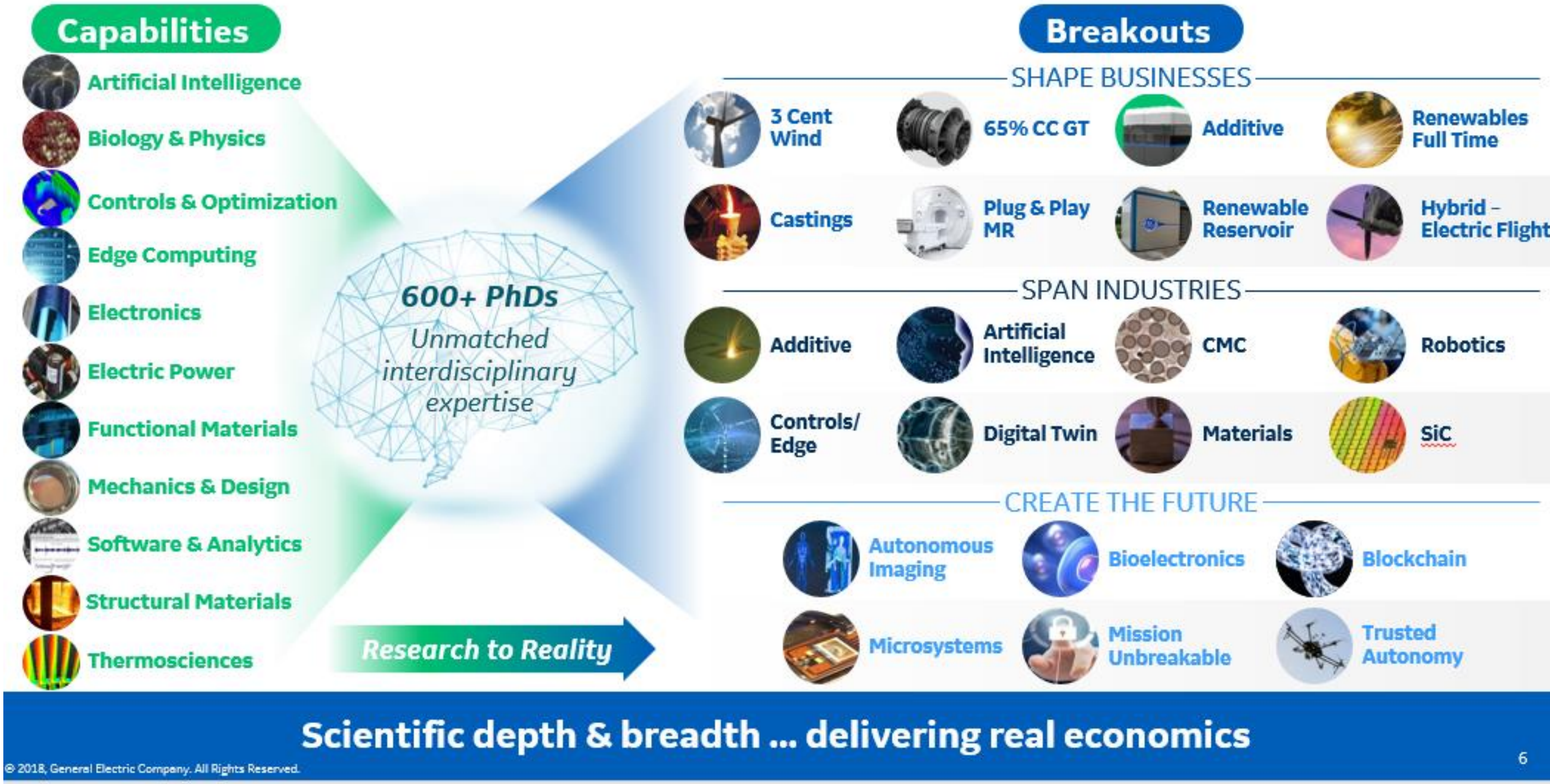
General Electric:

→127 years legacy → Global Reach
→Multi-disciplinary → Key Player in the Global Economy
→ Continuously Innovating



GE Global Research Center:

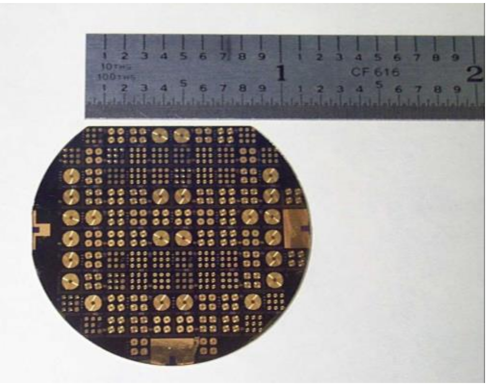
→Two locations – Niskayuna, NY & Bangalore, India, →Research Hub
→1,100 Scientists and Engineers, 600+ PhDs →~3,000 patents per year across GE
→11 technical disciplines →~60,000 visitors globally/year



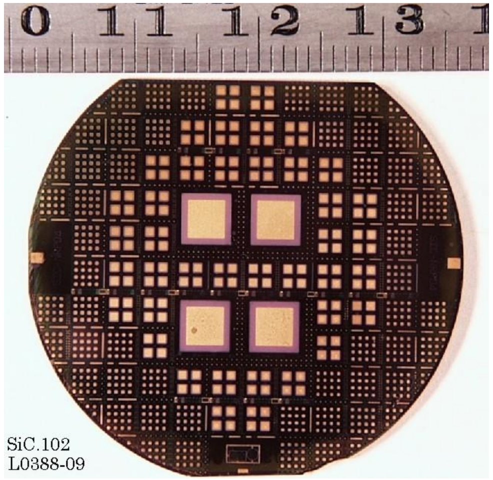
My SiC Credentials

- Started thinking about SiC in **1996**:
  - My PhD Thesis conclusion hailed SiC power devices as the future of Power Conversion.
  - Led modeling & testing task of GE DARPA Megawatt Program on SiC Power Devices **(1998-2000).**
- Worked on (1998-2019):
  1. Materials – Epitaxy.
  2. Device Structures- Design & Fab.
     1. Diodes, Thyristors, FETs, BJTs.
  3. Packaging.
  4. Applications.
  5. Commercialization.

$1_{3/8}$ " – 35mm Wafers.



SiC GTO Wafer: 50µm Epi.



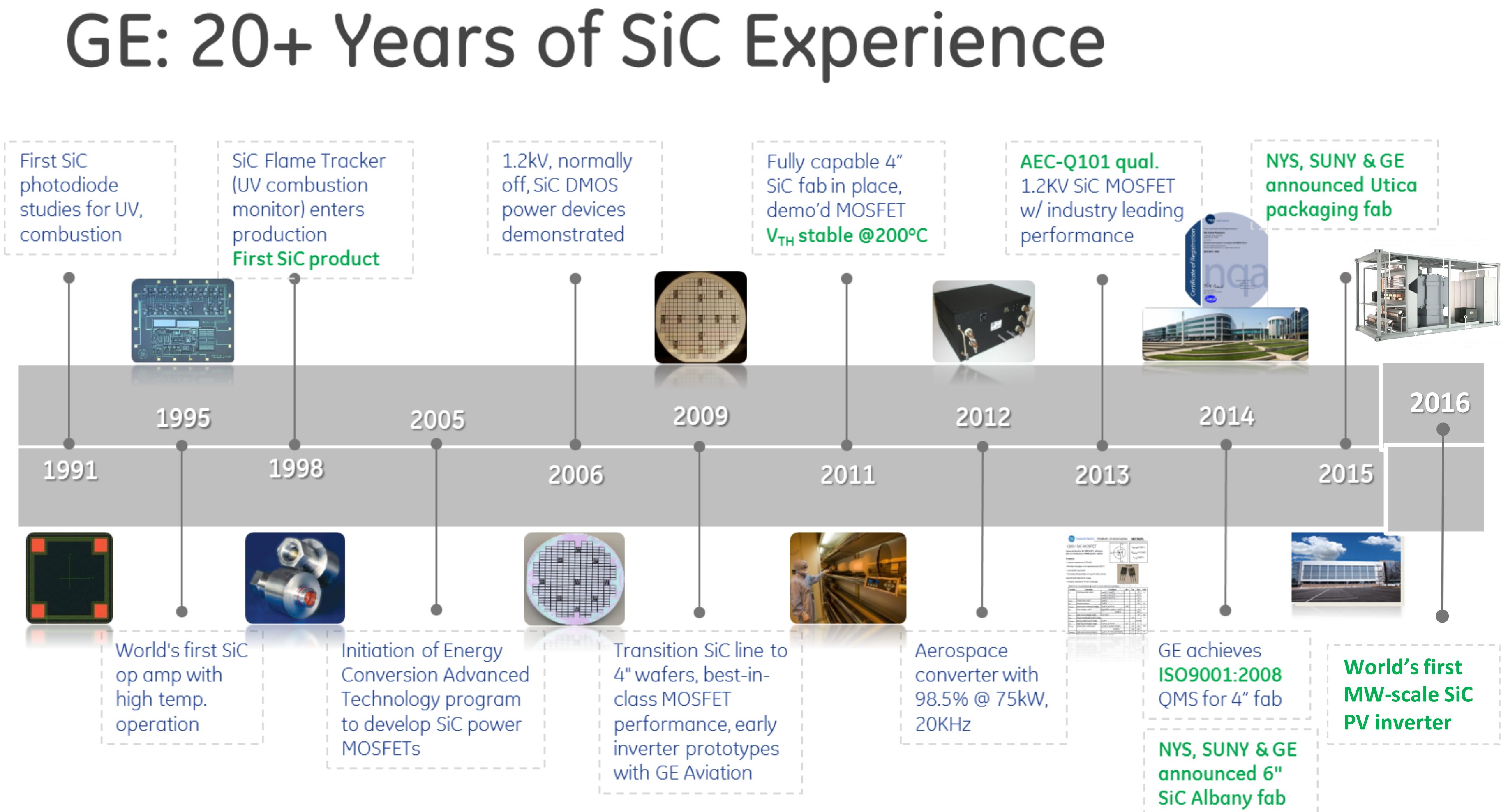
SiC PiN Mask Layout

Three Sizes: 4000µmx4000µm, 800µmx800µm, 250µmx250µm.

Wafers, Material, & Device Evolution Over the Past 20 Years

- 1”3/8 to 6” → 400% / Few microns of Epi →100-150microns.
- Few $1000s per wafer →Less than $1000 (in volumes).
- Too many killer defects →Fewer defects.
- 100s of µpipes per cm2 →Less than 1MP per cm2 – ZMP available.
- One commercial part →At least 5 commercial parts.
- Handful of manufacturers →Over 10 manufacturers.
- Small area devices (less than 1mmx1mm) →1cmx1cm.
- Few 100s of Vs blocking voltages →10s of kV → JTE Improvement.

GE SiC Timeline – Photodiodes & MOSFETs



** 2015-2017: Power Electronic Manufacturing Center 6" Fab. Commissioning.

* 2018-19 – Exploring Licensing Options and Partnerships for GE MOSFET Technology.

GE SiC Timeline – Schottky Diodes & Thyristors

1990

Started working with Cree.

1994

First SiC Photodiodes from GE's SiC installed in an Electric Power Plant.

*https://www.gemeasurement.com/sites/gemc.dev/files/flame_tracker_factsheet_r1_0.pdf

1998

DARPA SiC Megawatt: GE R&D, RPI, Powerex: Made PiN Diodes, GTOs:

- ✓ Built first Hybrid modules (Si IGBT/SiC PiN diodes).
- ✓ Performed first full comparison of Si and SiC diode.

2002

Built first 600V, 2*60A SiC Schottky diode module.

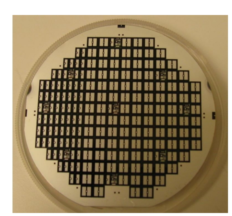
600V, 2x60A SiC Schottky Diode

2003

Started working on 3kV Pulse Power SiC Thyristors.

2006

First successful 3kV SiC Thyristors on 3" wafers.



2011

First successful 3kV SiC Thyristors on 4" wafers.

2013

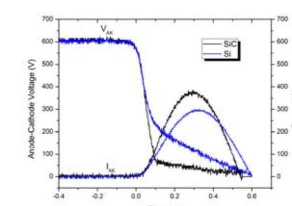
Completed over 1 million pulses at 2kV and 800A pulse current.

2015

Explored additional opportunities for SiC Thyristors – partnered with TPS to test GE Parts.

2016

Completed Phase 1 of SBIR with TPS and successfully demonstrated ns pulse capabilities of SiC Thyristors.

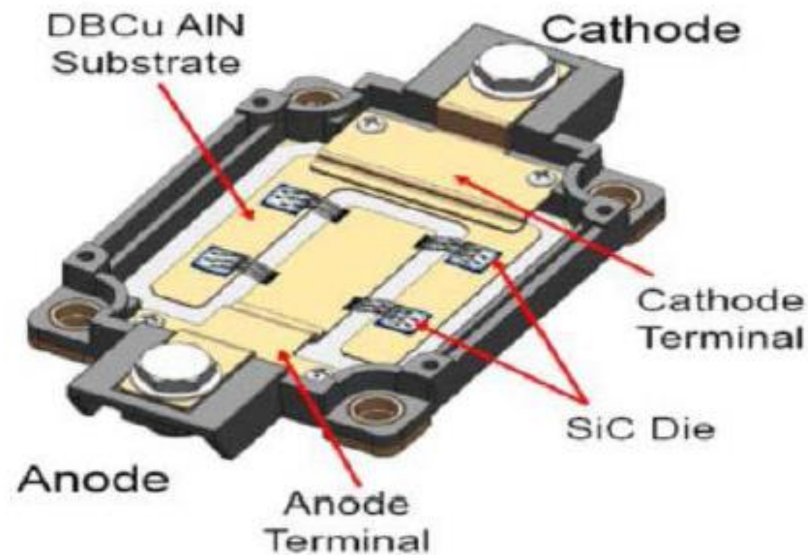


2017

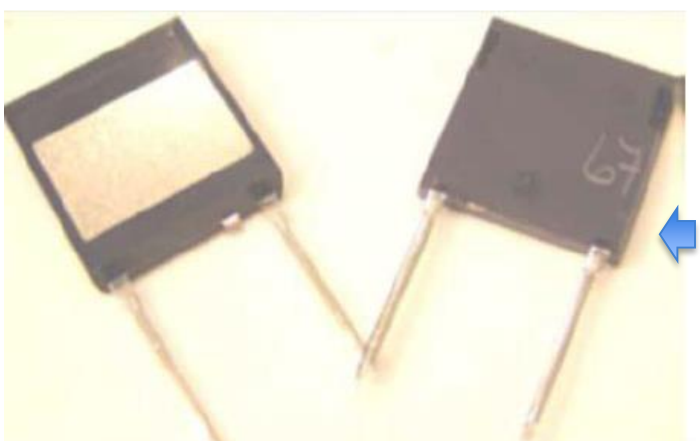
Still exploring opportunities for further commercializing SiC Thyristors, TVSs with commercial partners.

SiC Diodes: Schottky and PiN Diodes

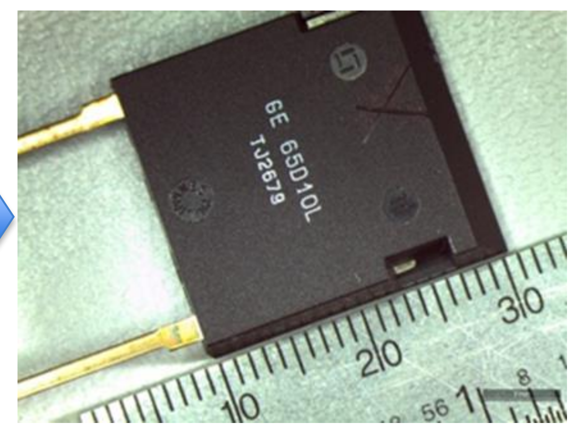
Powerex - ISOTOP™



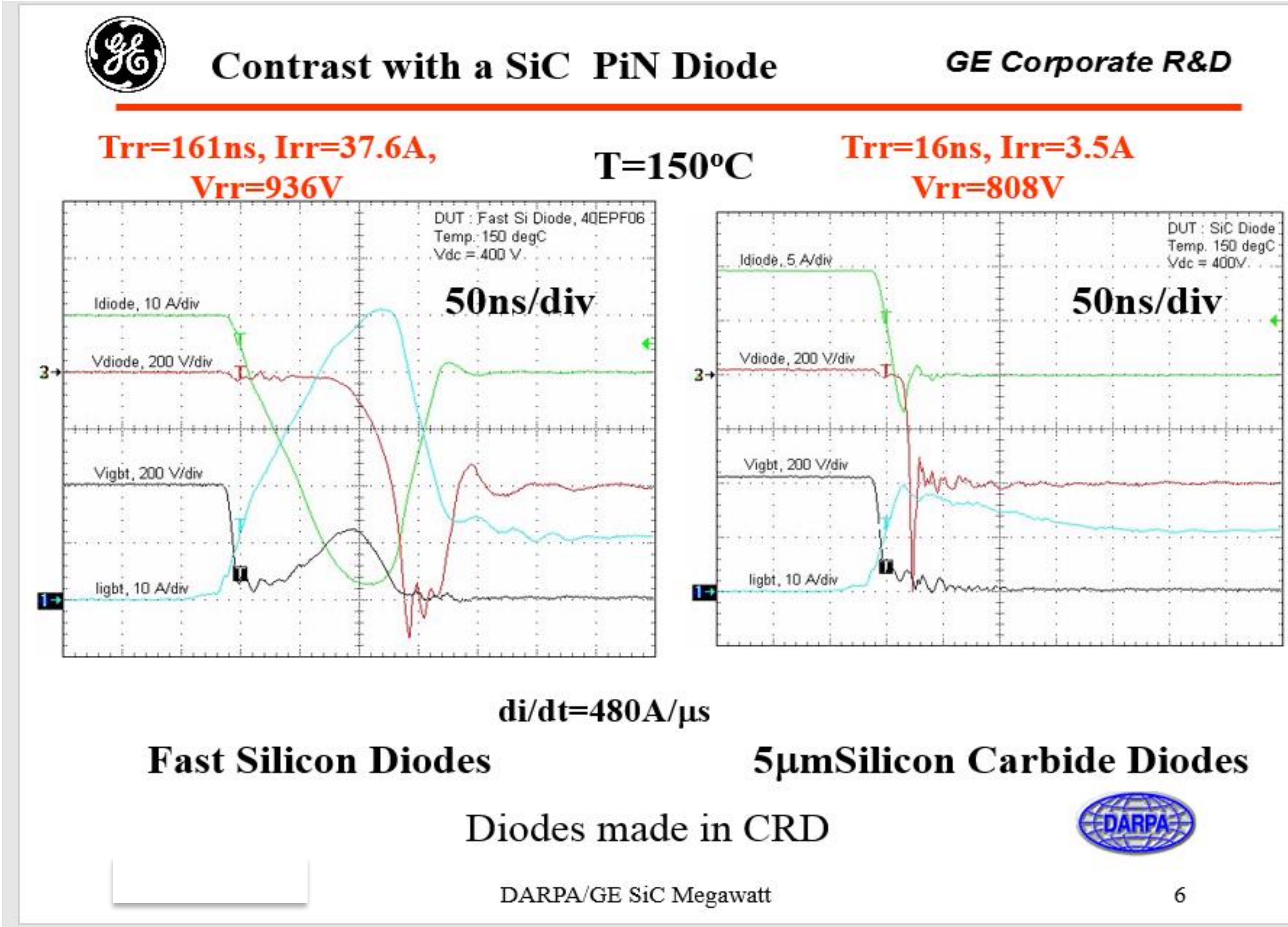
Powerex - ARPA-e



IXYS-ISOPLUS™



A Blast From The Past – Circa 1998

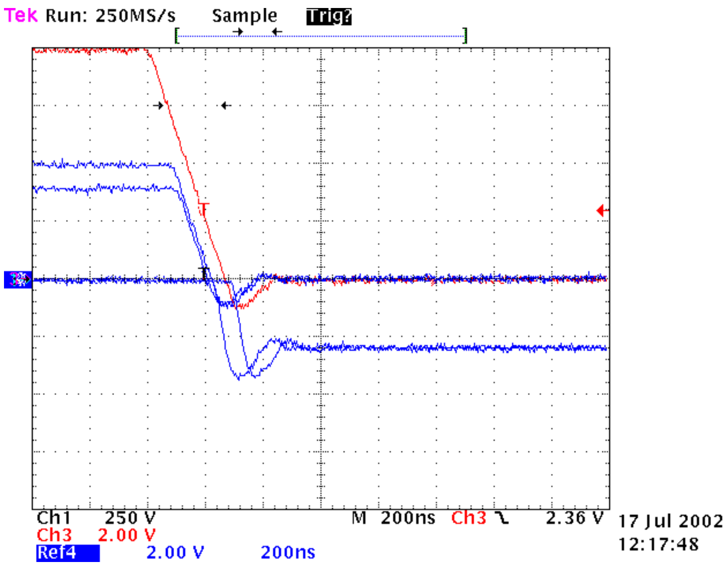


* "**Switching Characteristics of Silicon Carbide Power PiN Diodes,** "Journal of Solid State Electronics, Special Issue on Wide Bandgap Materials, 2000, A. Elasser et al.

Been There, Done That

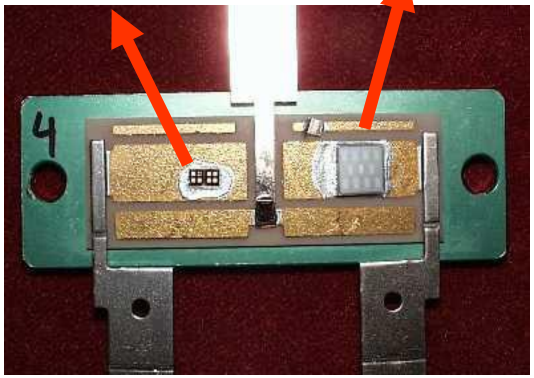
600V, 2x60A SiC Schottky Diode. Circa 2001-2002

Made from a 2" Wafer – Infineon Gen. 1 diodes.



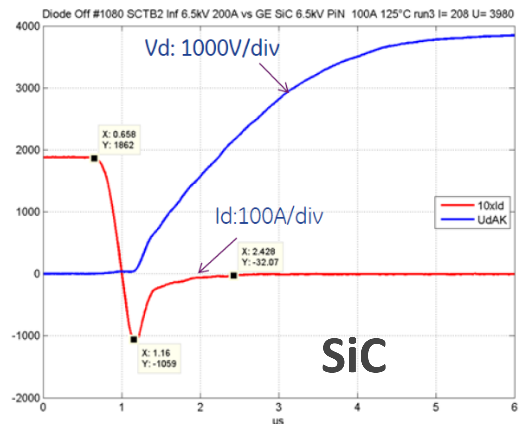
600V, 20A SiC PiN Diodes.

600V, 75A Si IGBTs.

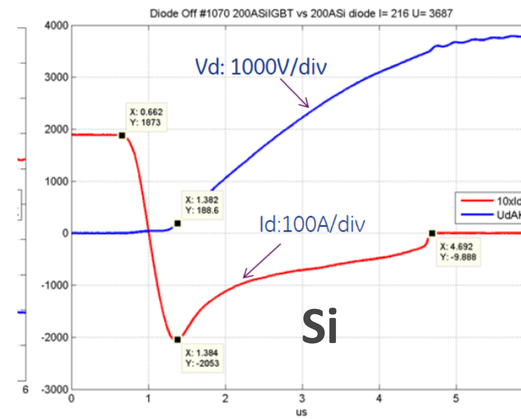


Hybrid Si/SiC Modules From The Late 90s.

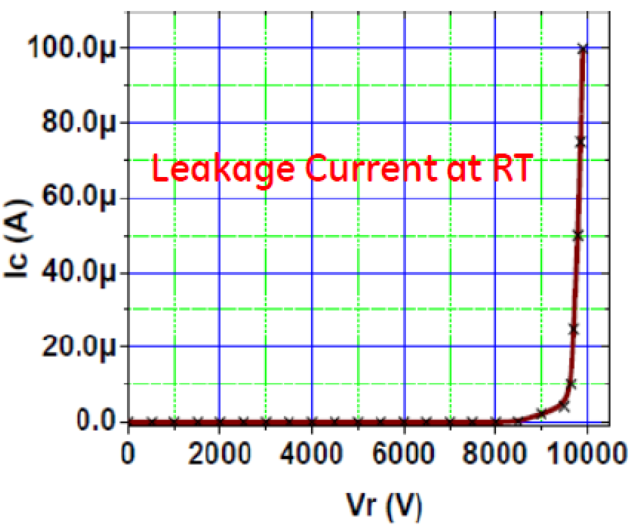
6.5kV SiC PiN Diodes Circa 2010



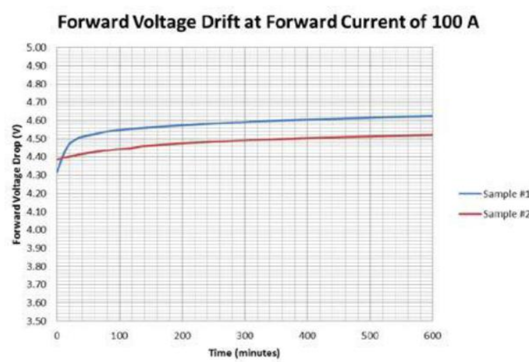
Turn-off, at 125°C



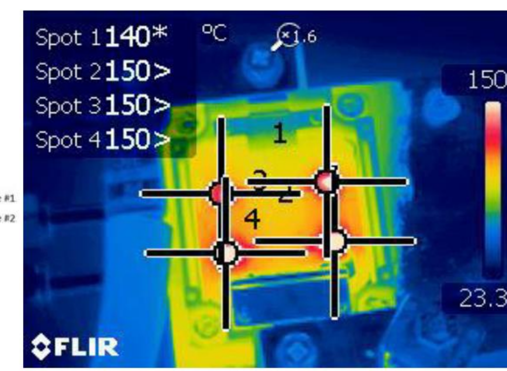
Turn-off, at 125°C



Bipolar Degradation and Current Sharing

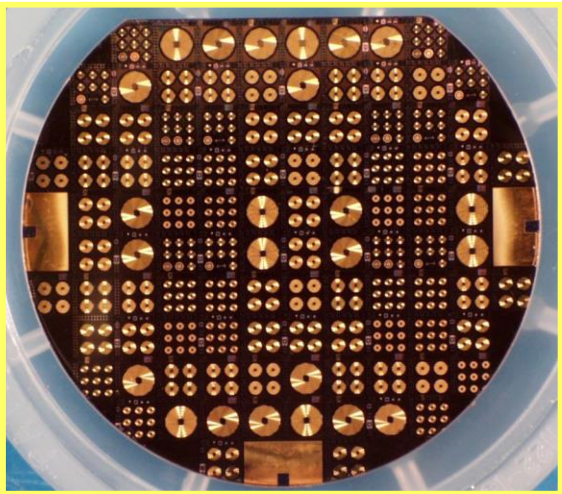


2 samples run for
10 hours- slight increase
in forward drop

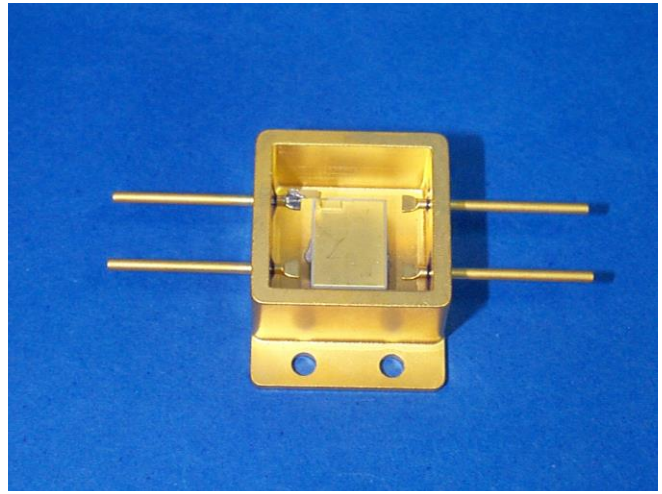


Open Module run at 100A
showing current sharing
amongst the 4 chips

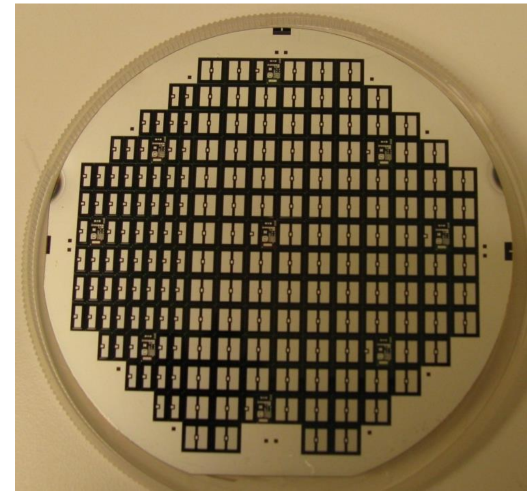
SiC GTOs (1999) & Thyristors (2003)



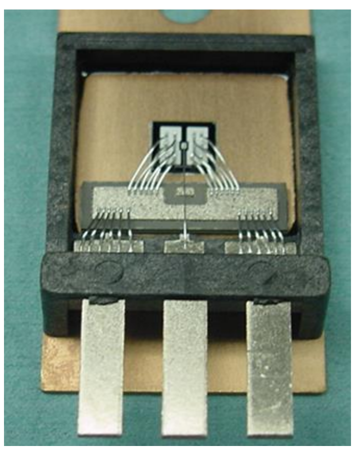
35mm SiC GTO Wafer.



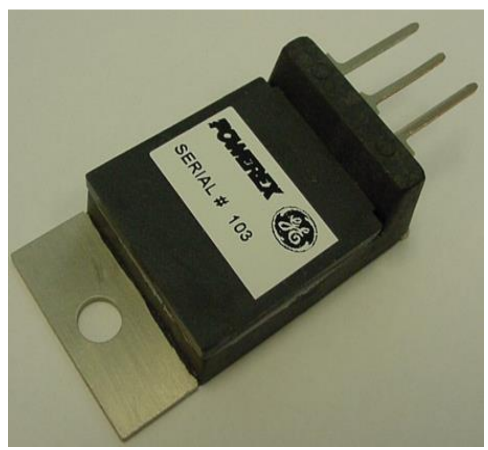
5kV SiC HT GTO package.



4” SiC Thyristor Wafer.



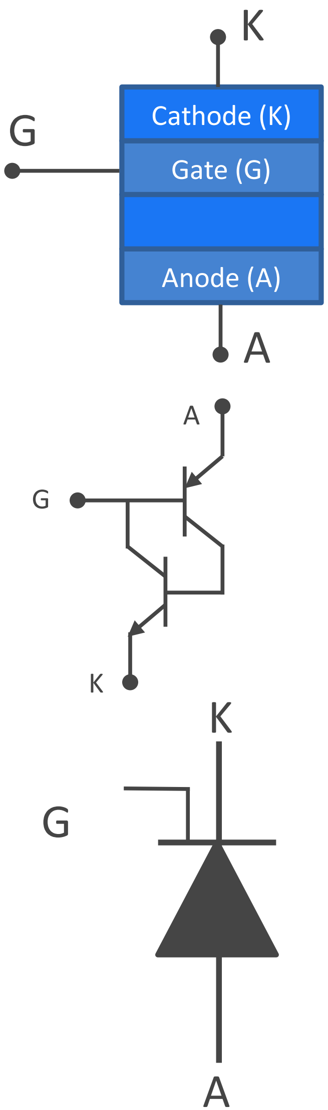
3kV SiC Thyristor



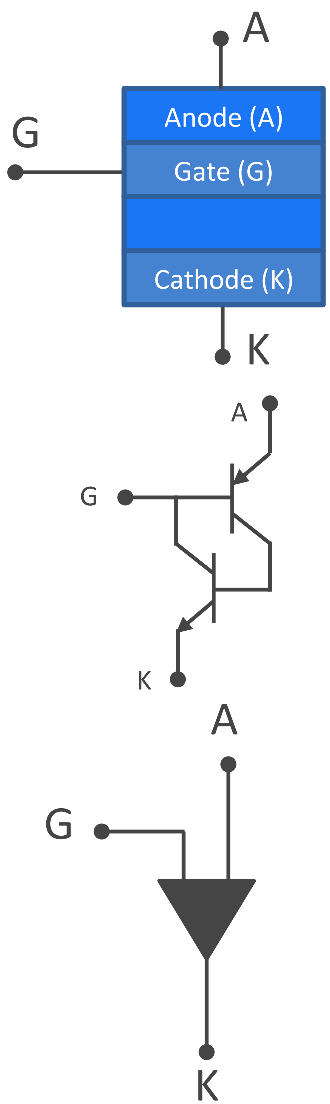
Jumbo TO 247

Powerex QIS HV Packages

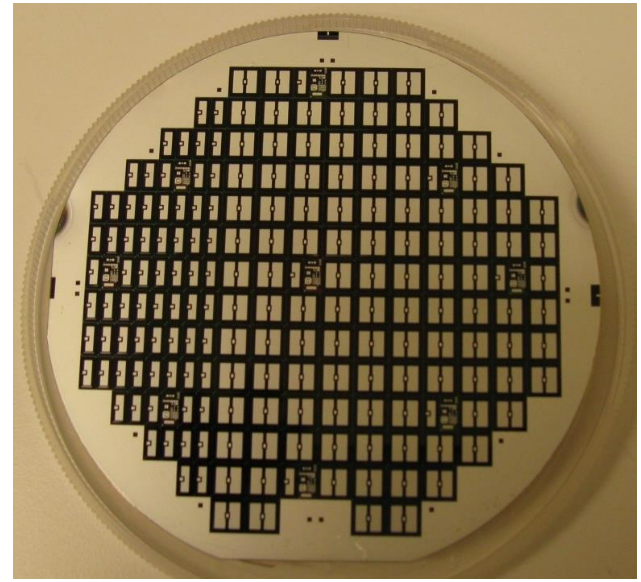
3kV SiC Thyristors



Si

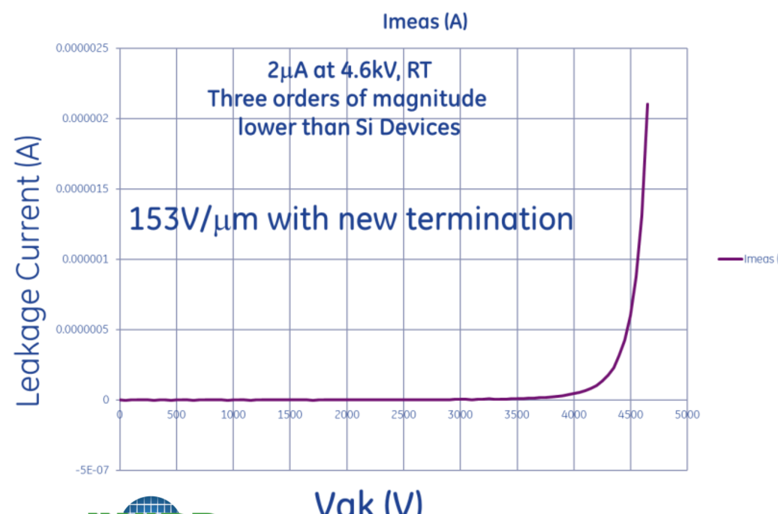


SiC

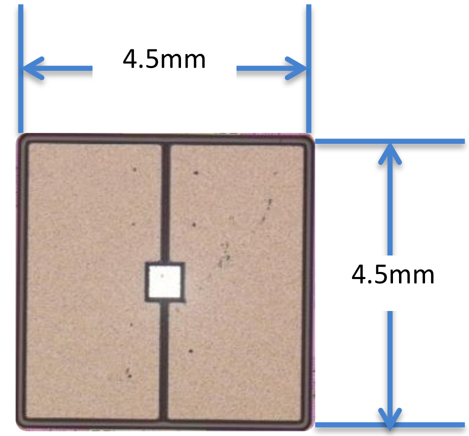


6mmx6mm Chips- 4” Wafer

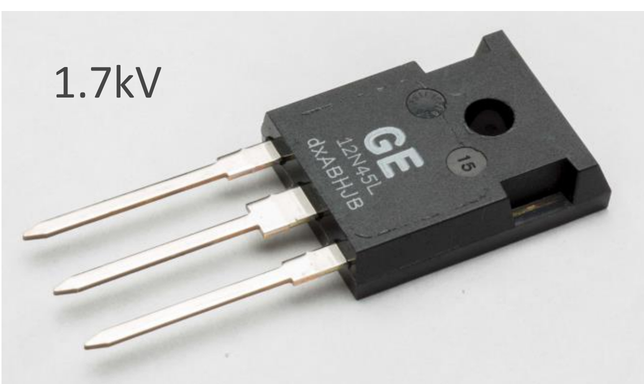
6mmx6mm Forward Blocking Characteristics

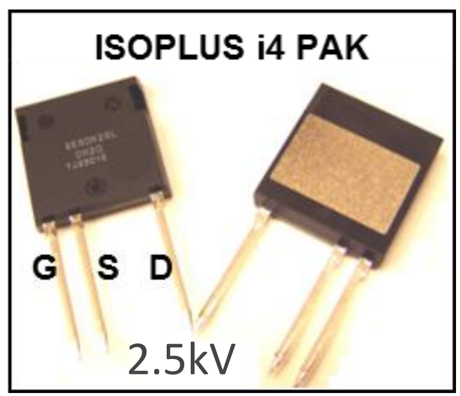


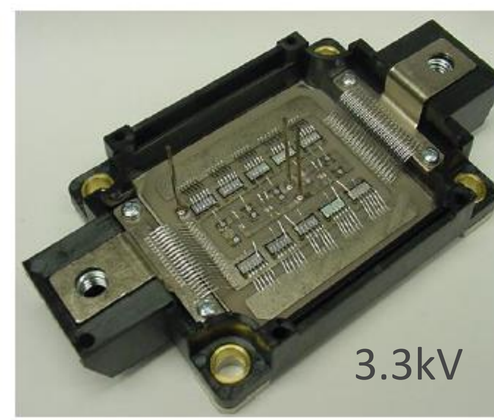
GE SiC MOSFETs: 1.2kV, 1.7kV, 2.5kV, 3.3kV; Discrete and Modules



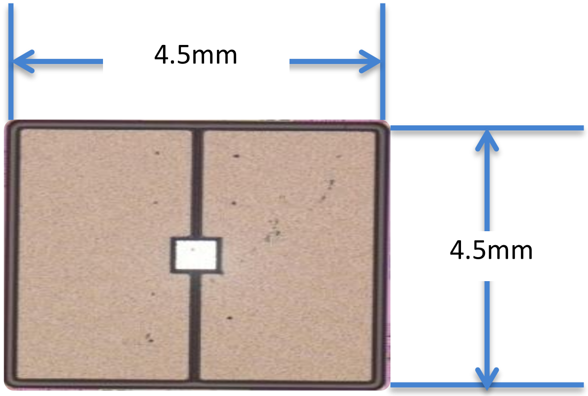
Chip

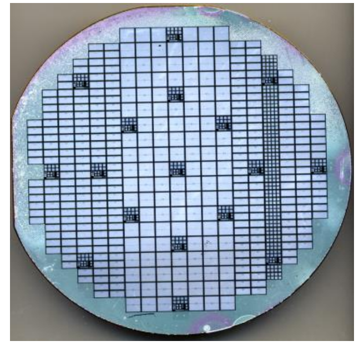


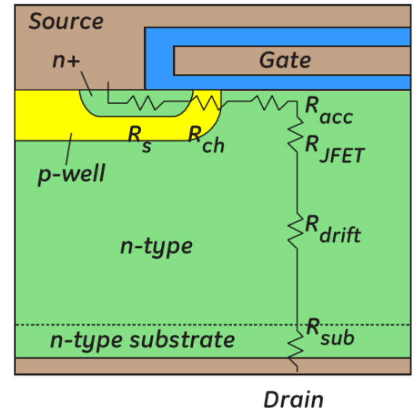




GE SiC MOSFETs



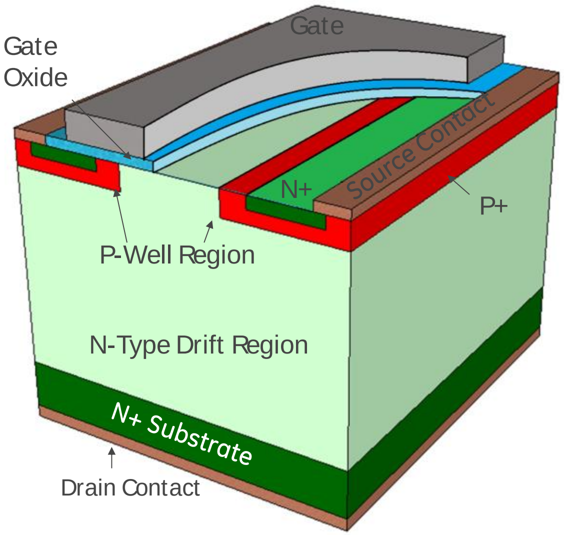




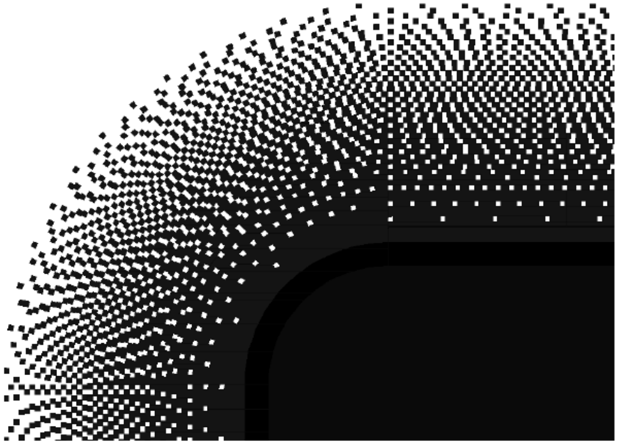
- Graded Junction Terminations.
- Low Rdson.
- 200°C Tj max.
- AECQ101 Qualified.
- 1.2kV, 1.7kV, 2.5kV, and 3.3kV.
- 1.2kV and 1.7kV Modules up to 1200A.
- Less than 5nH Module package inductance.
- High Avalanche Energy (**3J** for 1.2kV and 1.7kV devices- 9J to 15J/cm^2).
- High Short Circuit capability (up to 10µs - recently improved*).
- Optimized process for 4" and 6" wafers.
- High Oxide Reliability.
- Small voltage threshold drift.
- Tested for NBTI and PBTI.

* "Optimization of 1700V SiC MOSFET for Short Circuit Ruggedness," A. Bolotnikov et al. ECSCRM 2018.

GE SiC MOSFETs: Device Structure, Terminations, Reliability Data, Qualification.



Device Structure.



Graded JTE.

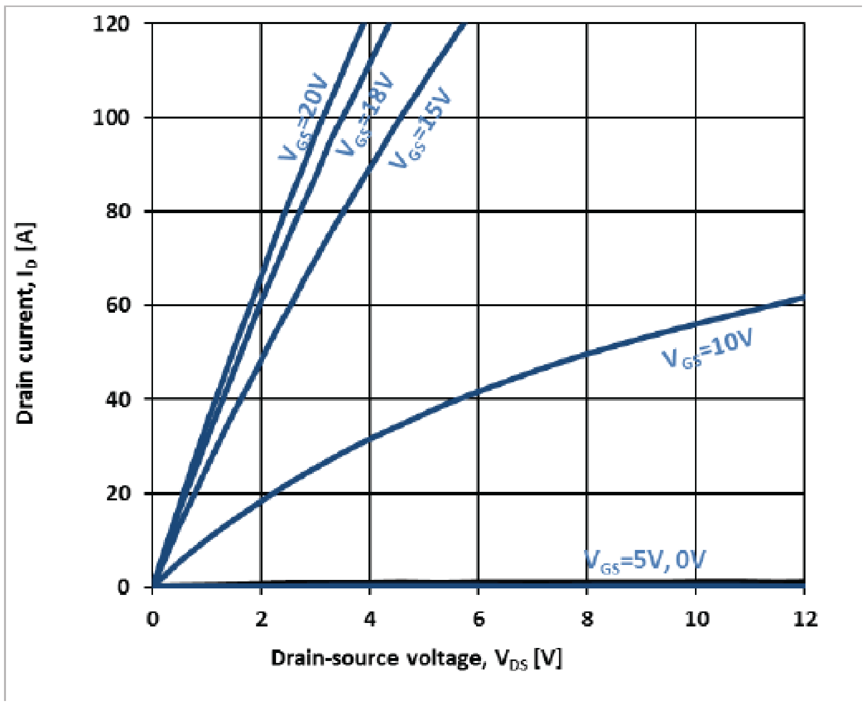
ISO 9001 Certified in 2014.

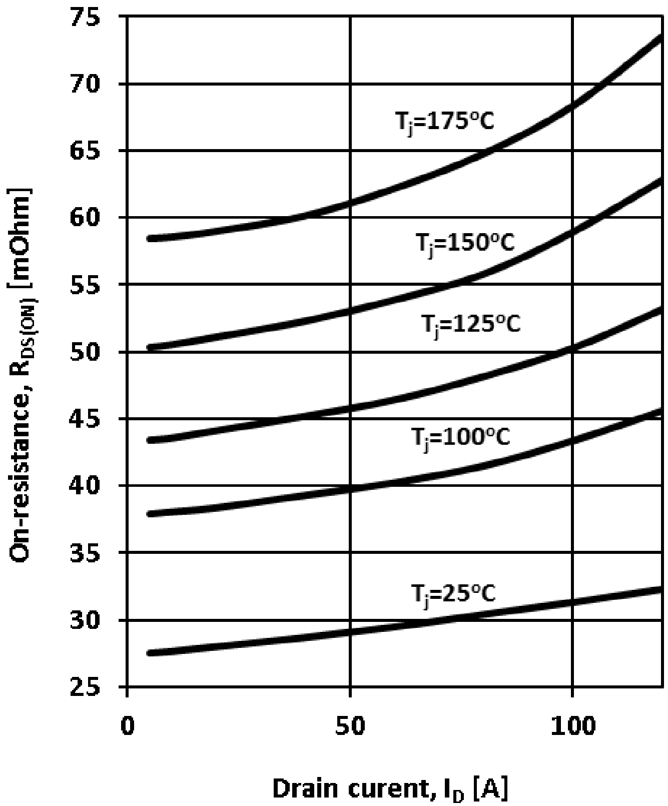
HTGB: 1000 hr, 200ºC, V_{GS}=23V:
✔ passed

HTRB: 1000 hr, 200ºC, V_{DS}=960V:
✔ passed

1000 temp. cycles (-55 to +200ºC):
✔ passed

1.7KV, 70A @ 25ºC, 29mΩ.

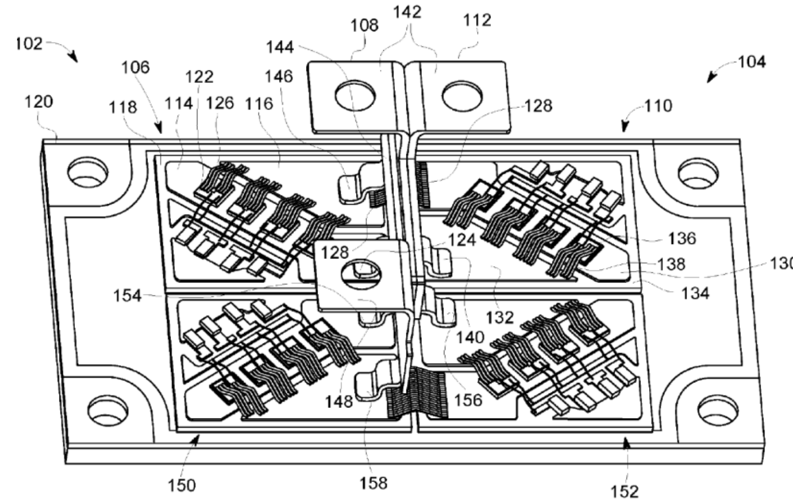




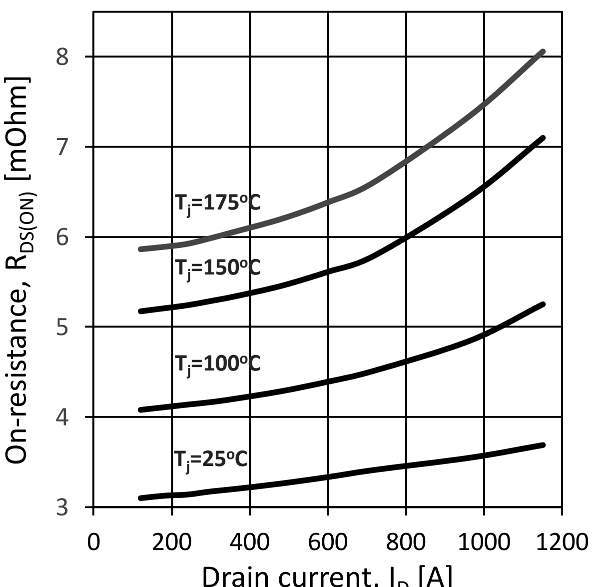
- Chip size: 4.5mm x 4.5mm (20.25mm²)
- 70A Rated @ T_C=25ºC
- T_{J_MAX} = 175ºC (package limited)
- $R_{DS,On}$=29mΩ @(70A, T_J=25ºC), 54mΩ @150ºC
- Normally-off w/ avalanche limited BV @2150V

Rdson vs. Temperature →
Positive Temp. Coefficient →
Ease of paralleling.

Silicon Carbide Modules

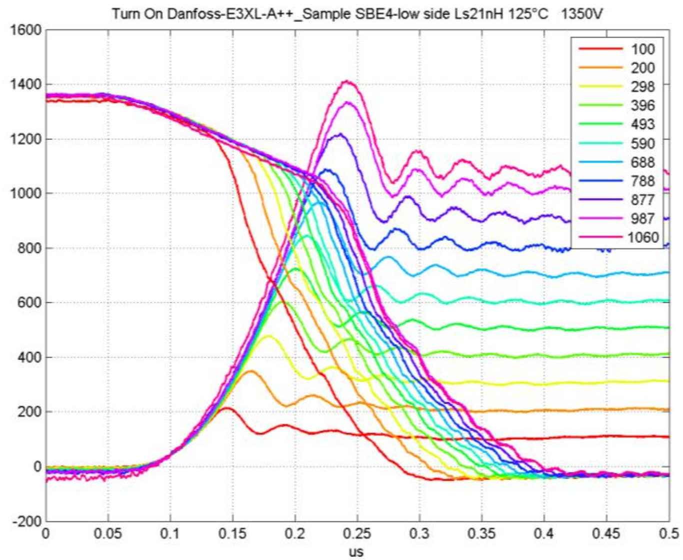


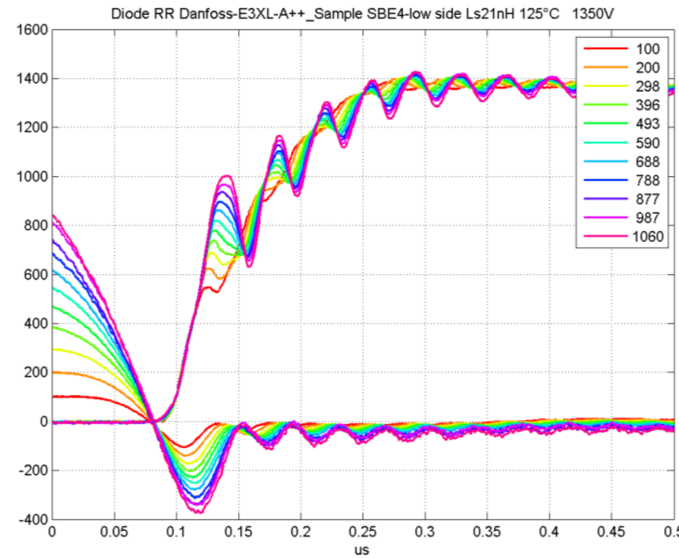
Low Inductance Package
US Patent#: 9,972,569



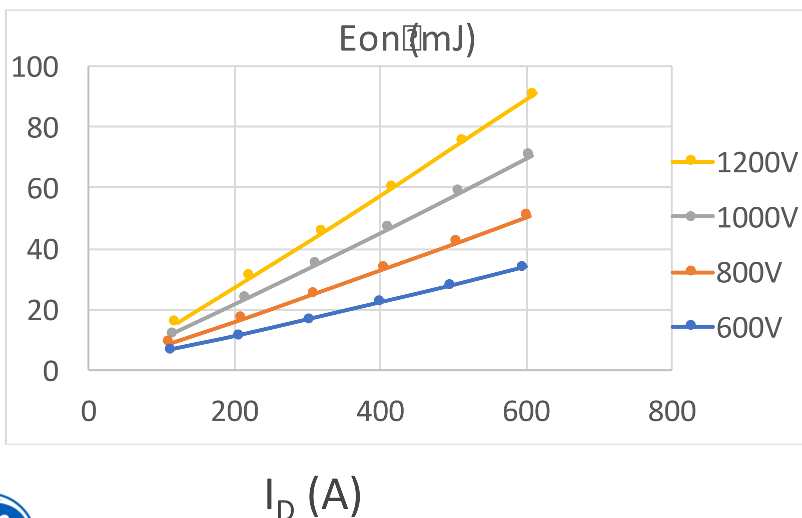
- 1.2kV & 1.7kV, up to 600A, Tj-max =175°C.
- Compatible with E3-style footprint.
- 12 MOSFET chips per switch.
- Designed for low inductance: 4.5nH.
- Body diode + 3Q MOSFET for low cond. Losses.
- Embedded temperature sensors (NTC).

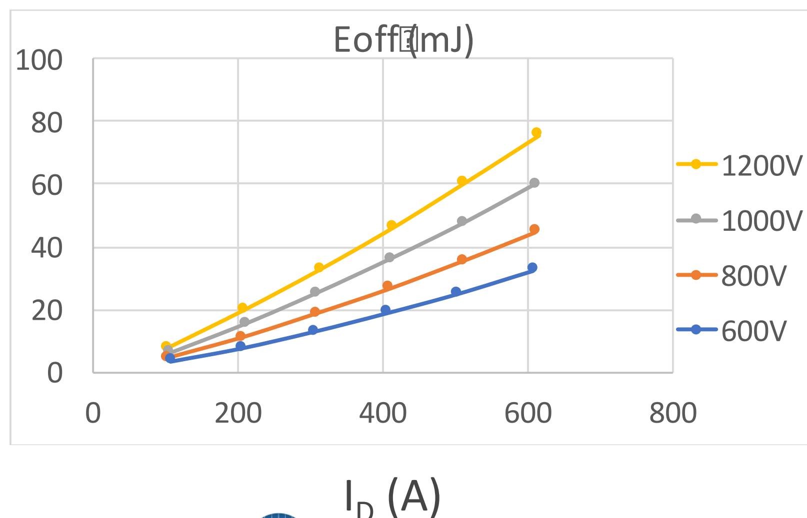
1.7kV Modules Switching (Phase Leg)





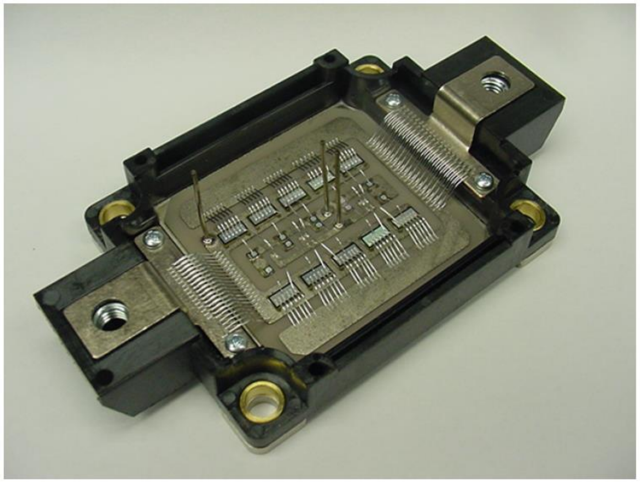
Vgs=20V, Rgon=5.58Ω, Rgoff=4.6Ω.



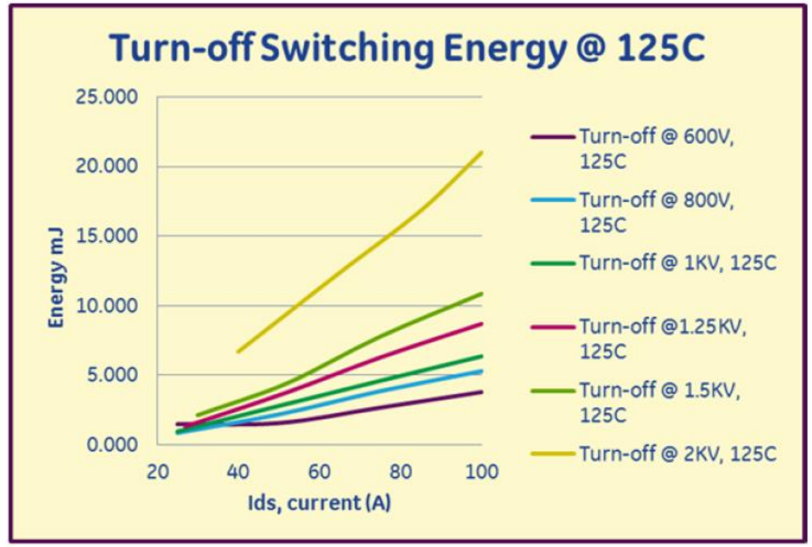


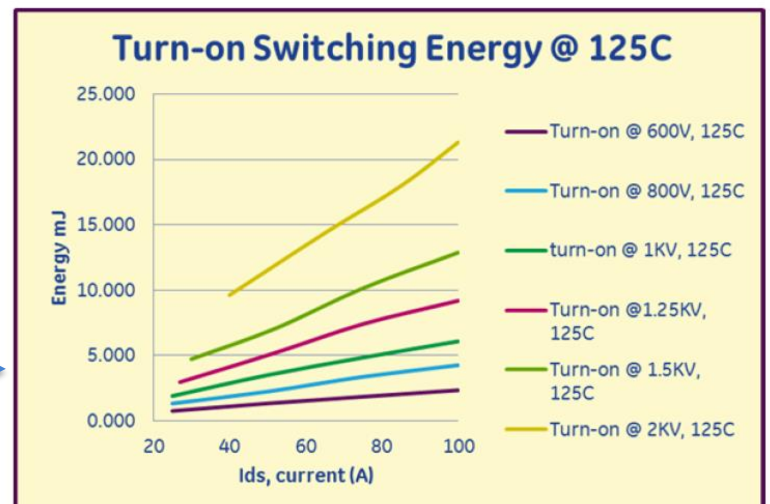
GE Public

2.5kV, 3.3kV SiC MOSFETs



3.3kV, 120A SiC MOSFET Module.





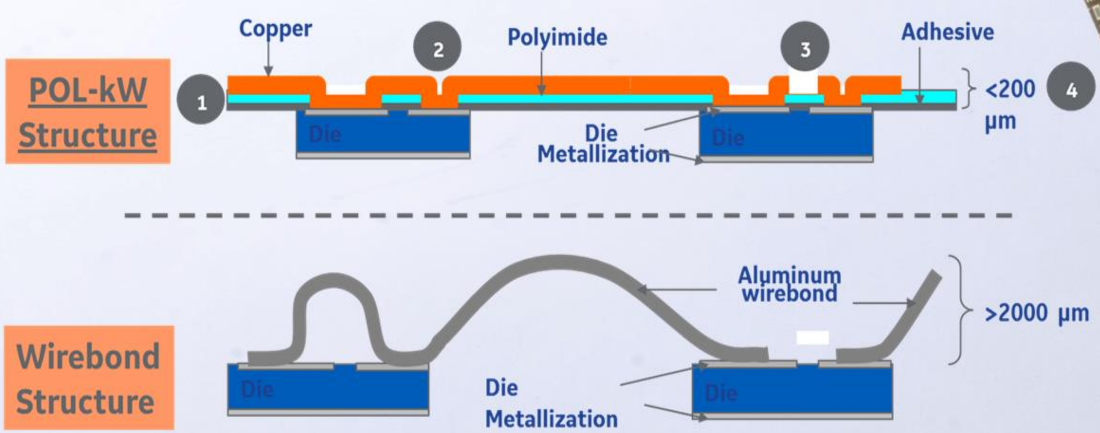
3.3kV, 120A SiC MOSFET Module Turn-off Switching Losses @ 125^{o}C, Rg =5Ω.
3.3kV, 120A SiC MOSFET Module Turn-on switching losses @ 125^{o}C, Rg =5Ω.

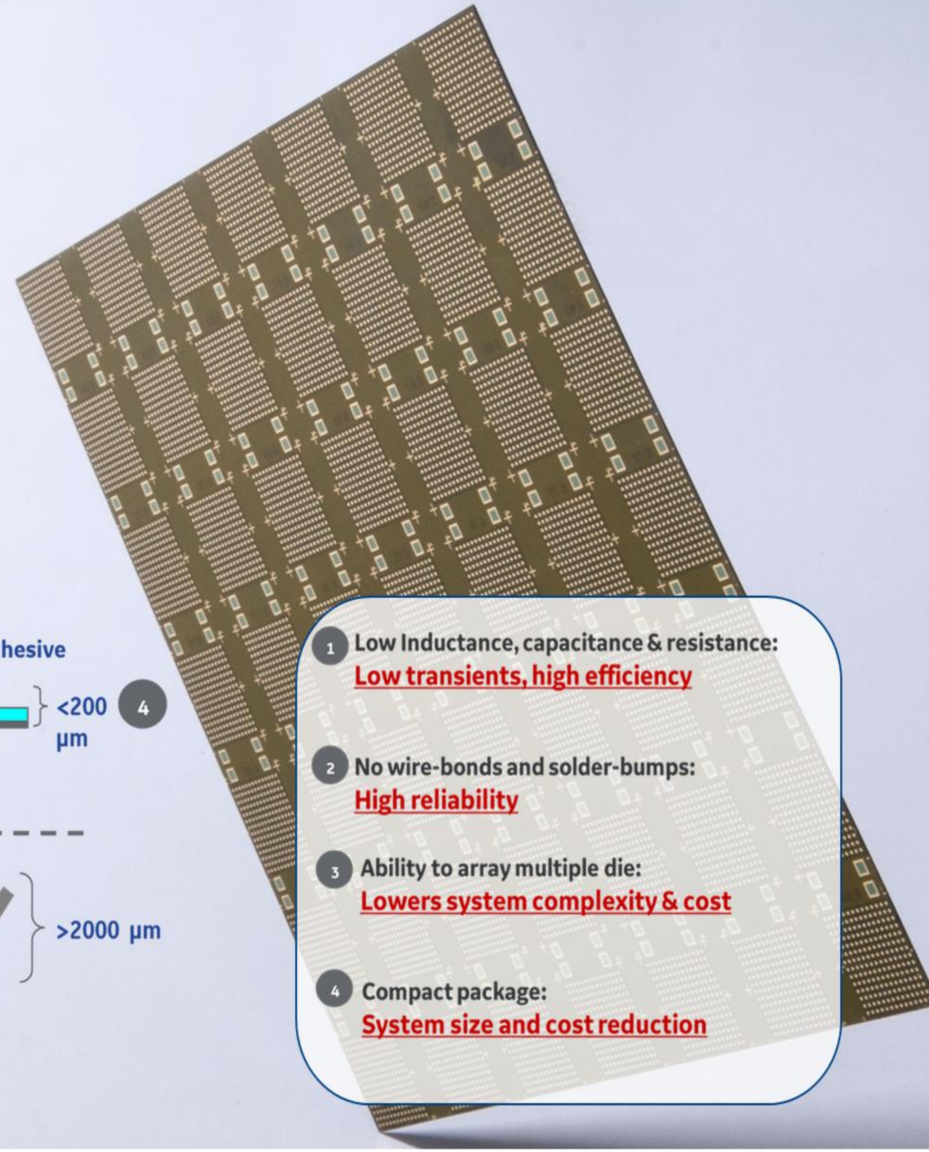
Next Generation Packaging & High Voltage SiC MOSFETs

GE POL Packaging Technology

Power Overlay (POL) technology

- *Unique packaging technology* **Combining flex, PCB and wafer level processes** *to improve device miniaturization and performance*
- **Wire bondless and Solderless Direct pad interconnect** High quality / control in microvia and patterning
- *Ideal for high power density applications*





1. Low Inductance, capacitance & resistance: **Low transients, high efficiency**
2. No wire-bonds and solder-bumps: **High reliability**
3. Ability to array multiple die: **Lowers system complexity & cost**
4. Compact package: **System size and cost reduction**

GE POL Products Portfolio

GEAS SiC MOSFET POL Module Portfolio

600A, 1200V
½ bridge HTMP

400A - ½ bridge

200A, 1200V Dual

1600A, 1200V
½ bridge

250A, 1700V – 6 pack

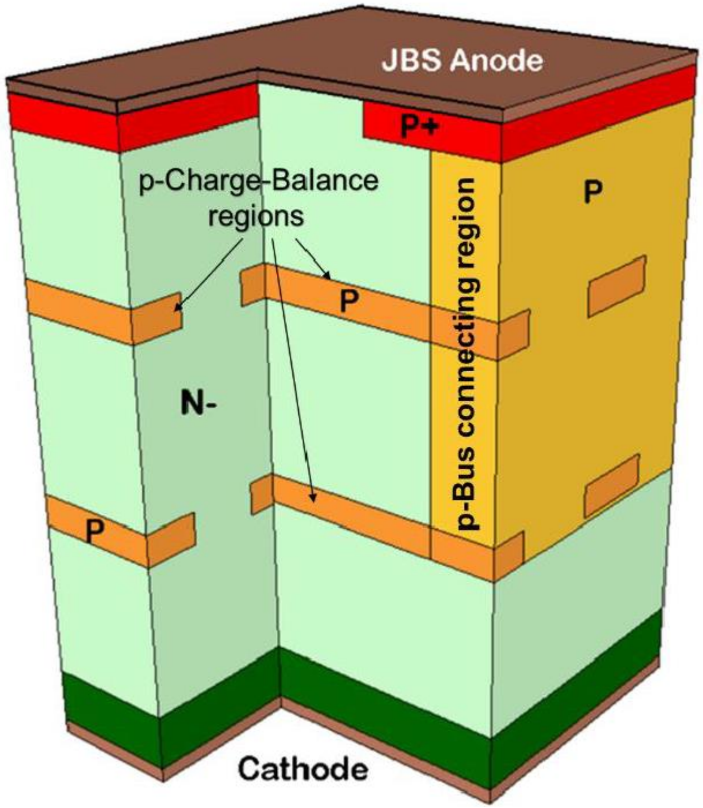
250A, 1700V - Dual

300A, 1200V
3 Channel SSPC

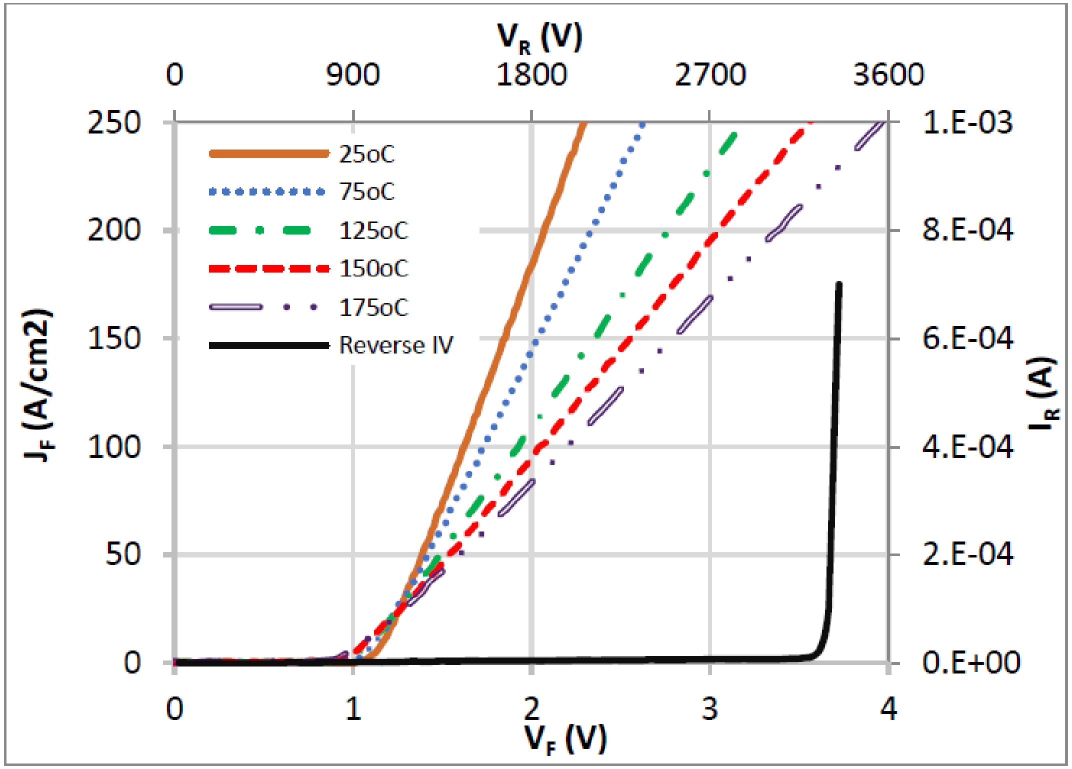
NPI offerings from GEAS using POL
Higher power density
Higher operation temp.
Less loss and voltage overshoot
Less weight
200C Junction temp operation

https://www.geaviation.com/sites/default/files/Silicon-Carbide-Power-Modules.pdf

Charge Balance JBS Diodes



Schematic of SiC CB-JBS diode depicting p-Charge Balance and p-Connecting regions.

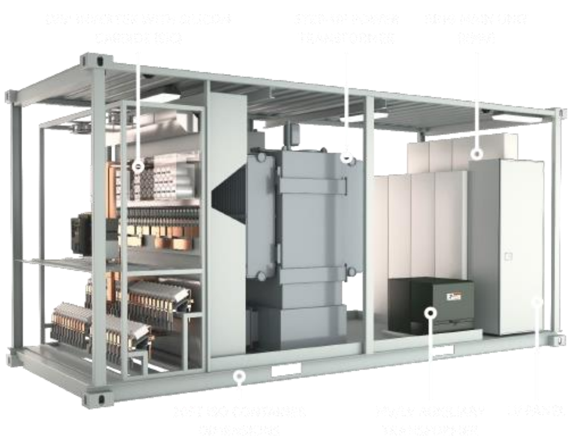


Forward and Blocking I-V characteristics of 3kV SiC CB-JBS diode.

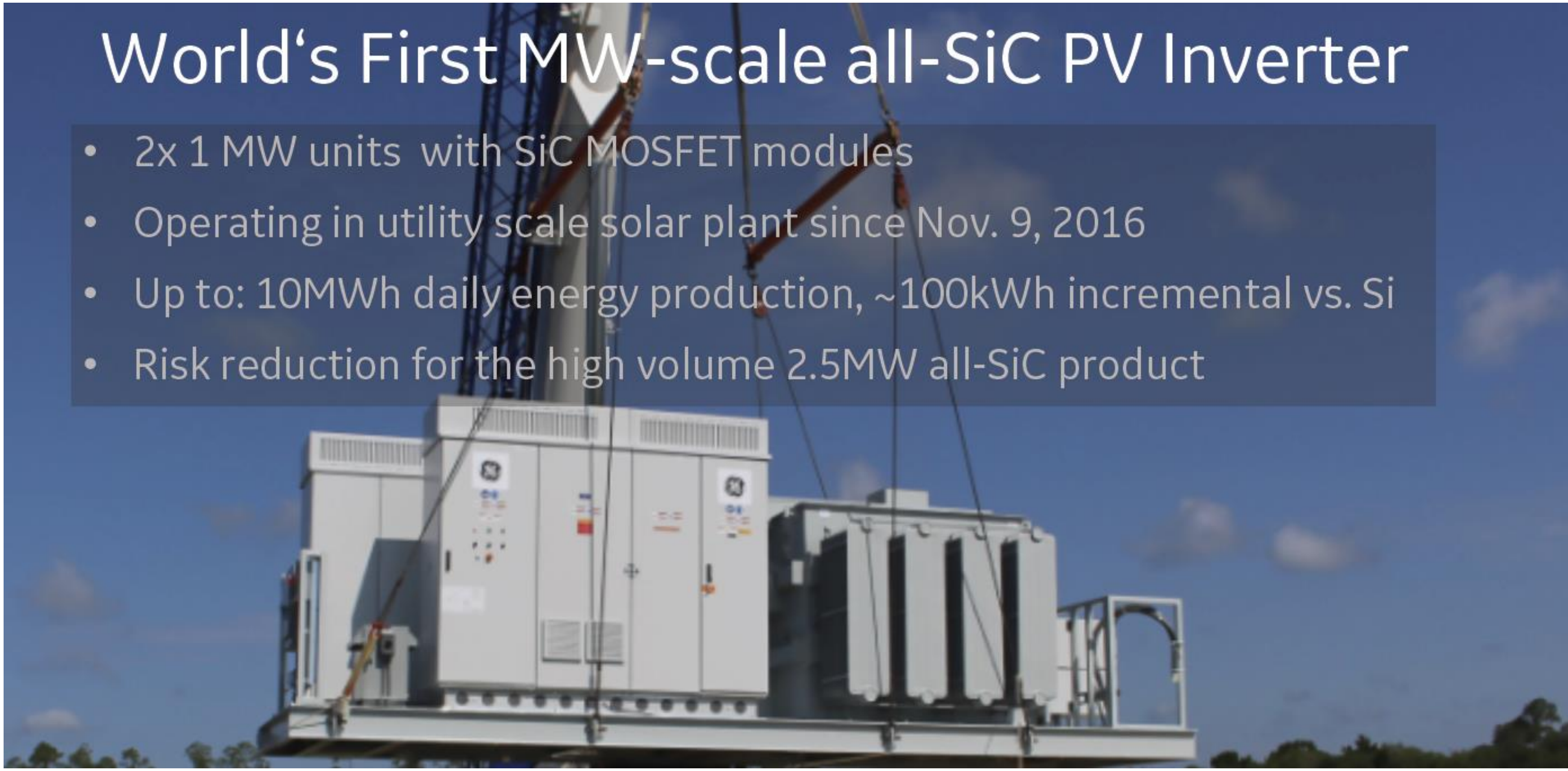
* A. Bolotnikov et al. "SiC Charge-Balanced Devices Offering Breakthrough Performance Surpassing the 1-D Ron versus BV Limit," ECSCRM 2018.

GE Silicon Carbide Applications

- 1MW, 1500V Solar PV Inverter.
- 1MW Wind Converter for 3MW DFIG Machines.
- 1MW NASA Hybrid Flight Converter.
- Numerous Aviation Applications.
- 3MVA MR Gradient Amplifiers.
- Energy Storage DC/DC Buck Boost Converters.



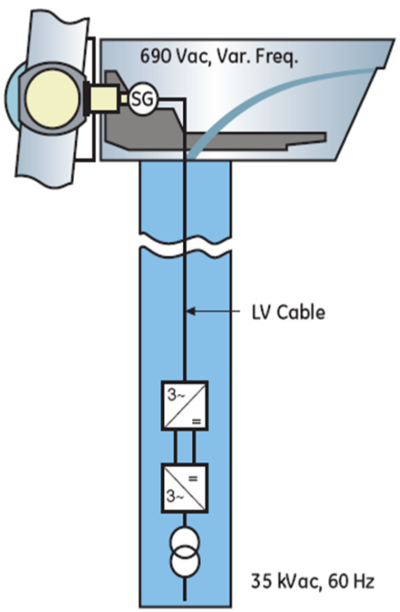
1MW SiC Solar Inverter



- 1.7kV, SiC MOSFET Power Devices.
- 2-level topology, air cooled.
- 3x parallel modules sharing single gate drive unit.

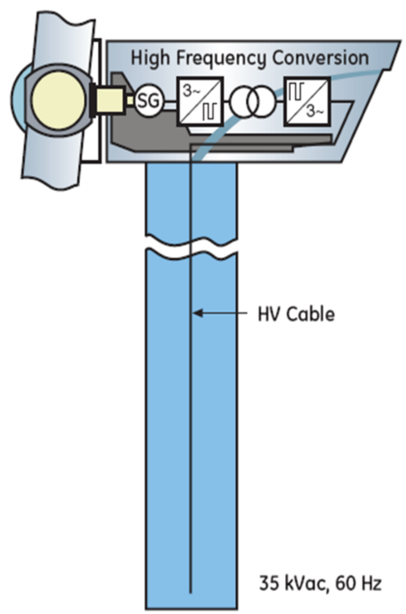
1MW SiC Wind DFIG Converter For 3MW DFIG Machines

Solid-State Transformer For Wind Power Conversion



Current Configuration

- Down-tower converters + transformer
- Heavy/expensive LV cables

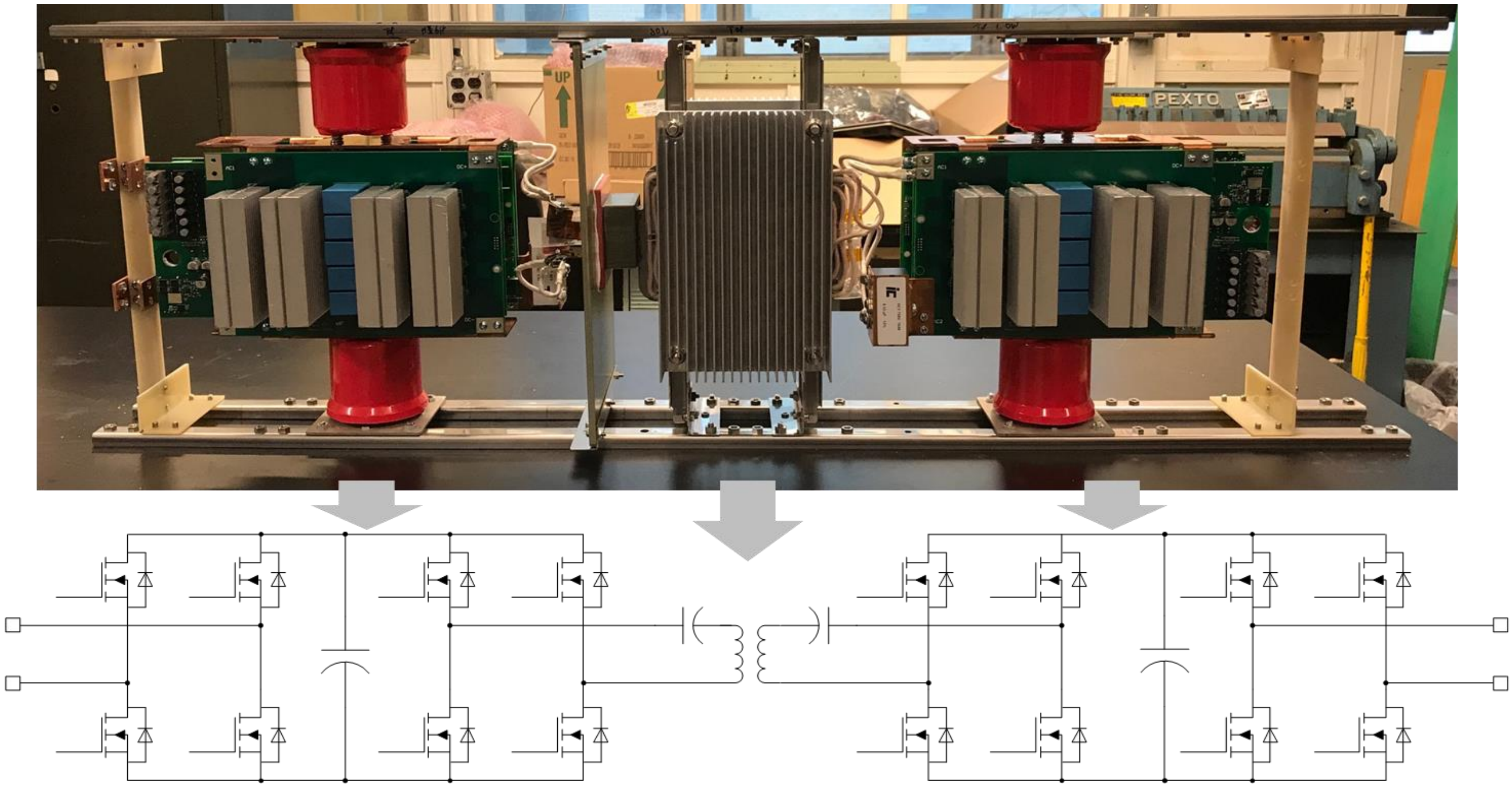


Improved Configuration

- Up-tower converters with integrated HF step up
- Lighter/ cheaper HV cables

** Funded by the US the Department of Energy - DOE Grant No. DE-EE0007252 for the work presented in this paper.

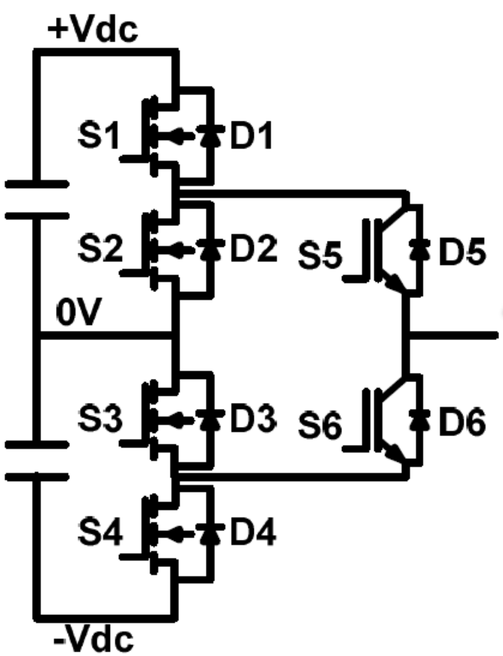
Solid-State Transformer SiC Wind Power Electronics Building Block

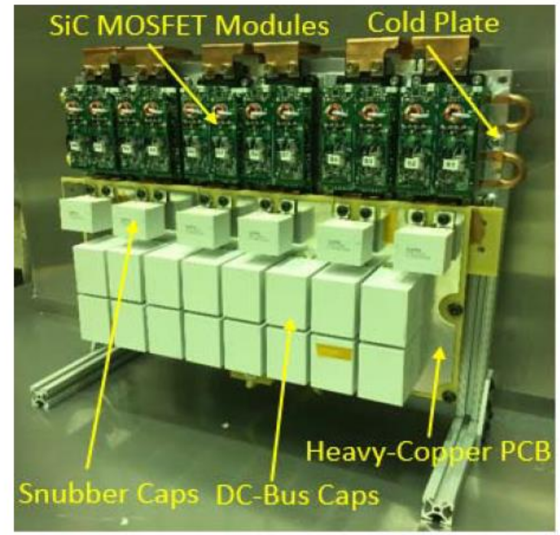


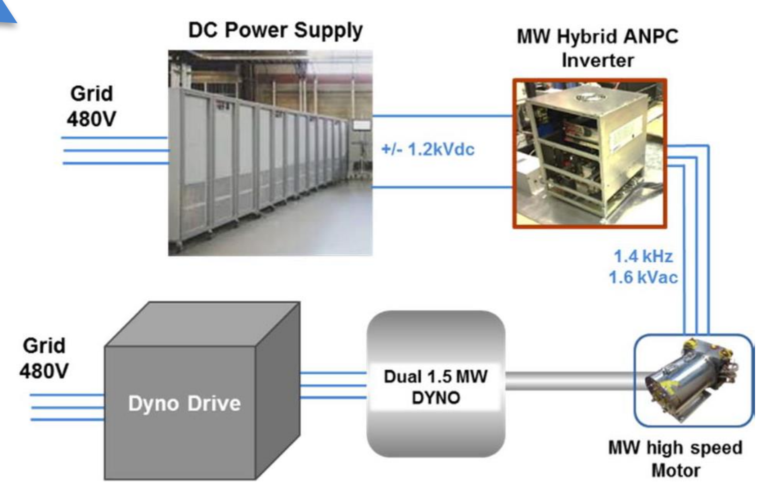
- 690 VAC / 1000 VDC on primary and secondary sides, 175 kHz transformer
- 40kW – 150 kW Building Blocks depending on partial/fully populated boards

** Funded by the US the Department of Energy - DOE Grant No. DE-EE0007252 for the work presented in this paper.

Hybrid Flight Converter Topology





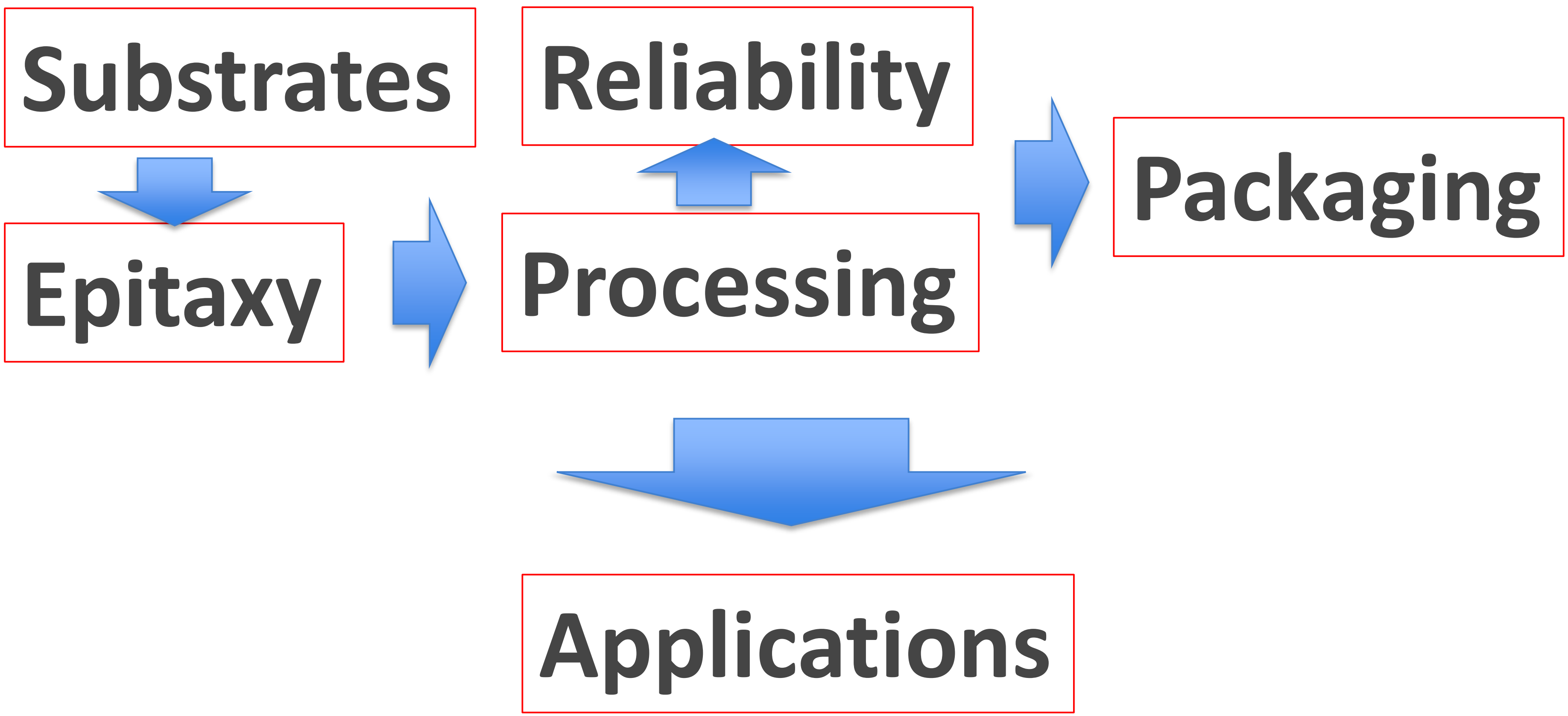


Hybrid Three-Level ANPC Inverter for Aircraft Hybrid-Electric Propulsion Systems.

@1MW, η of 99%, 98kg Weight, 12kVA/kg density.

** Funded by the U.S. National Aeronautics and Space Administration (NASA)
and the Department of Energy (DOE) supported- (NASA Grant No. NNC15CA29C and DOE Grant No. DE-EE0007252) for the work presented in this paper.

Silicon Carbide Challenges



SiC Carbide Devices Grand Challenges

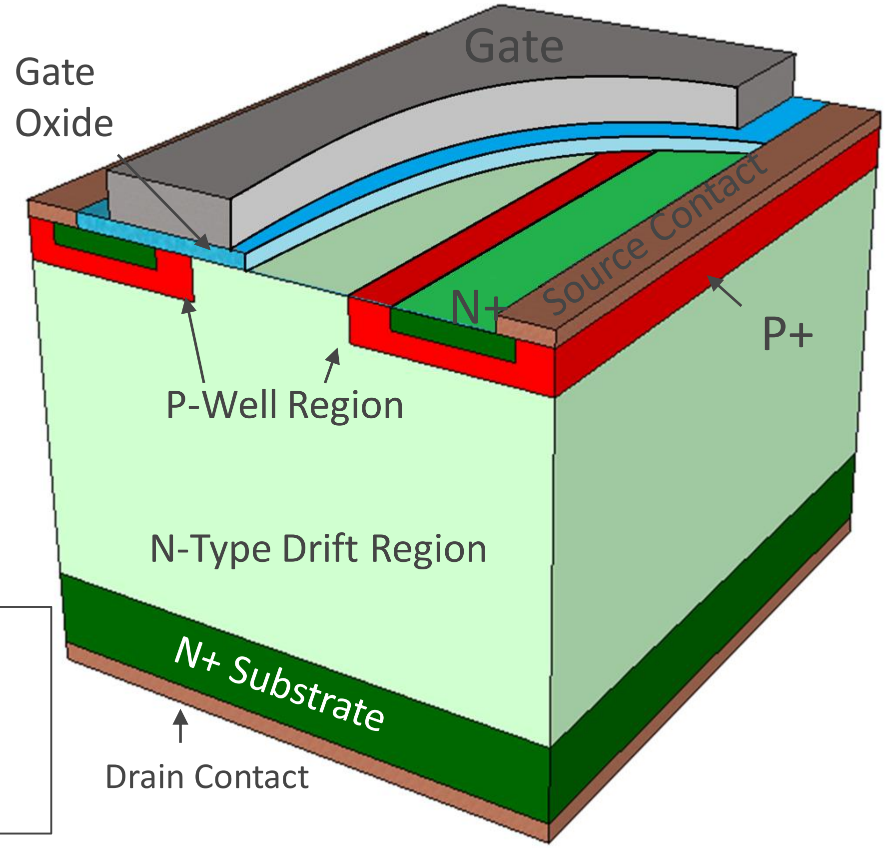
Challenge 1: Substrates & Material Defects.

Challenge 2: Epitaxy, Uniformity, Thickness, Lightly Doped P-Type.

Challenge 3: Long Term Reliability.

Challenge 4: High Electric Field Mitigation – Terminations, Passivation, Testing, Packaging.

Challenge 5: Module Packaging, Gel, Wirebonds Inductance.



Challenge 9: Carrier Lifetime.

Challenge 8: Bipolar Degradation.

Challenge 7: Processing Knowledge at High Temperature, Ion Implantation, Deep Etching.

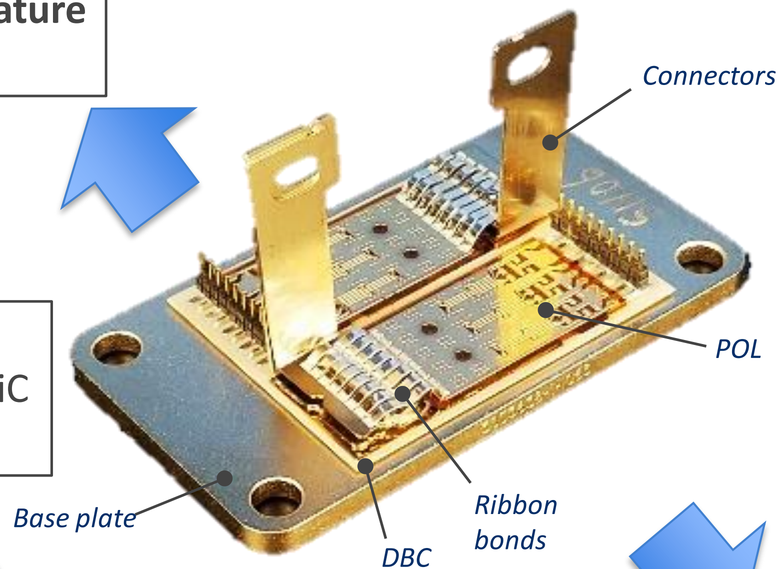
Challenge 6: Low Channel Mobility → oxide interface issues, charge traps, SiO2 quality, etc.

SiC Has Come a Long Way….But There are Still Challenges to Tackle

SiC Carbide Packaging Challenges

Challenge 4: **Cosmic Radiation – Need Packages to Operate at High Altitudes (e.g. nHPD^2).**

Challenge 1: **High Temperature Operation- Beyond 175^{o}C.**



Challenge 2: High Voltage Packages - Need to fulfill SiC Entitlement.

Challenge 5: High Reliability Required to use SiC in Demanding Applications.

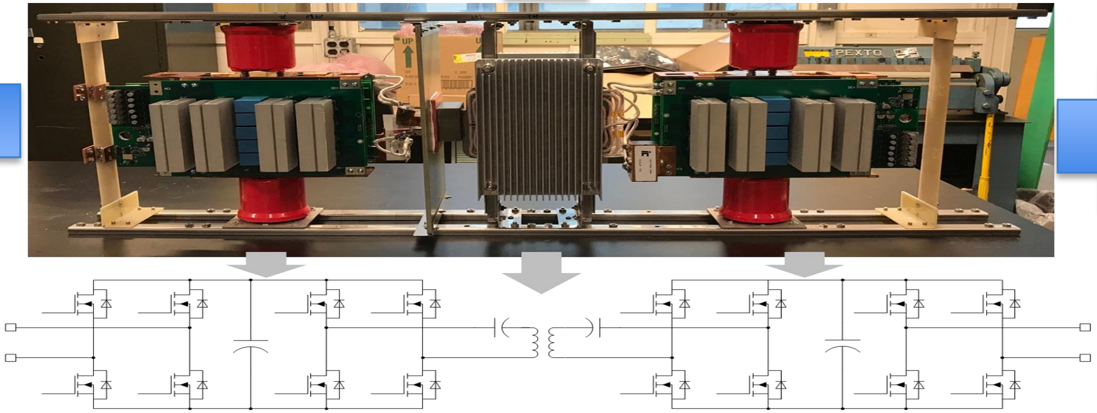
Challenge 6: **Fail Safe Modules – Need Failure Contained Packages.**

Challenge 3: **Low Inductance packages for high frequency applications. (e.g. POL, LinPak,…).**

SiC Carbide Converters' Challenges

Challenge 1: Cost – There is still a lot of room for improvement.

Challenge 2:
Short Circuit Ruggedness – Need to Match or surpass IGBTs.
EMI Mitigation, Robust Gate Drives, etc.



Challenge 4: Lack of Bipolar Devices such as PiN Diodes, Thyristors etc.. – needed for Pulse Power Applications

Challenge 3: Meet HV, HT, HF Entitlements, Rest of Components Need to Follow: Chips, Packages, Gate Drives, Passives, Controls, etc.

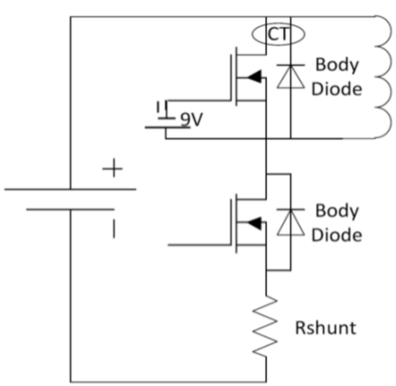
Thank You For your Attention, Questions?

Merci de Vôtre Attention, Questions?

Appendix

1.7kV Modules Paralleling

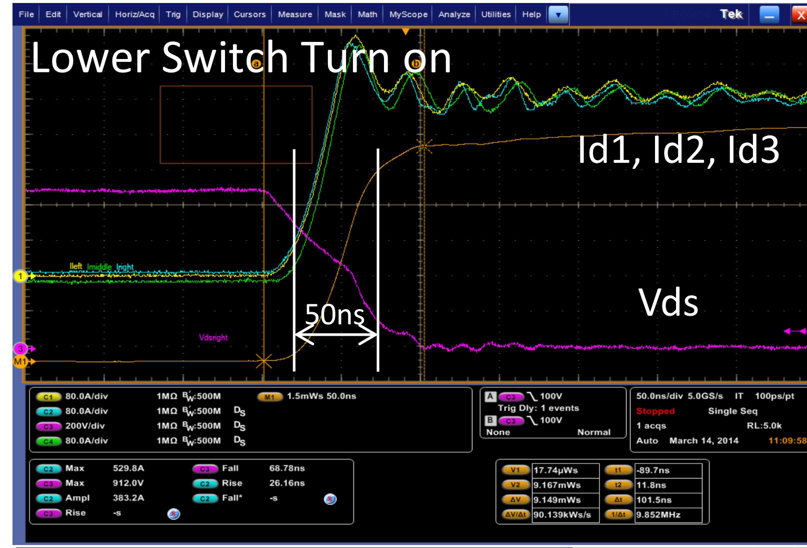
3 modules in parallel @ 900V, 1200A

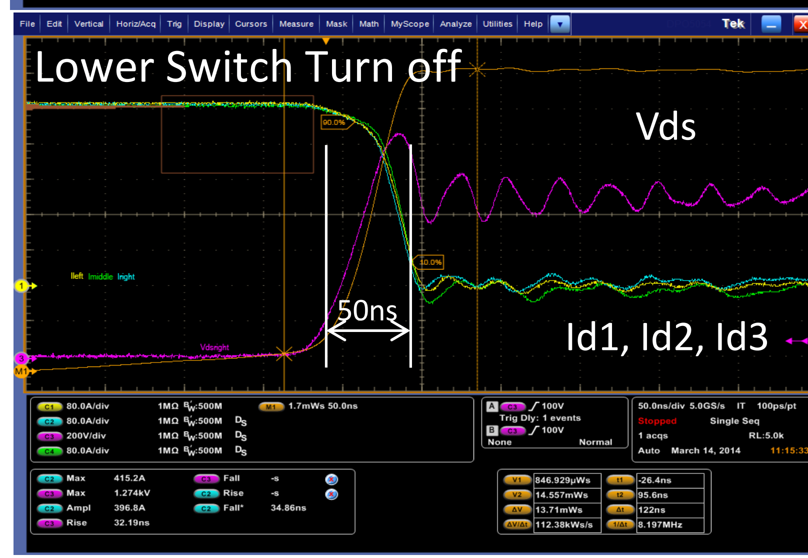


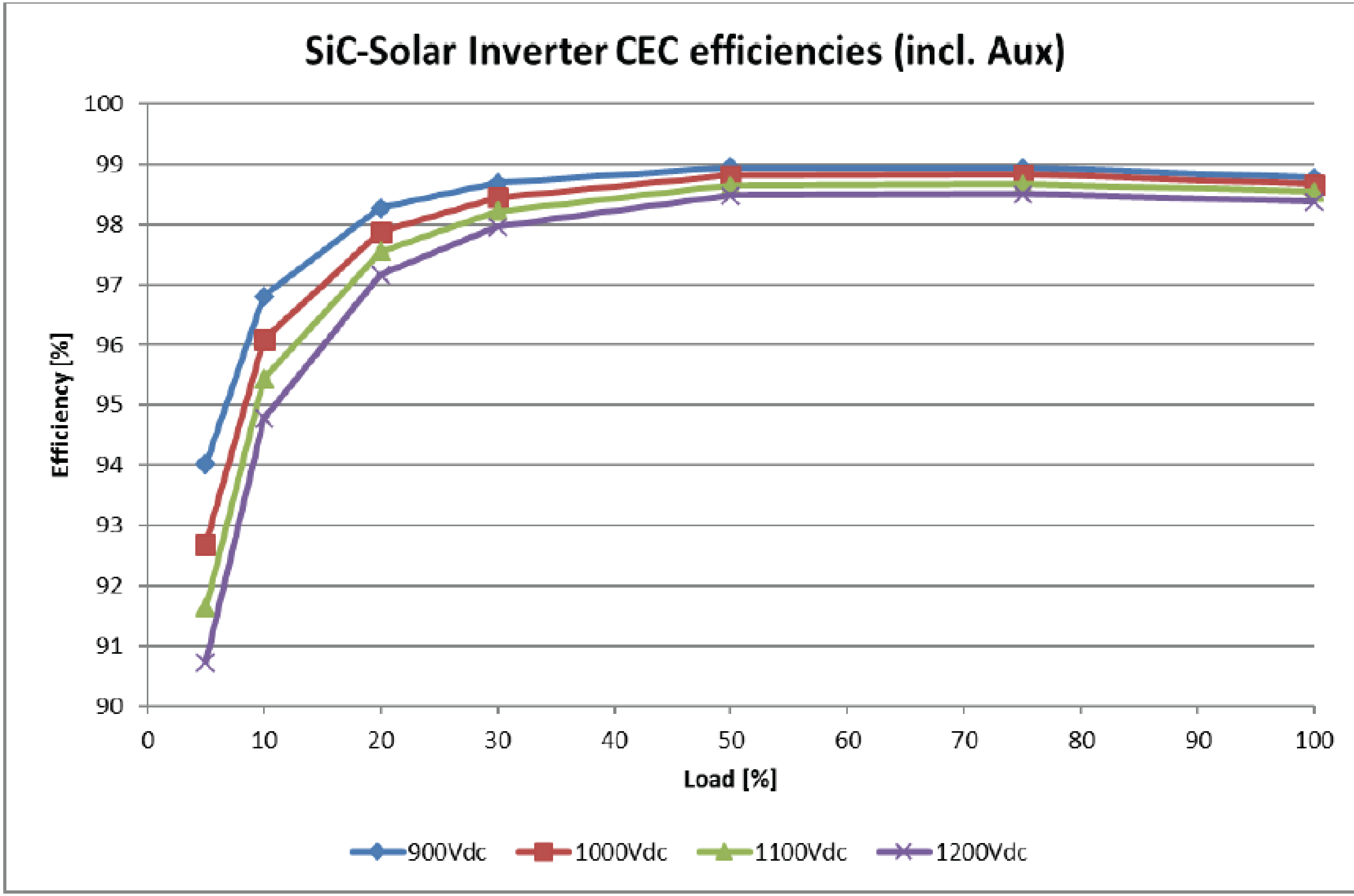
- ☑ Static and dynamic current sharing → no scalability issues
- ☑ Using body diode → improve current density
- ☑ Fast switching with low overshoots

Switching Losses <1/10th Equivalent Si IGBT

Double Pulse Inductive Testing







Converter efficiency, early prototype to validate SiC entitlement (AC reactor core losses high / not optimized for 8kHz)

GE High Voltage SiC Super Junction Transistor

GE Research Awarded $3 MM ARPA-E Project to Develop World's 1st High-Voltage Silicon Carbide Super Junction Transistor for Next Generation Grid Solutions.

- Will achieve 10X reduction in power losses compared to conventional silicon insulated-gate bipolar transistors (IGBTs)
- Key enabler for next generation medium- and high voltage direct current (MVDC & HVDC) grids that could support more diverse, renewable intensive energy landscape
- Could also support other advanced power conversion applications in Energy, Aviation, and Healthcare sectors

GE research team drawing from 15+ years of research and application experience to create the world's leading Silicon Carbide (SiC) technology platform

https://www.ge.com/research/newsroom/ge-research-awarded-3-mm-arpa-e-project-develop-worlds-1st-high-voltage-silicon-carbide