CURENT
CENTER FOR ULTRA-WIDE-AREA RESILIENT ELECTRIC ENERGY TRANSMISSION NETWORKS

THE UNIVERSITY of TENNESSEE KNOXVILLE

Parasitic Inductance Extraction and Verification for 3D Planar Bond All Module

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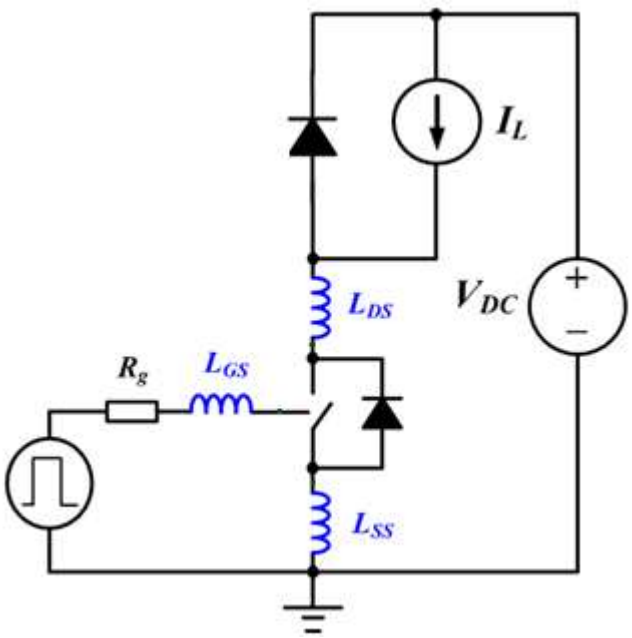
Outline

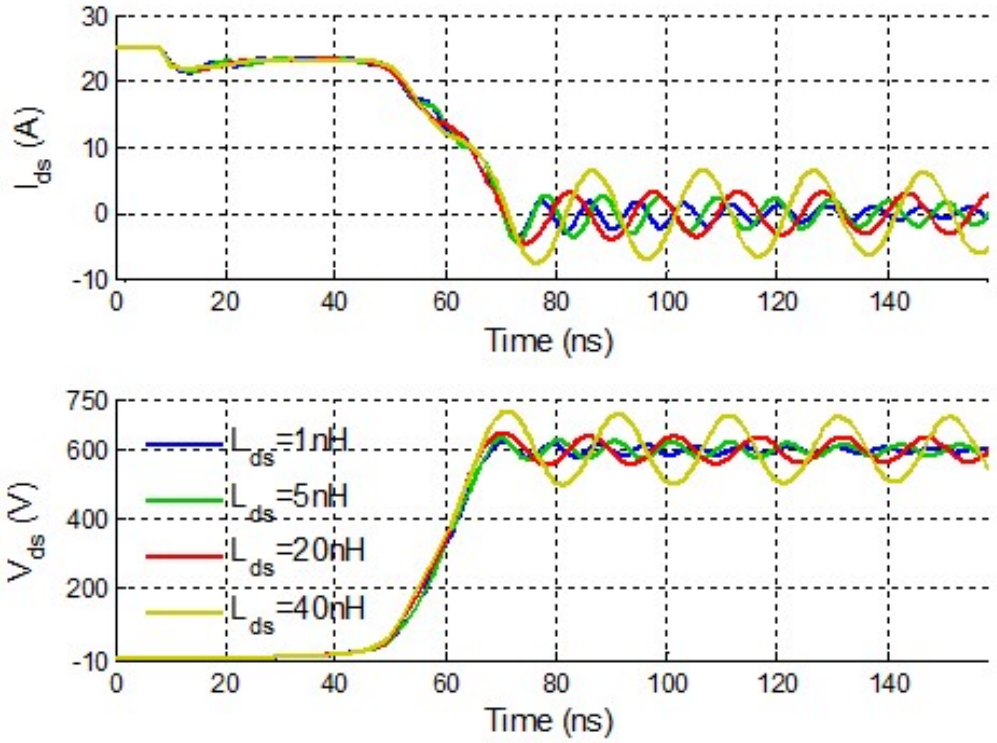
- Background
- Parasitic Inductance Extraction
- Parasitic Inductance Experiment Verification
- Conclusion

Background

- Power Loop Inductance L_{ds} and its side effect on switching transients



Circuit Schematics

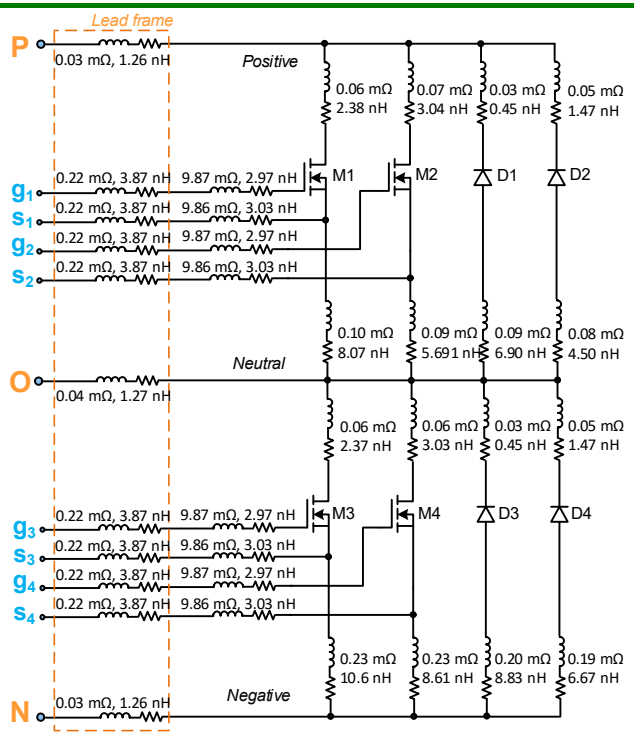


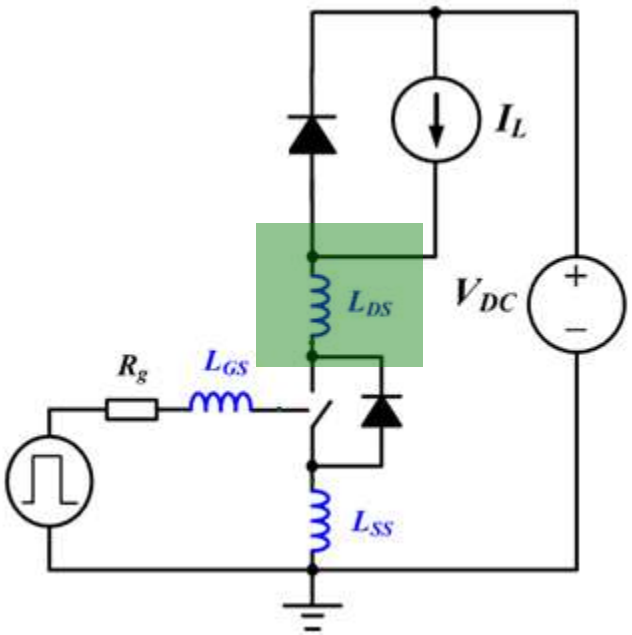
Turn-off waveforms with different L_{ds}

- Power loop inductance L_{ds} will lead to large voltage spikes during active device's turning off.

Z. Chen, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in International Power Electronics Conference (IPEC), 2010, pp. 164-169.

Purpose of the Study





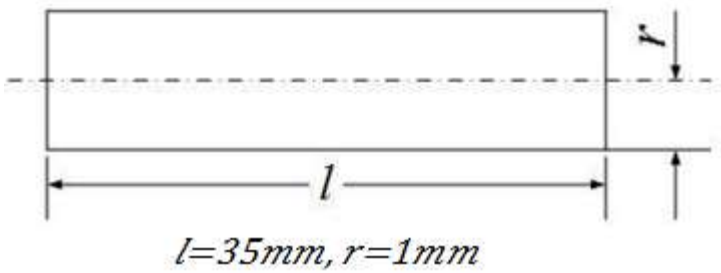
- Develop methods to extract the lumped power loop inductance value in simulation.
- Explore the physical meaning of the lumped power loop inductance (is L_{ds} a constant time-invariant value or a time-varying parameter?).

Outline

- Background
- **Parasitic Inductance Extraction**
  - Simulation of simple round wire
  - Simulation of paralleled wirebonds
  - Simulation of a 3D Planar Bond All module
- **Parasitic Inductance Experiment Verification**
- **Conclusion**

Simulation of One Round Wire

- Theoretical Calculation for Round Wire

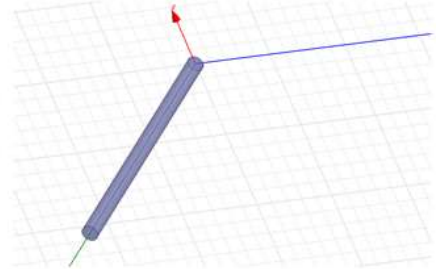


l=35mm, r=1mm

$$L_p = \frac{1}{5} l\left(In\frac{4l}{d} - \frac{3}{4}\right)$$ Low frequency range

$$L_p = \frac{1}{5} l\left(In\frac{4l}{d} - 1\right)$$ High frequency rage considering skin effect

- Theoretical Calculation for Round Wire
  - Same parameters are used for a round wire in Q3D simulation.

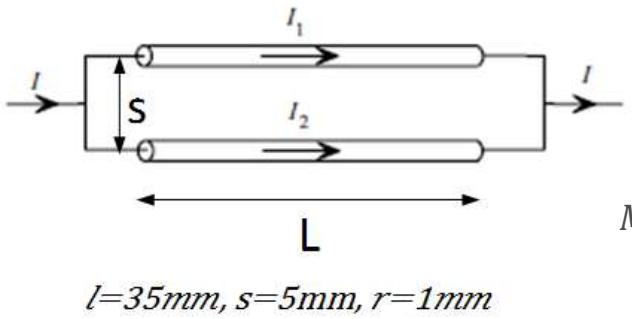


- Result and Comparison

Inductance	Theoretical Calculation	Simulations
Low frequency	24.49 nH	24.70 nH
High frequency	22.74 nH	22.98 nH @ 100MHz

Two Round Wires with Current in One Direction

- Theoretical Calculation for Round Wire



l=35mm, s=5mm, r=1mm

$$L_{total} = 0.5(L_p + |M_p|)$$

$$M_p = \frac{1}{5} l \left(In\left(\frac{l}{s+r} + \sqrt{\left(\frac{l}{s+r}\right)^2 + 1} \right) - \sqrt{\left(\frac{s+r}{l}\right)^2 + 1} + \frac{s+r}{l} \right)$$

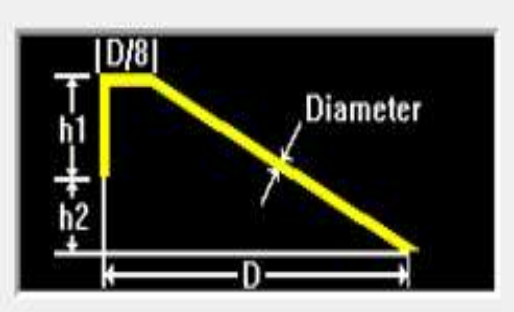
- The mutual inductance M_p will play a role in the total inductance value L_{total}.
- The closer the distance (smaller s), the larger the value of mutual inductance M_p, resulting a larger total inductance value L_{total}.

- Result and Comparison

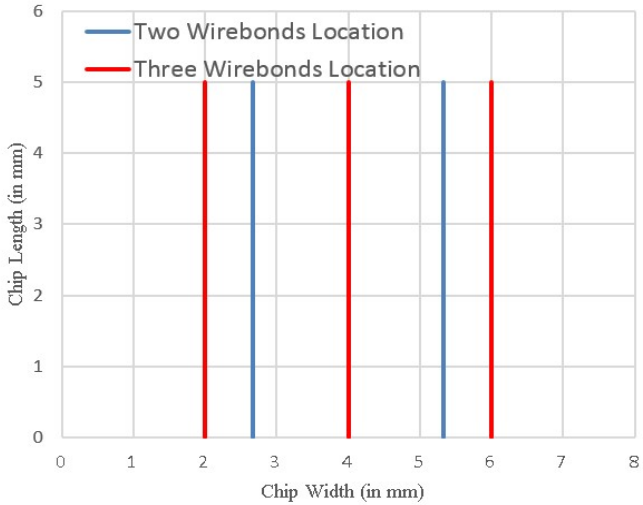
Inductance	Theoretical Calculation	Simulations
Low frequency	18.46 nH	18.57 nH
High frequency	17.90 nH	17.61 nH @ 100MHz

Simulation of Wirebonds

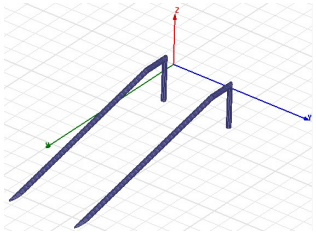
- Wirebond Selection
  - The number of wirebonds is typically determined by the current rating of the device and the current capabilities of each wirebond considering some design margin.
  - Different combinations of the number of wirebonds and gauge of wires can be obtained for the same current capability.
- Wirebond Parameters in Q3D Simulation



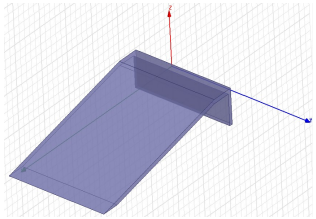
$h1 = 2mm, h2 = 0,$
$D = 12mm, d = 10\ or\ 15\ mils$



Location of wirebonds



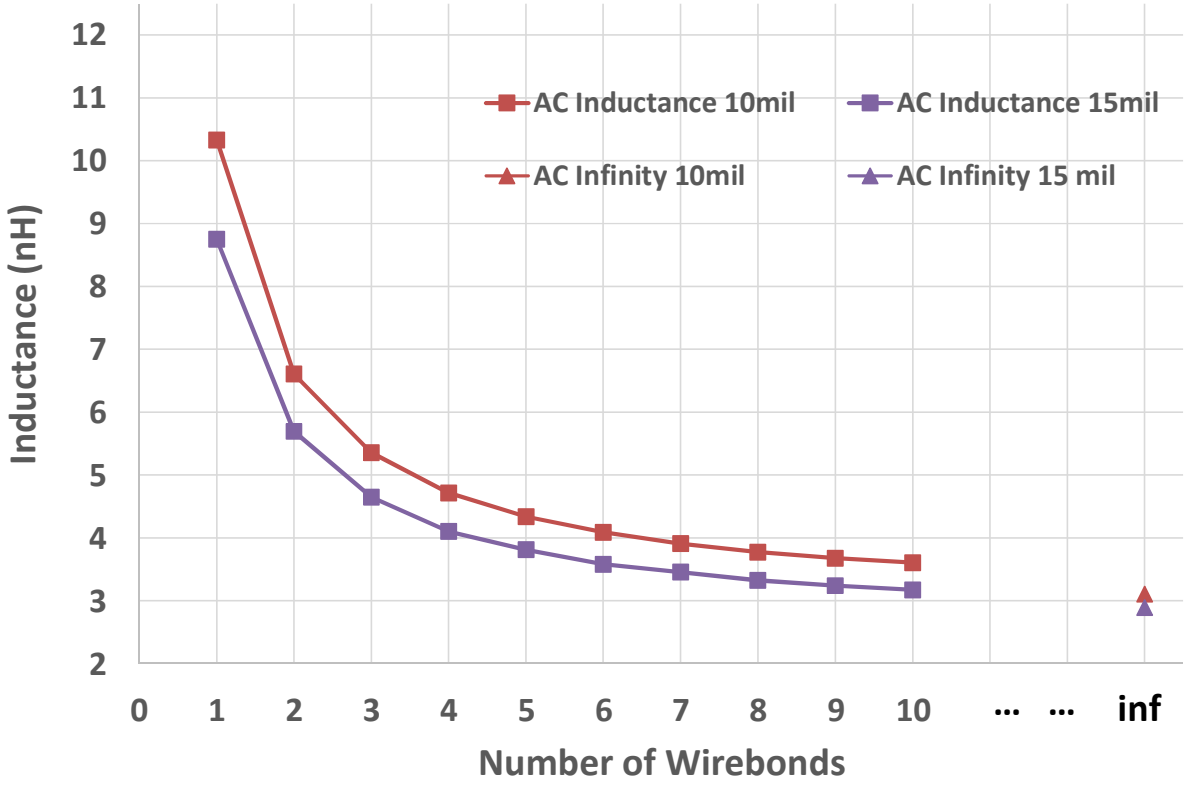
Two wirebonds



Aluminum bar

Simulation of Wirebonds Cont.

- Parasitic Inductance of Wirebonds Vs. the number of wirebonds at different gauges



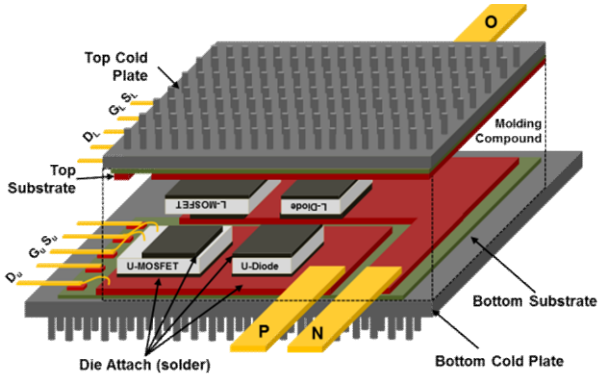
- The inductance value indeed decreases with increasing numbers of wirebonds.
- However, due to the width limitation of the chip and effect of mutual inductance, the rate of change of inductance is slower at higher number of wirebonds.

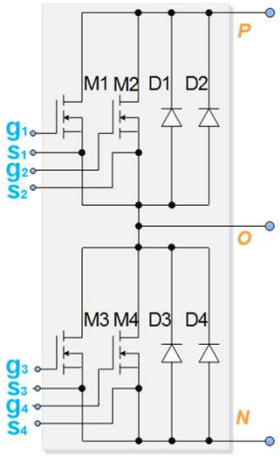
Outline

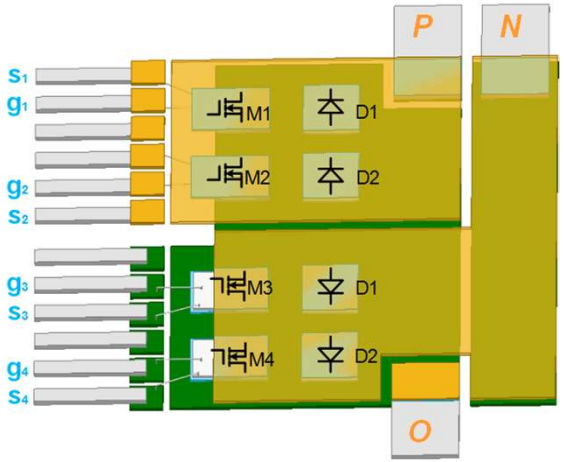
- Background
- **Parasitic Inductance Extraction**
  - Simulation of simple round wire → **Verified software accuracy**
  - Simulation of paralleled wirebonds → **Studied the effect of mutual inductance**
  - Simulation of a 3D Planar Bond All module → **Extract L_{ds}**
- **Parasitic Inductance Experiment Verification**
- **Conclusion**

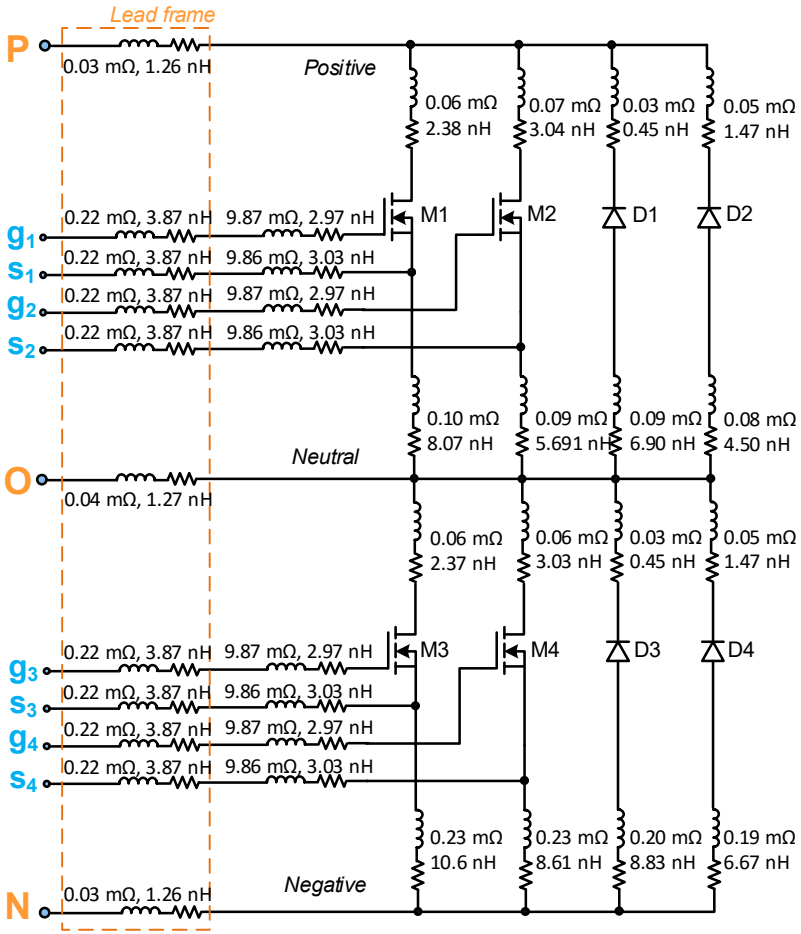
Simulation of 3D PBA Module

- 3D Planar Bond All (PBA) Module





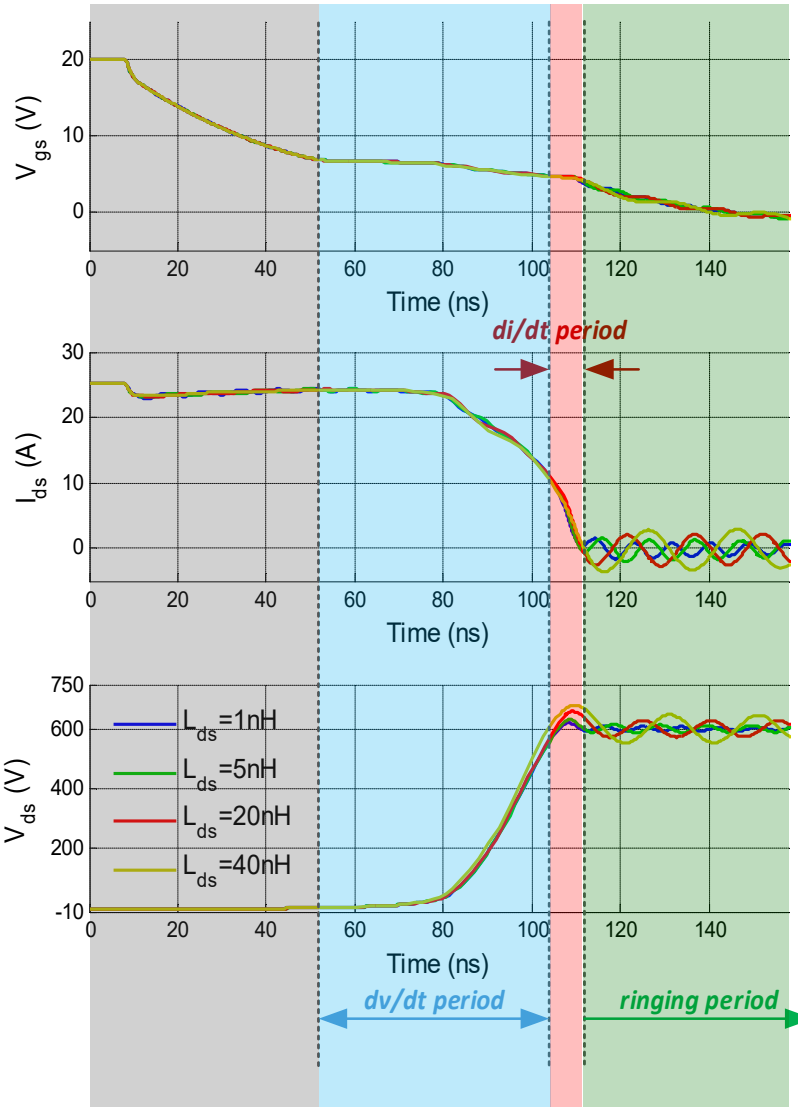


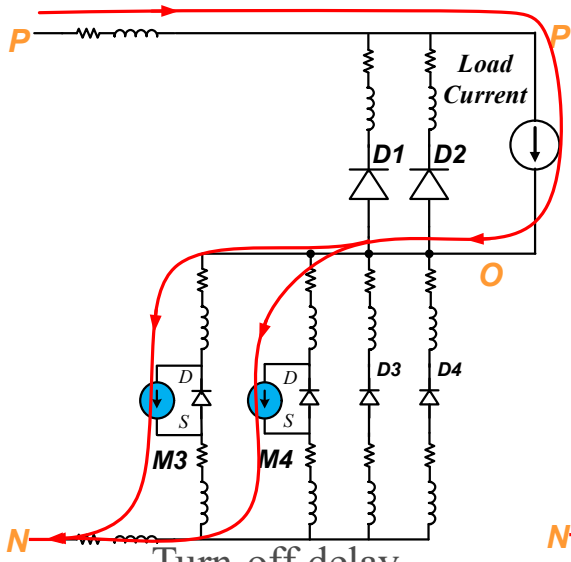


[Z. Liang, "Integrated double sided cooling packaging of planar SiC power modules," in 2015 IEEE Energy Conversion Congress and Exposition (ECCE), 2015, pp. 4907-4912.

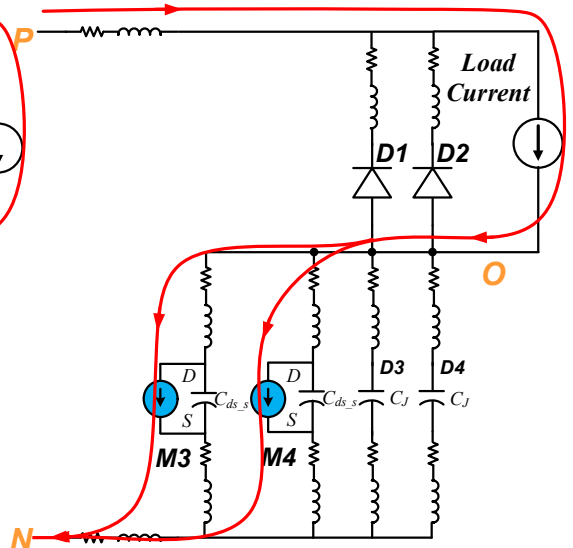
Simulation of 3D PBA Module Cont.

❑ Switching Waveforms

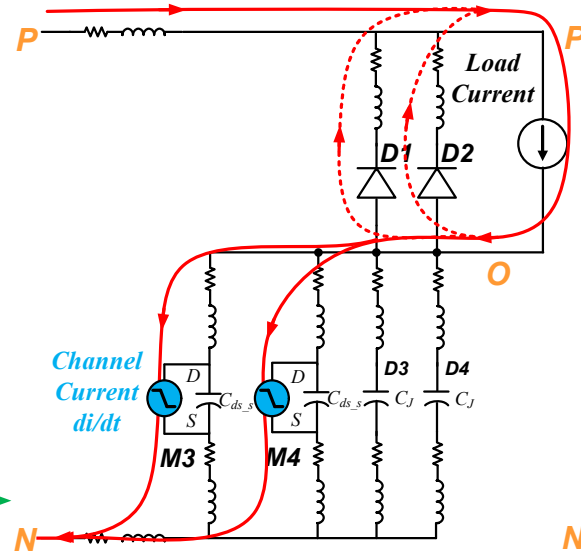




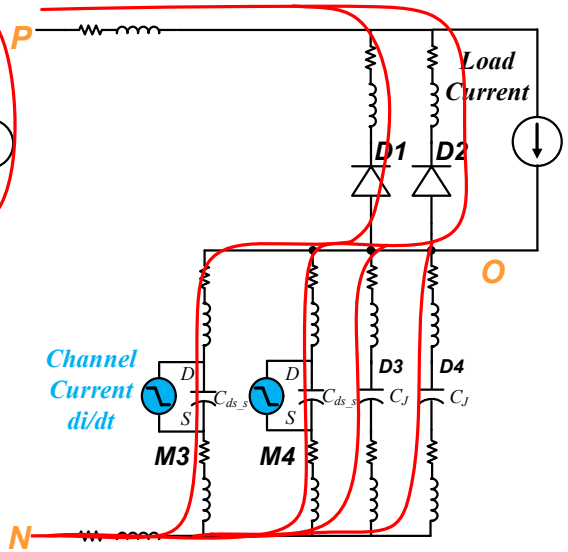
Turn-off delay



dv/dt period



di/dt period

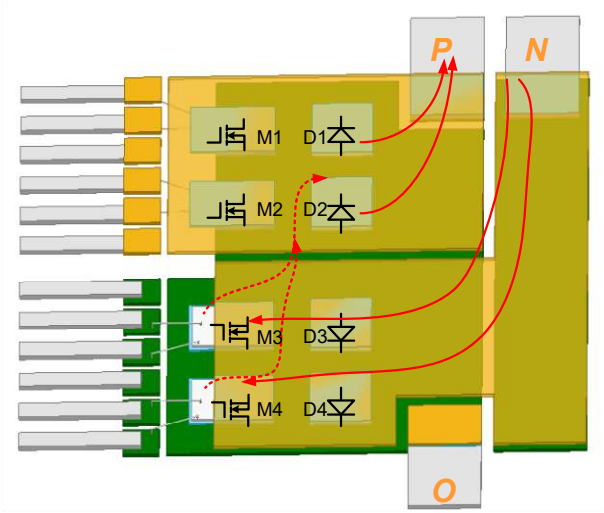


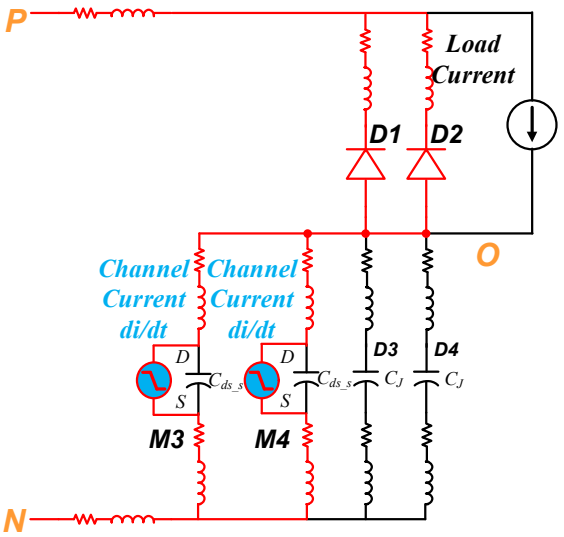
ringing period

Simulation of 3D PBA Module Cont.

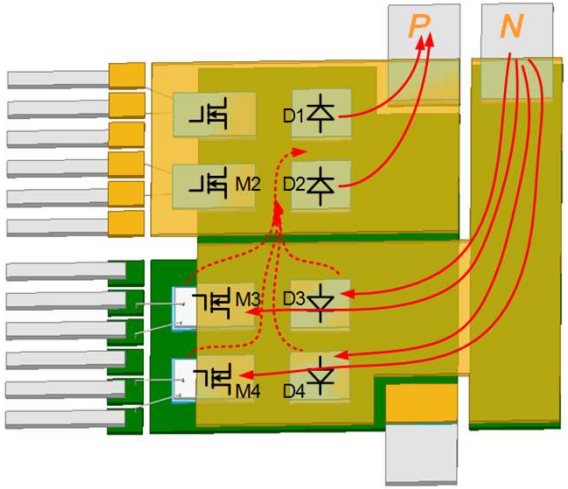
- Switching Transients and Parasitic Inductances

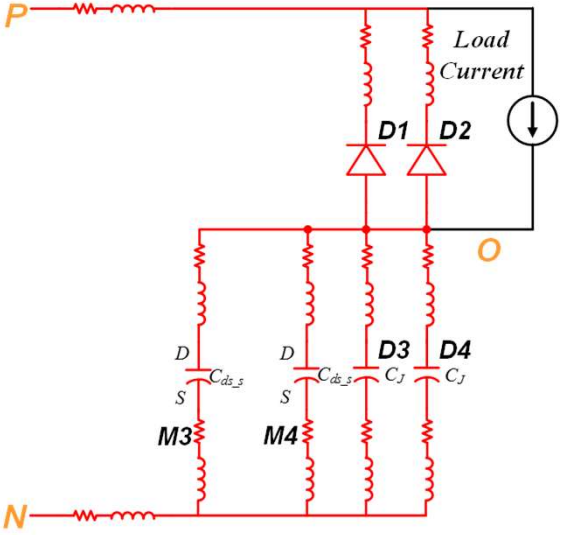
di/dt period





ringing period





Simulation of 3D PBA Module Cont.

❑ Simulation Result

Condition (@100MHz)		Upper Device	Lower Device
Turn off Loop Inductance	During di/dt	6.01 nH	6.03 nH
	Ring period	5.73 nH	5.82 nH

- The parasitic inductance values during di/dt and in ringing period are different for both upper and lower devices.
- There is some discrepancy between the turn off power loop inductance values for upper and lower device because of the the asymmetric package design.

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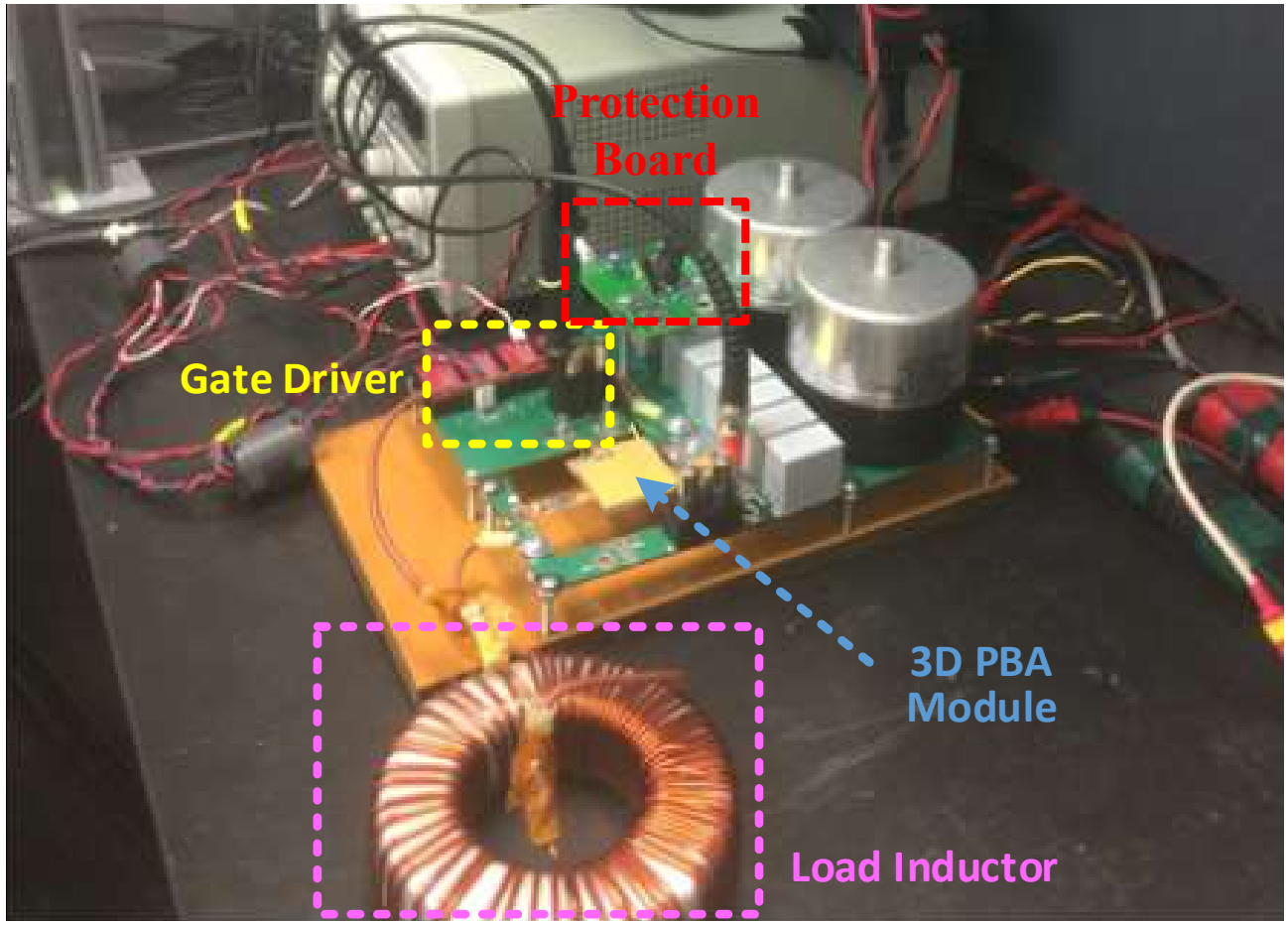
  - Simulation of a 3D Planar Bond All module
- **Parasitic Inductance Experiment Verification**
- **Conclusion**

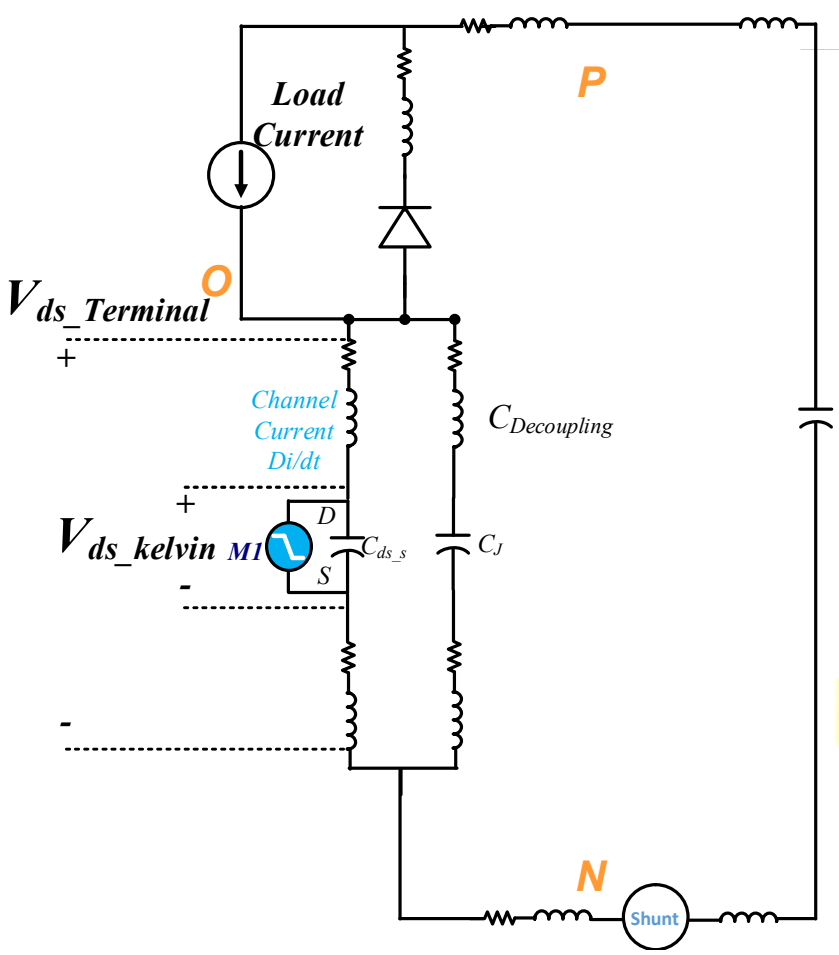
Experiment Set-up

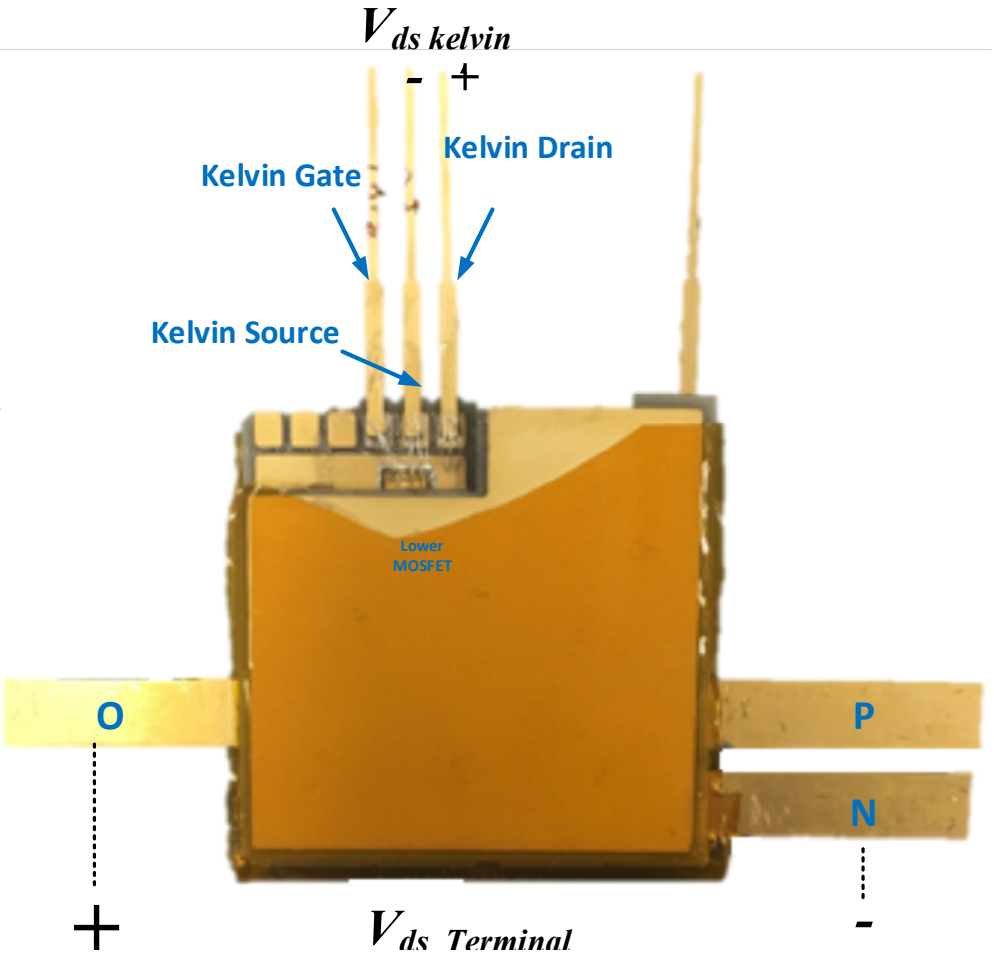
- Double Pulse Test Bench



3D PBA Module

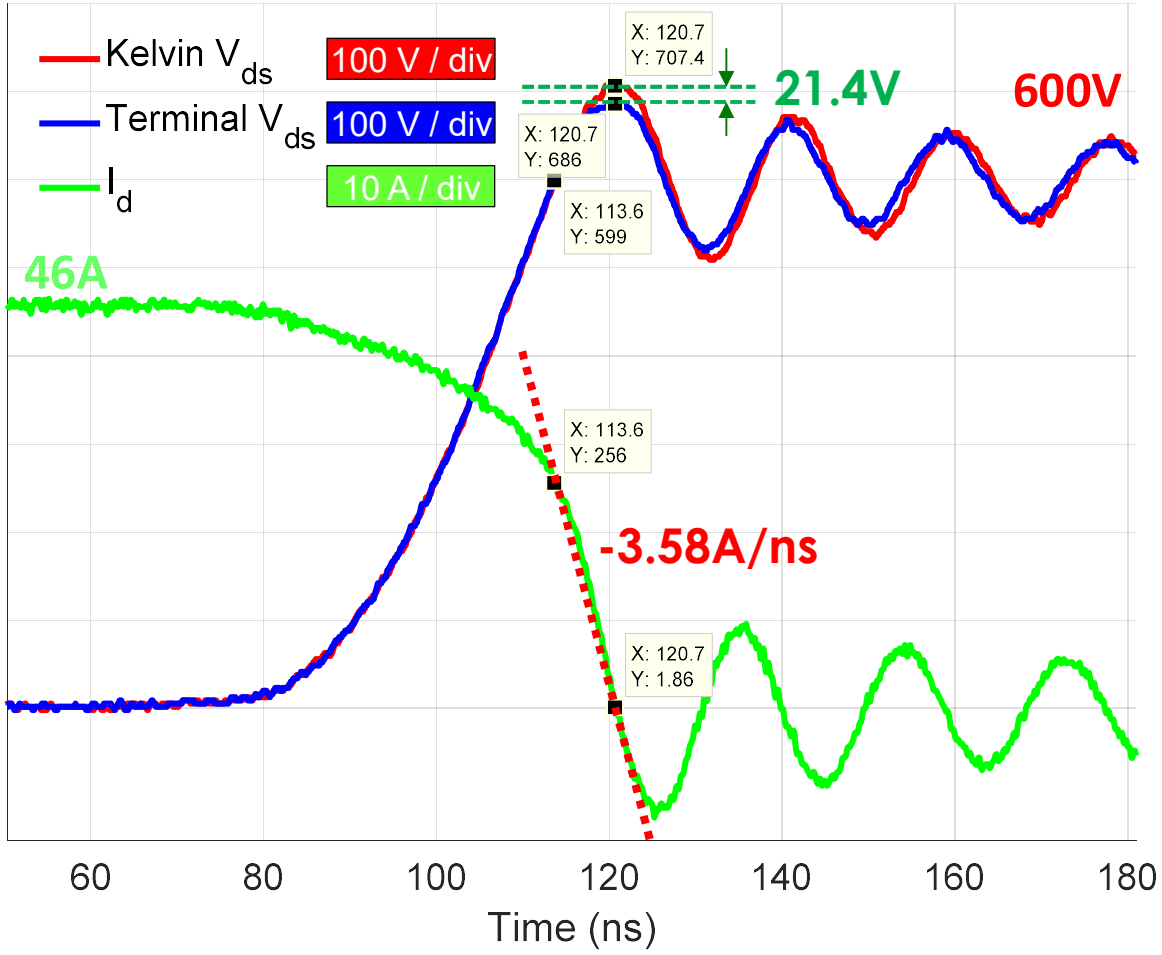
- Accessible Kelvin Connection





Experiment Result

- Experiment Turn-off Waveforms



$$L_{exp} = 21.4\,V/(3.58\,A/n\,s) = 5.98\,nH$$

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Conclusion and Future Work

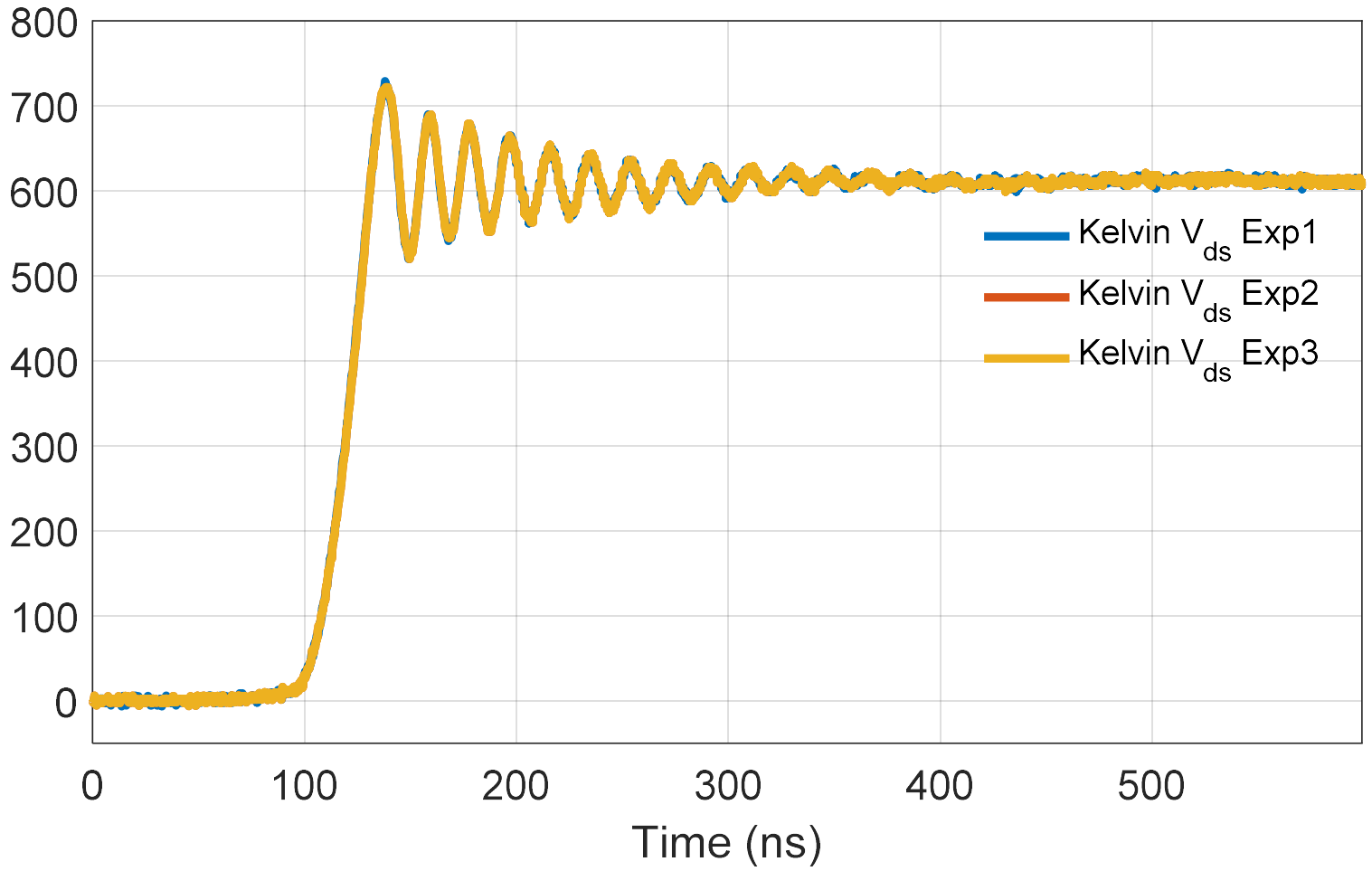
- Conclusion
  - For wirebond connections, the total parasitic inductance value cannot be effectively reduced simply by increasing the number of wirebonds.
  - A method to extract the power loop inductance is discussed in detail for a 3D PBA module.
  - It is observed in simulation that power loop inductance's value is varying.
- Future Work
  - Design and fabricate an ultra-low inductance SiC power module.

Thank you !

Back Up

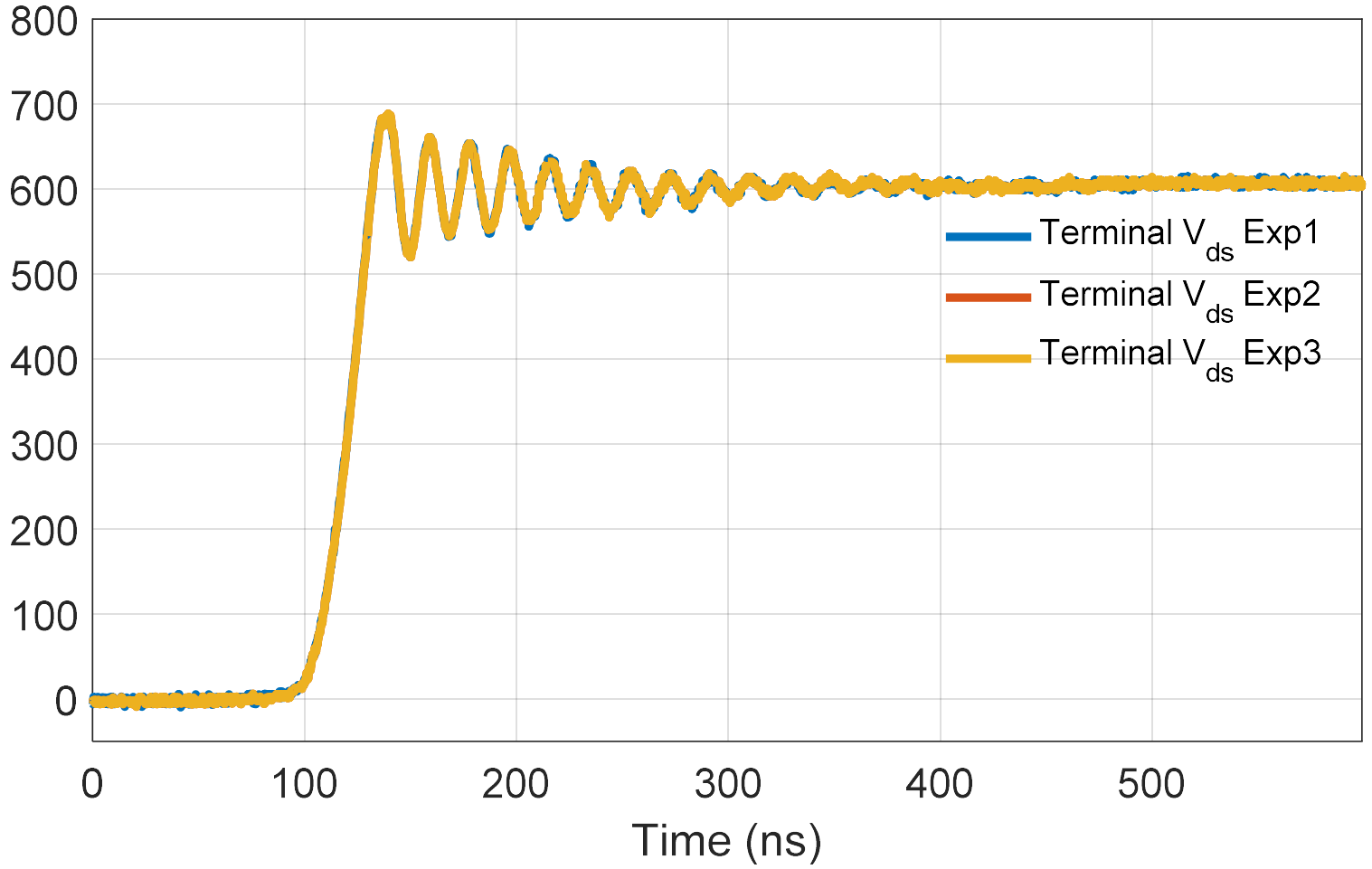
Consistency in Test Result1

- Kelvin V_{ds} at different times
  - Almost the same curves are obtained at the same testing condition.



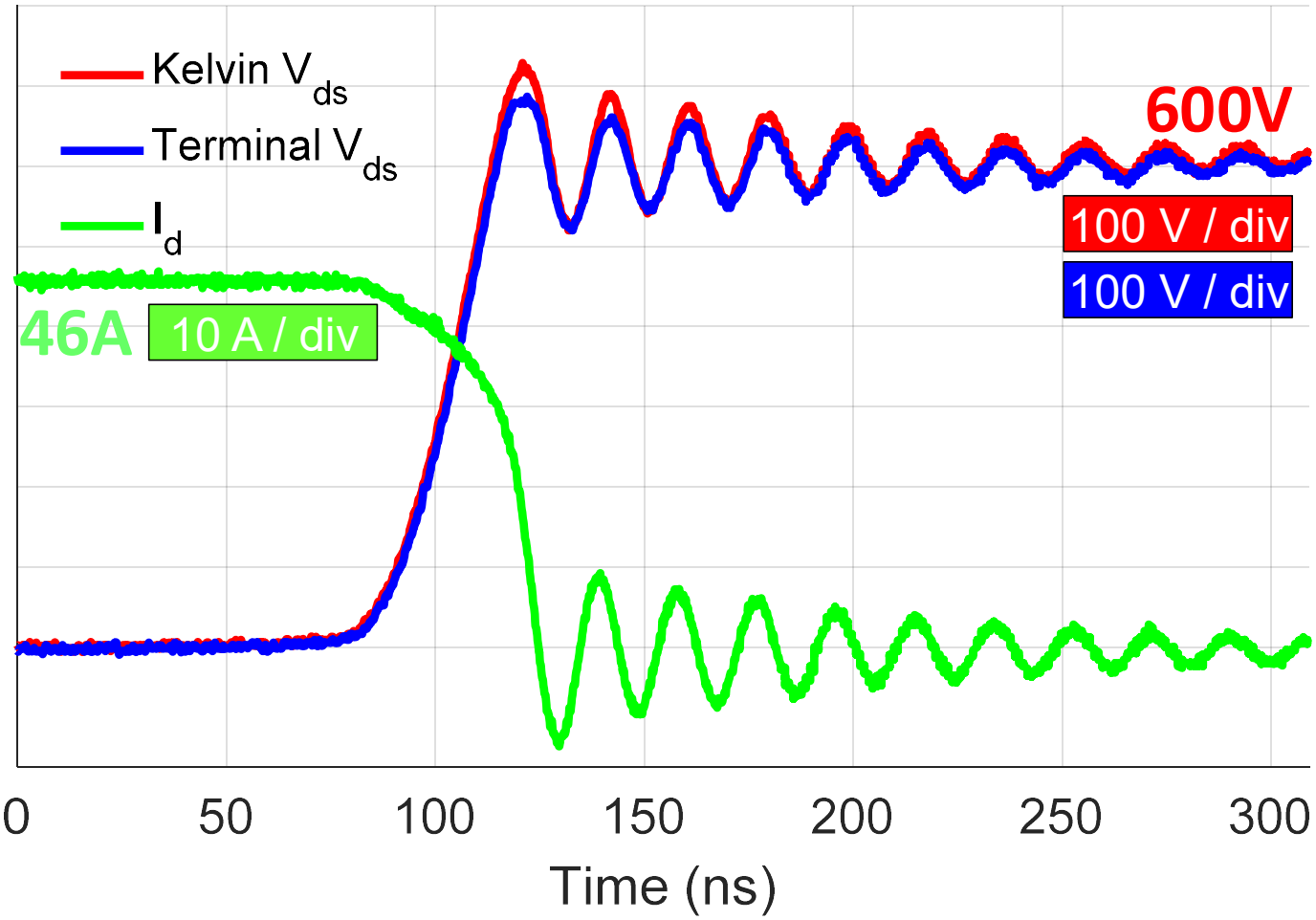
Consistency in Test Result2

- Terminal V_{ds} at different times
  - Almost the same curves are obtained at the same testing condition.



Problem

- Test results at same time with different probes
  - Kelvin and Terminal voltages are not well aligned.



Problem

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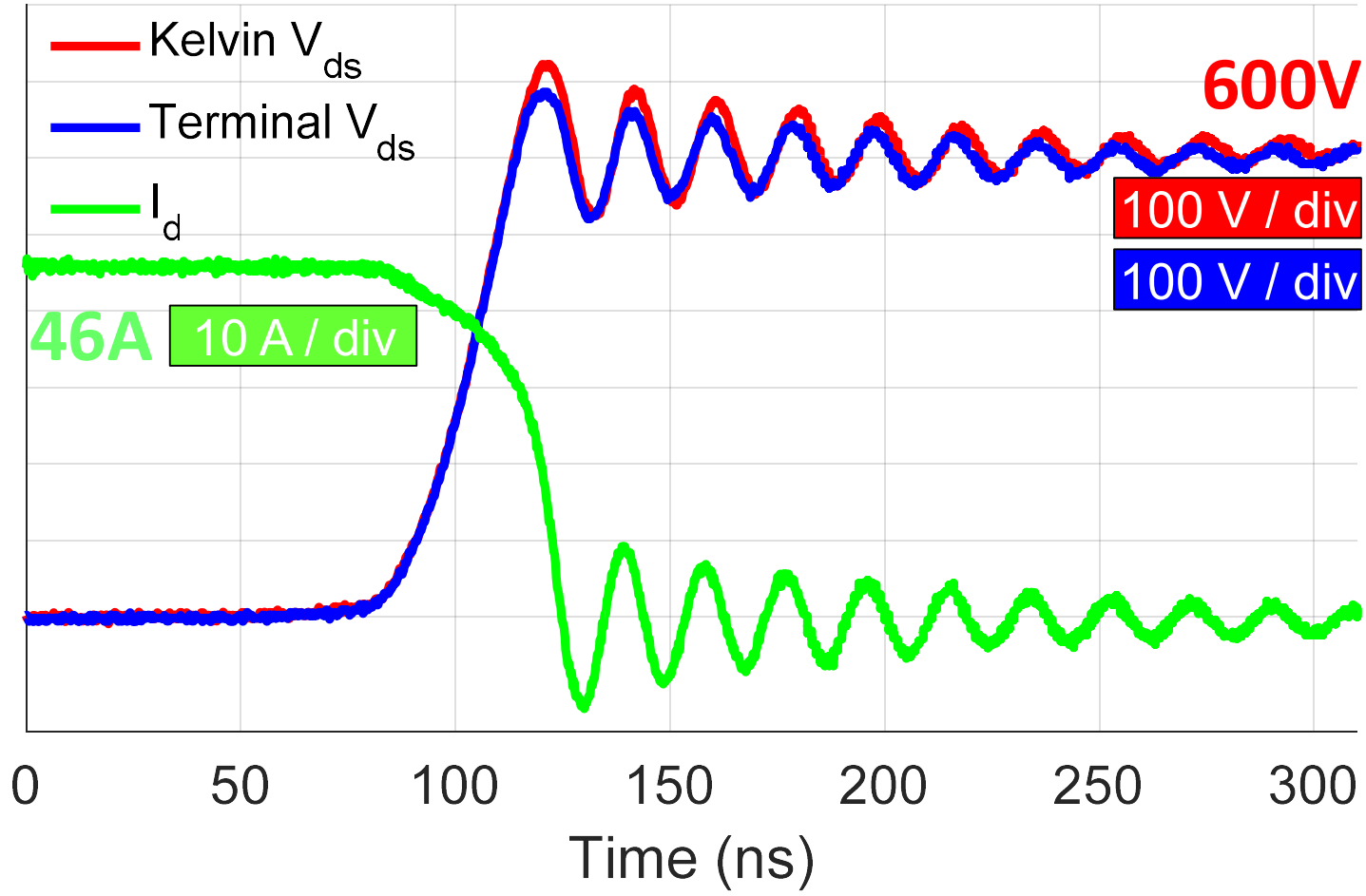
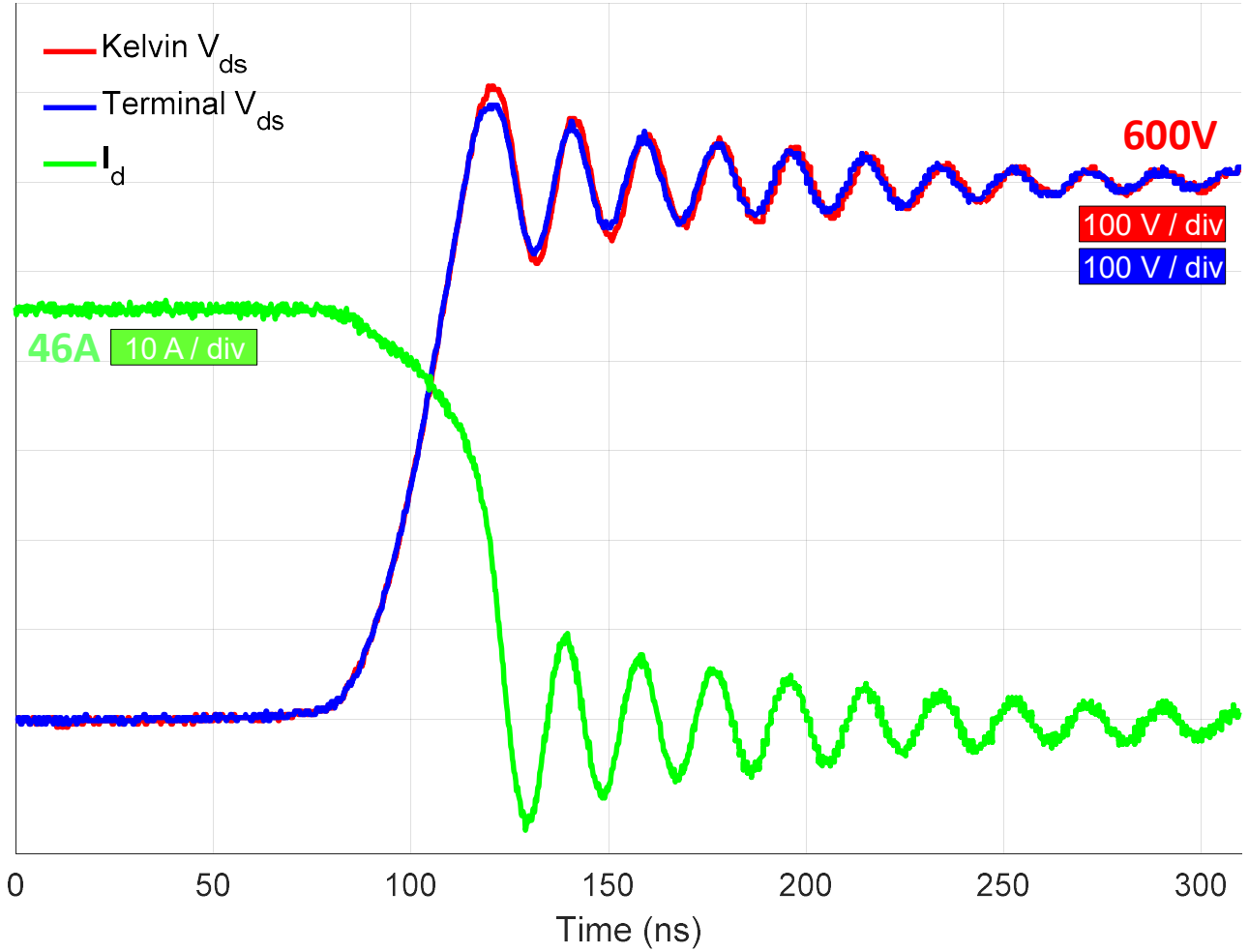


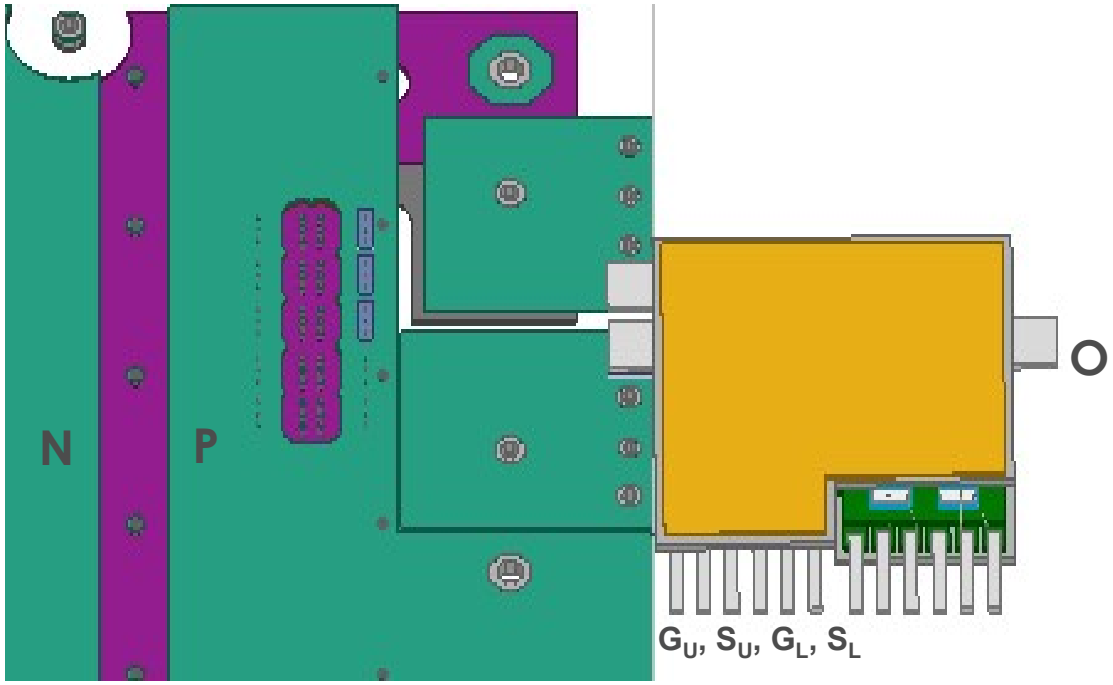
Problem Solved

- Test results at separate time with same probes
  - Kelvin and Terminal voltages aligned pretty well.



Simulation including Bus-bar

❑ Simulation Result



Condition **(@100 MHz)**		**Upper Device**	**Lower Device**
Turn off Loop Inductance	During di/dt	**23.00 nH**	**23.03 nH**
	Ringing Period	**21.78 nH**	**22.32 nH**

PCB Introduced Parasitic Inductance

- Simulation Result