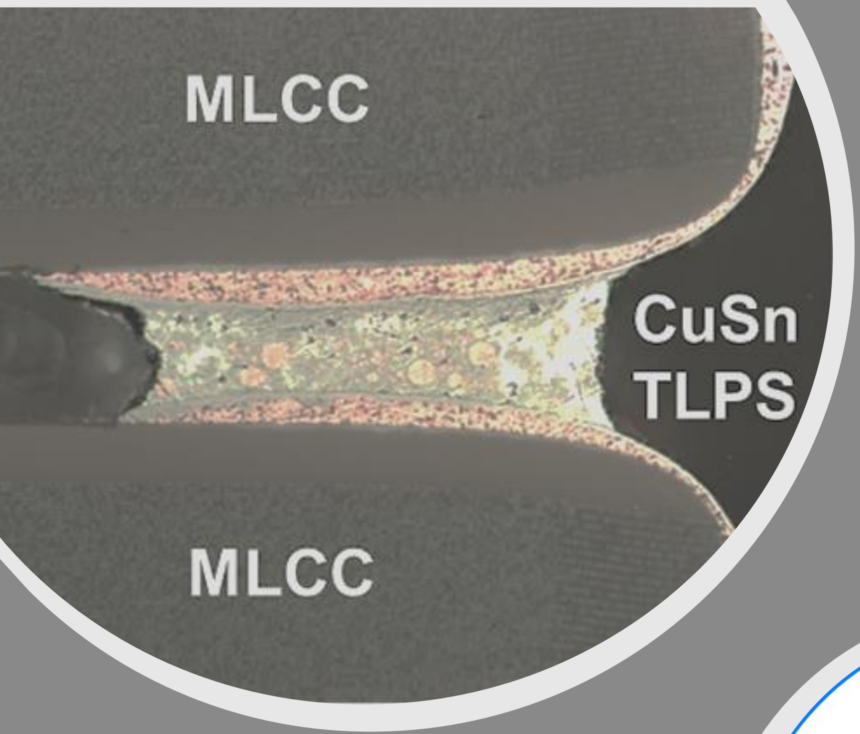
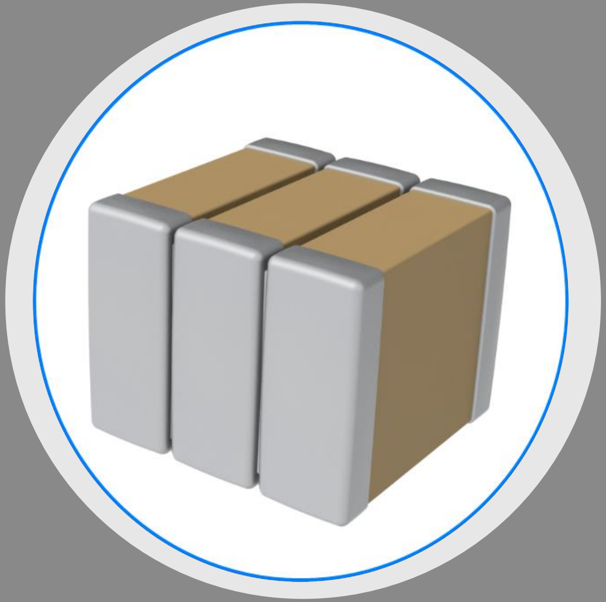




Packaging and integration of passive components to reduce board space with optimized thermal and electrical performance

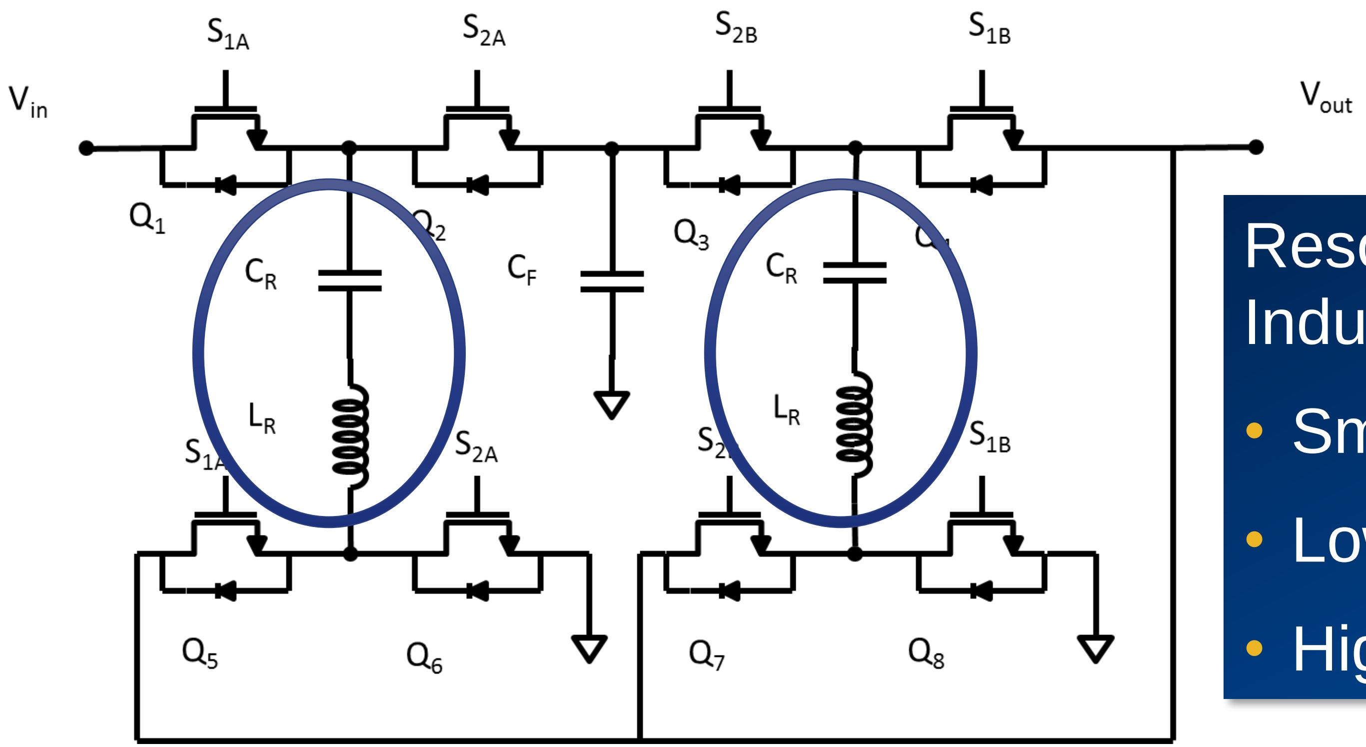
John Bultitude, Tony Burk, Allen Templeton, Nathan Reed, Galen Miller, John McConnell, Javaid Qazi, Abhijit Gurav, Lonnie Jones, Jim Magee, Manuel Ortiz, Mark Laps, Reggie Phillips, Kunihiro Kusano, Kenichi Chatani & Yoshihiro Saito

Presentation Outline

- Resonant Capacitors & Inductors for Switched Tank Converters
  - U2J Capacitors & Mn-Zn Ferrite inductors
  - Leadless Stacks for reduced footprint
  - High Current Handling
- LC Module for further size reduction
- WBG Capacitor Requirements for higher power & voltages
  - C0G Capacitors
  - Leadless Stacks for higher capacitance
- Packaging Roadmap

Switched Tank Converters

48V – 12V Step Down Power Conversion with 98.92% efficiency up to 650W [1]



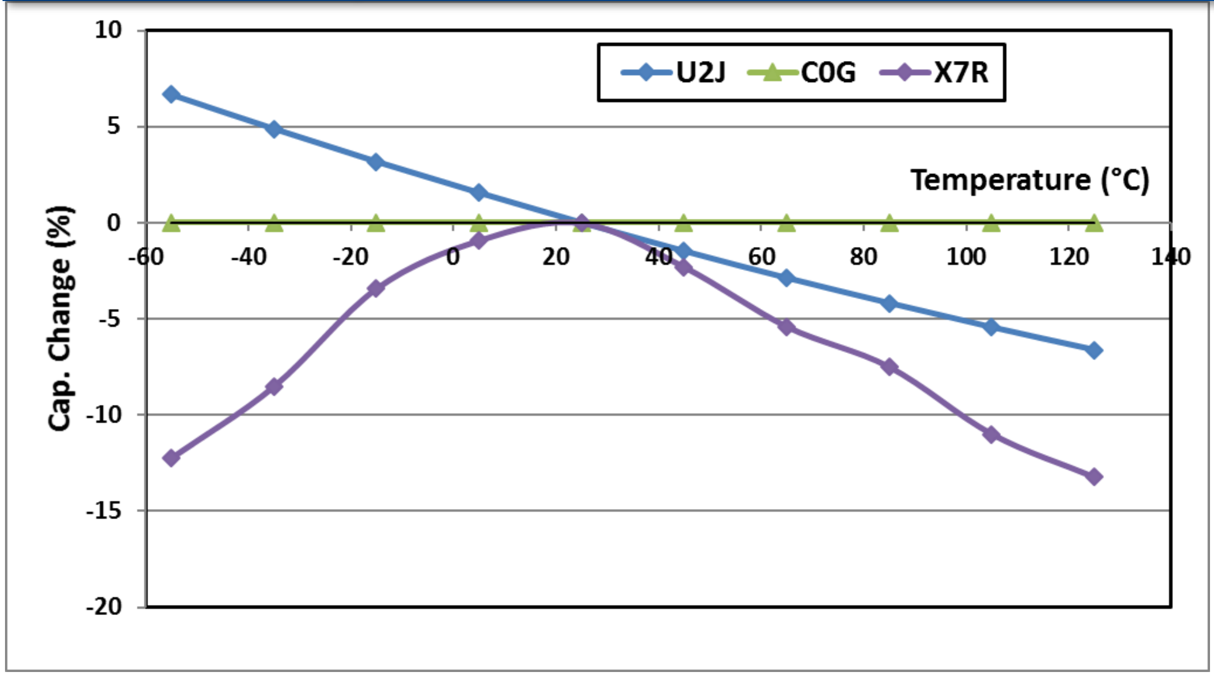
Resonant Capacitors and Inductors with

- Small Footprint
- Low AC Losses
- High Frequency ~300kHz

*[1] **S. Jiang, C. Nan, X. Li, C. Chung, M. Yazdani, “Switched tank converters”, Proceedings 33rd Annual IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, March 4-8, 2018, pp.81-90.***

Development of U2J Resonant Capacitors

- Change of capacitance with temperature for X7R is too large, although K ~ 3500
- C0G Dielectric Constant is too low K~ 31
- U2J Developed K~ 82



$$C = K\,K_0\,A\,n\,/\,t$$

Where:

C = Capacitance

K = Dielectric constant

K_0 = Permittivity of free space (8.854 x 10-12 F/m)

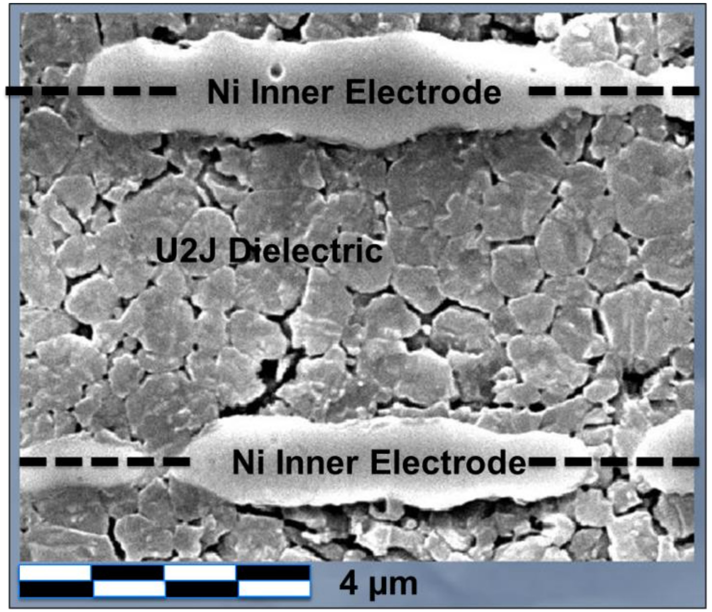
A = Overlap Area of opposed electrodes in MLCC

n = Number of active layers in MLCC

t = Thickness of active layers

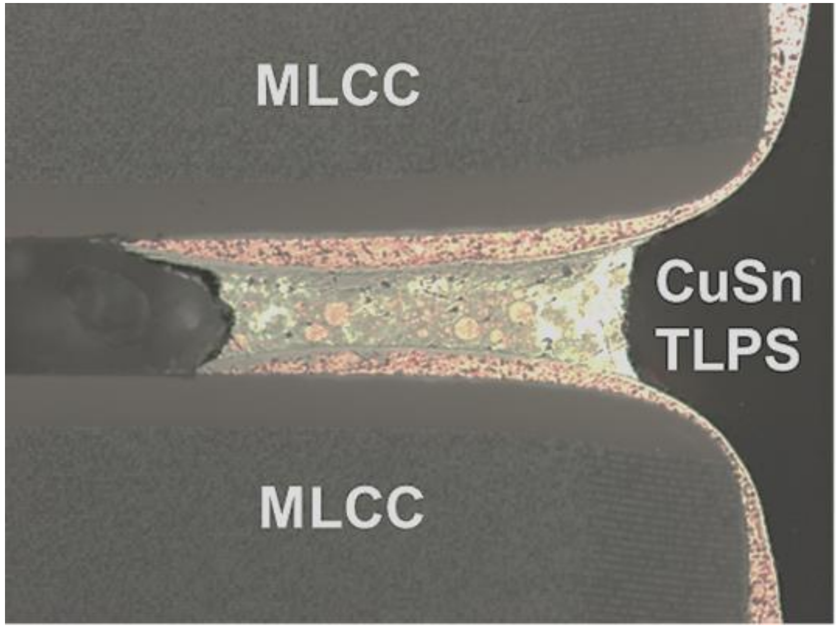
[2] *J. Bultitude & Y. Saito et al, "Development & Characterization of Resonant Capacitors and Inductors for Switched Tank Converters", Proceedings 2018 IEEE International Power Electronics and Application Conference and Exposition, November 4-7, Shenzhen, China*

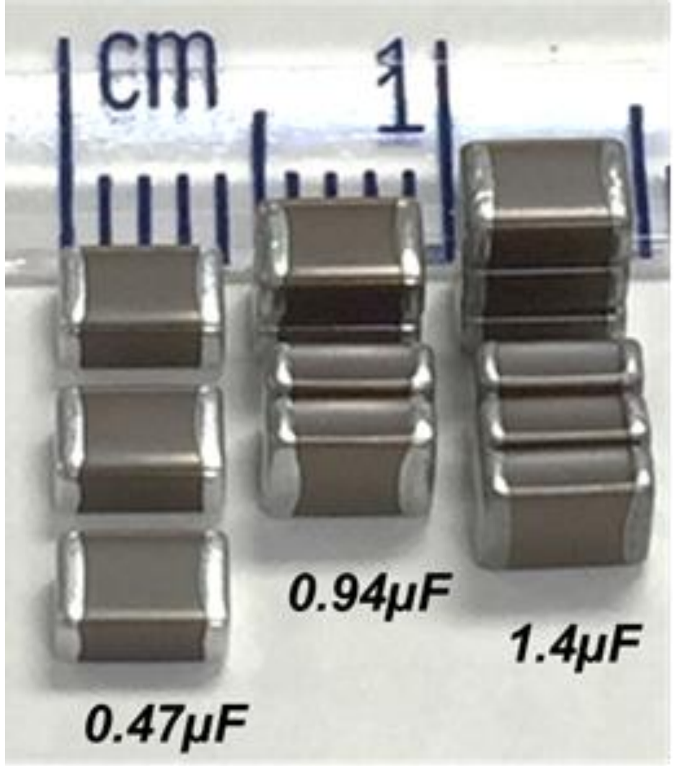
Development Leadless Stacked Capacitors



U2J 1812 0.47µF 50V MLCC

Transient Liquid Phase Sintering, TLPS is used to bond the terminals of the MLCC together



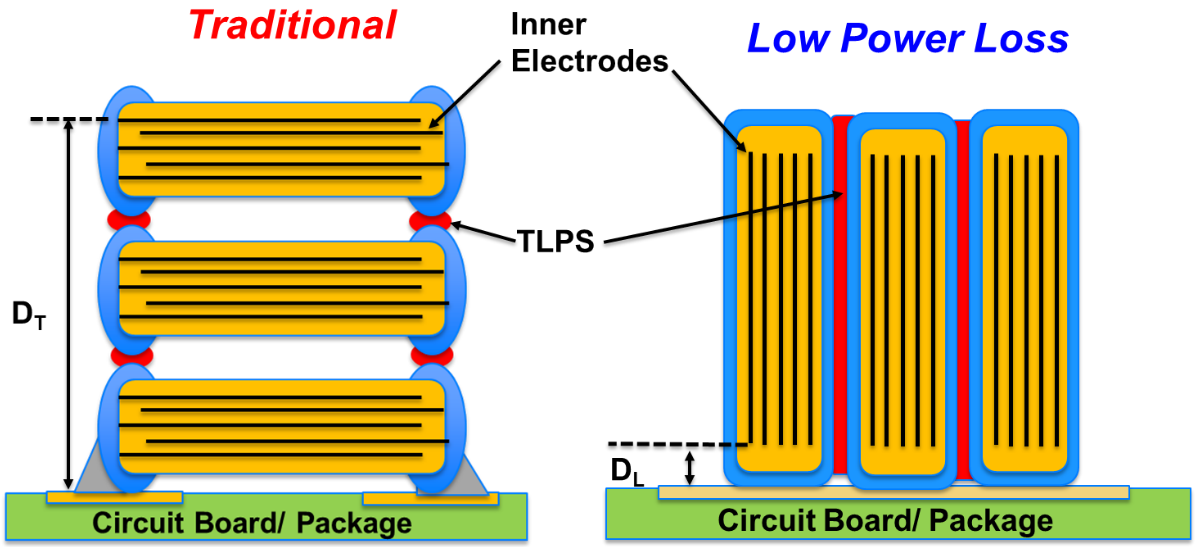


KEMET KONNEKT™ High Density Packaging

Leadless Stacks ESR & Orientation

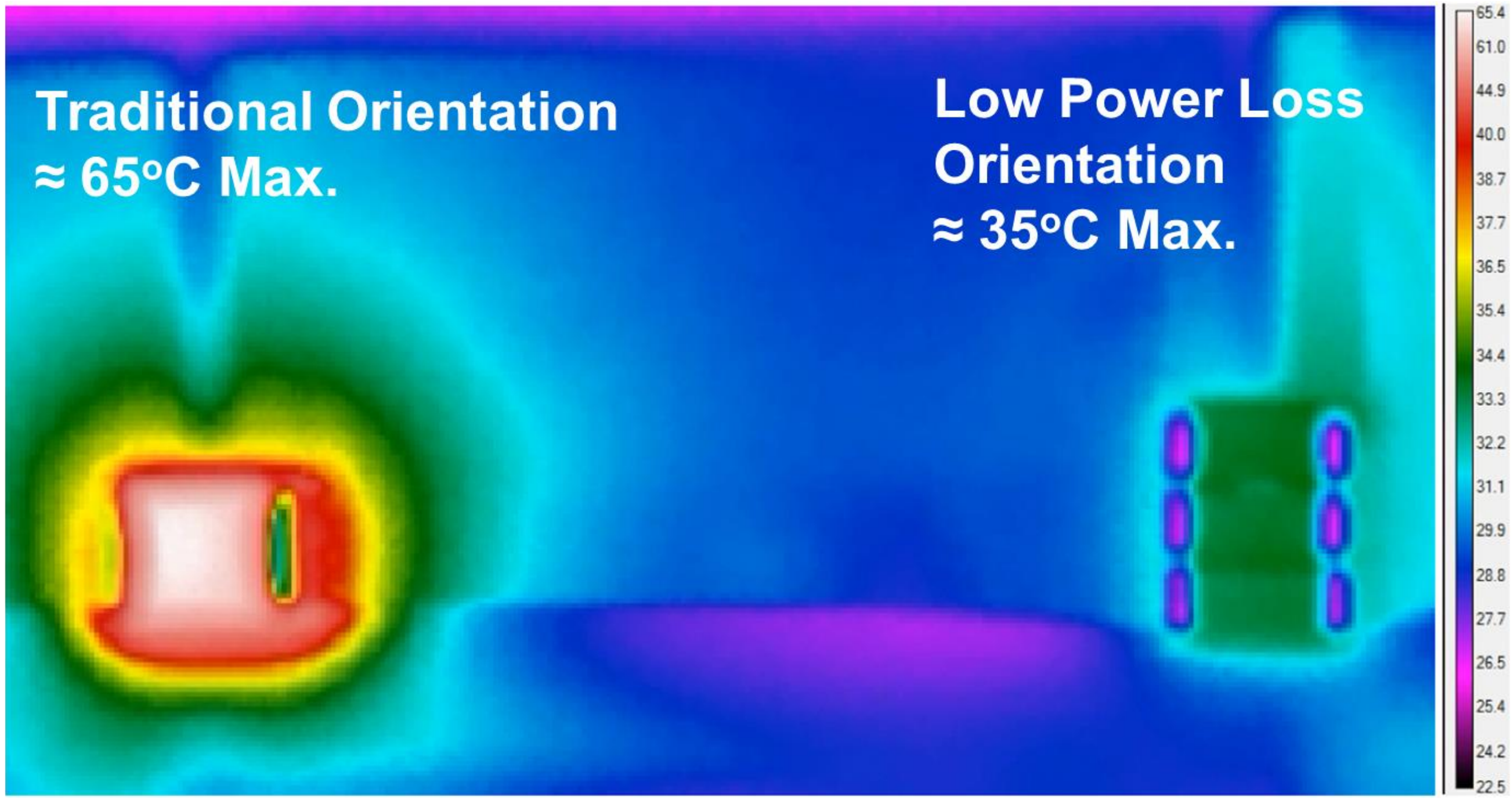
1.4µF Leadless Stacks have lowest ESR with electrodes perpendicular $P = i^2 ESR$

U2J Part Description	Part Number	Number of MLCC	E4980A ESR @ 300kHz (mΩ)	E4990A ESR @ 300kHz (mΩ)	Solder Pad Area (mm^2)
1812, 0.47µF, MLCC	C1812C474J5JACTU	1	0.4	1.2	24.0
2 x Traditional, 0.94µF	C1812C944J5JLCTU	2	1.4	1.3	24.0
3 x Traditional, 1.4µF	C1812C145J5JLCTU	3	1.7	1.6	24.0
2 x Low Loss, 0.94µF	C1812C944J5JLC7805	2	1	0.9	24.0
3 x Low Loss, 1.4µF	C1812C145J5JLC7805	3	0.8	0.4	38.4

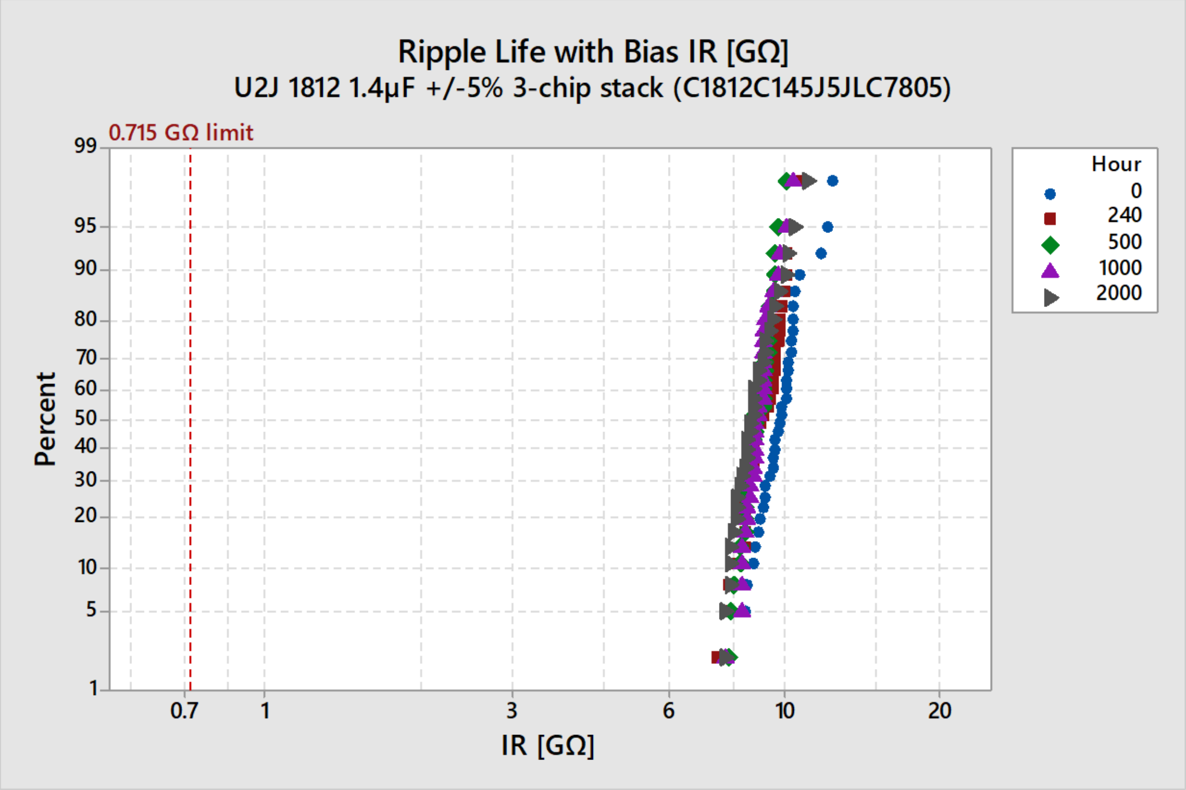


Leadless Stacks Ripple Current Heating

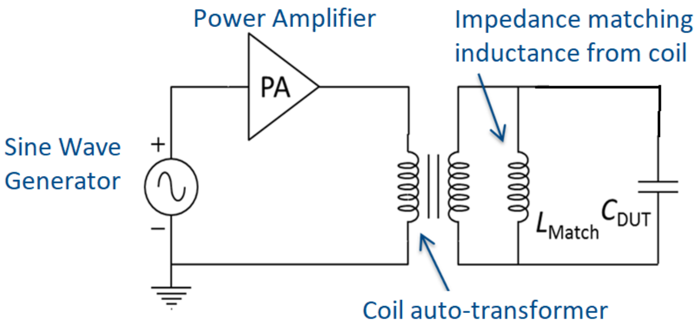
Lower ESR in Low Loss Orientation 1.4µF Leadless Stack has much lower self-heating at 300kHz $20A_{RMS}$



Leadless Stacks Ripple Current Life Testing



- 1.4µF Leadless Stack in the Low Loss Orientation were tested for 2000hours @ 105ºC with $30A_{RMS}$, 300kHz & $25V_{DC}$ applied
- IR remains stable and there were no failures (0/34)

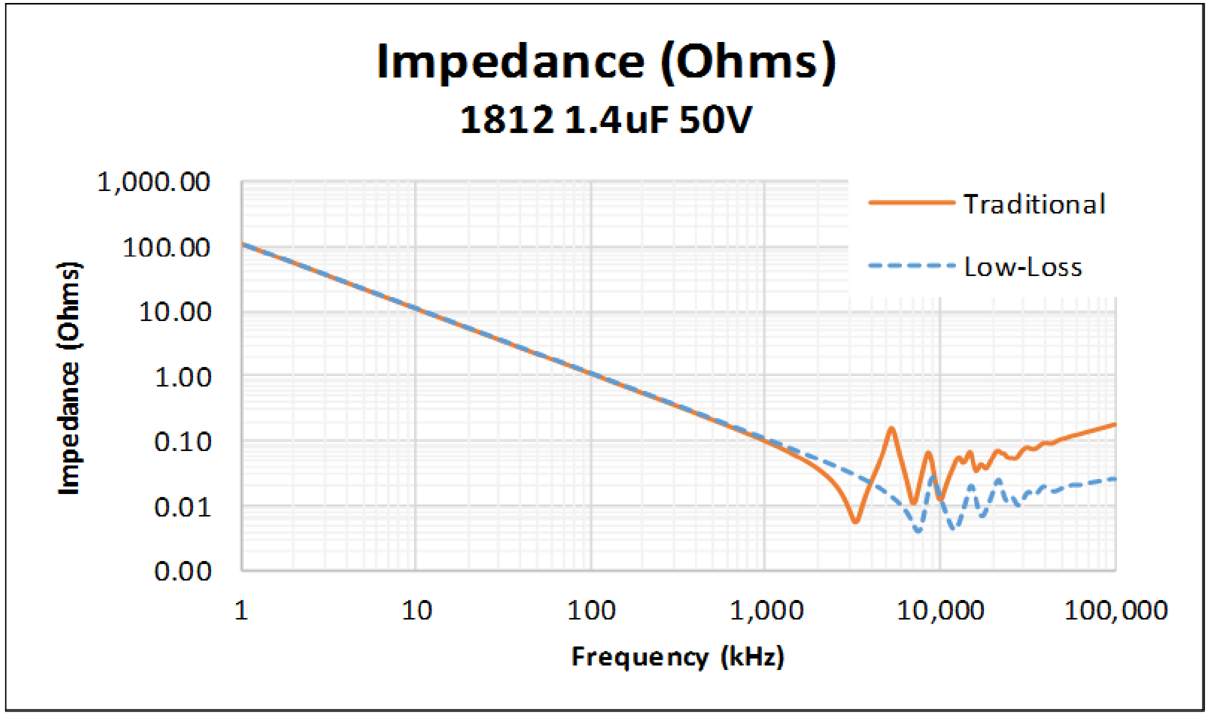


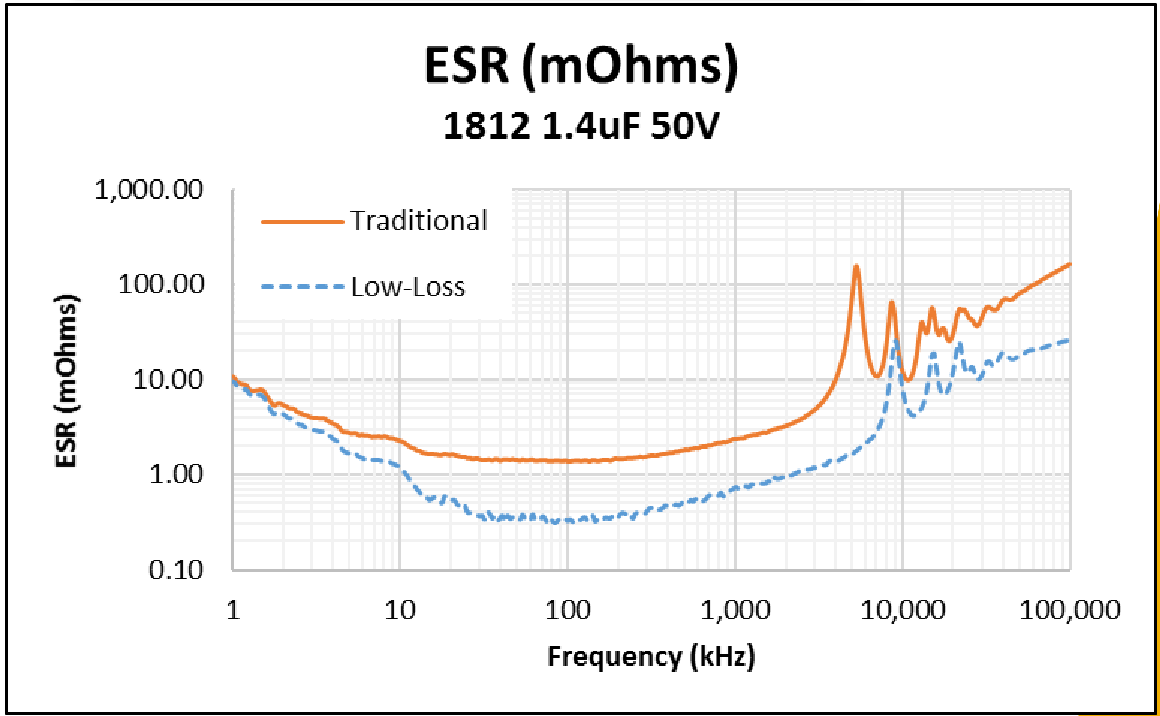
U2J Leadless Stack Development

U2J Part Description	Part Number	ESR (mΩ)			SRF	ESL
		1MHz	2MHz	3MHz	(MHz)	(pH)
1812, 0.47µF, MLCC	C1812C474J5JACTU	1.6	1.9	2.2	8.3	400
2 x Traditional, 0.94µF	C1812C944J5JLCTU	1.9	2.4	2.9	4.8	860
3 x Traditional, 1.4µF	C1812C145J5JLCTU	2.4	3.3	4.9	3.3	1100
2 x Low Loss, 0.94µF	C1812C944J5JLC7805	1.4	1.8	2.2	7.5	450
3 x Low Loss, 1.4µF	C1812C145J5JLC7805	0.7	1.0	1.2	7.5	400

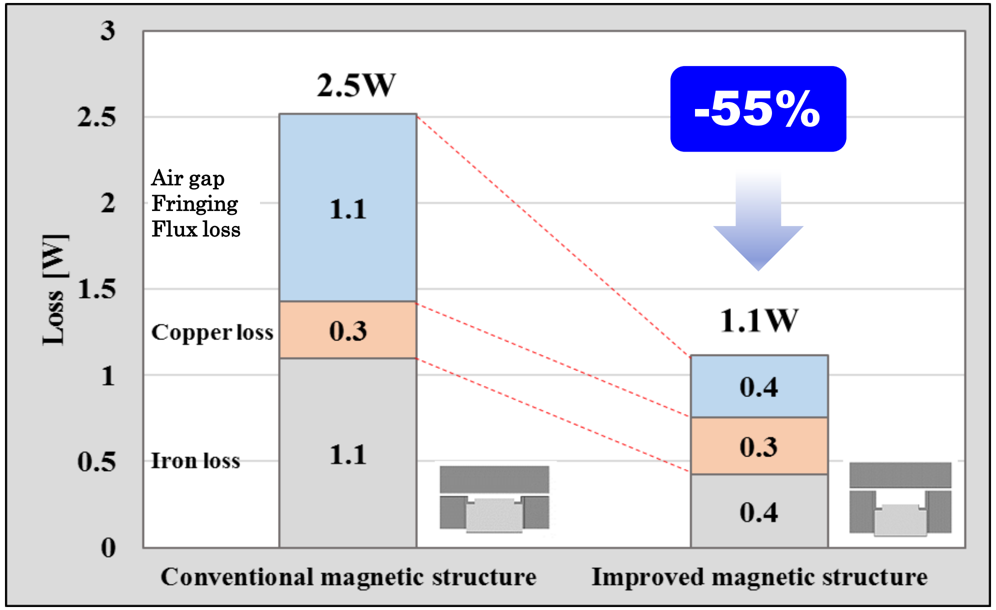
The Low Loss Orientation has:

- Low ESR
- Low ESL
- Higher SRF

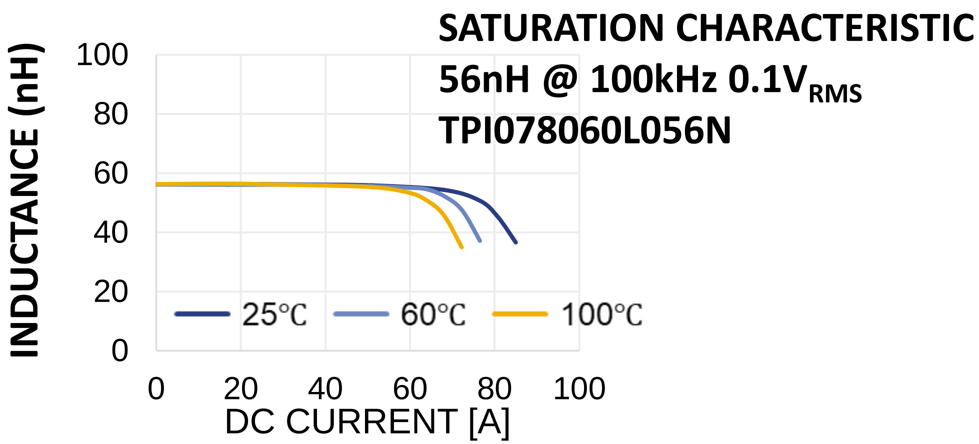


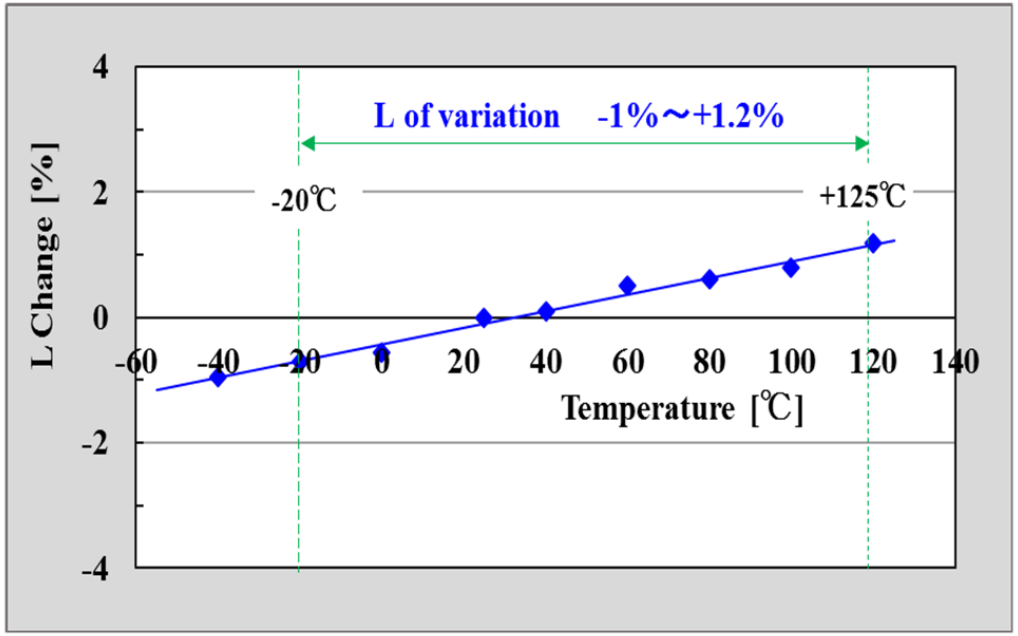


Development of Resonant Inductor



- Core loss reduced with the suitable material
- Fringing loss reduced by improved structure
- High saturation current
- Positive change of inductance with temperature compensates the negative change of U2J



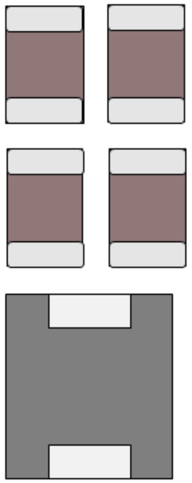


LC Module

Combine Capacitors and Inductor to achieve a smaller footprint

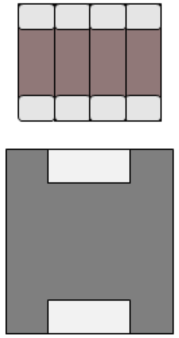
Component Footprints

Discrete 4 MLCCs & Inductor



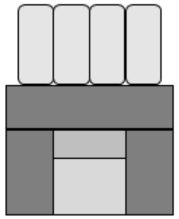
~124 mm²

Leadless Stack & Inductor



~93 mm²

LC Tank Module



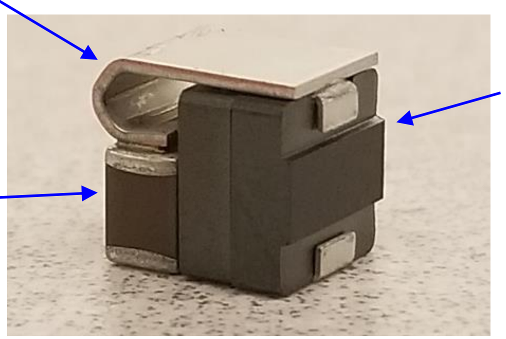
~69 mm²

Bottom Views

LC Module

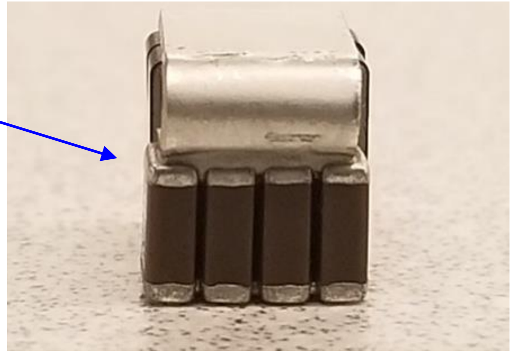
Sn Plated Cu J-Lead Connector
- Low impedance
- Machine Placeable

1812 4 Chip MLCC
- High Cap
- Low ESR



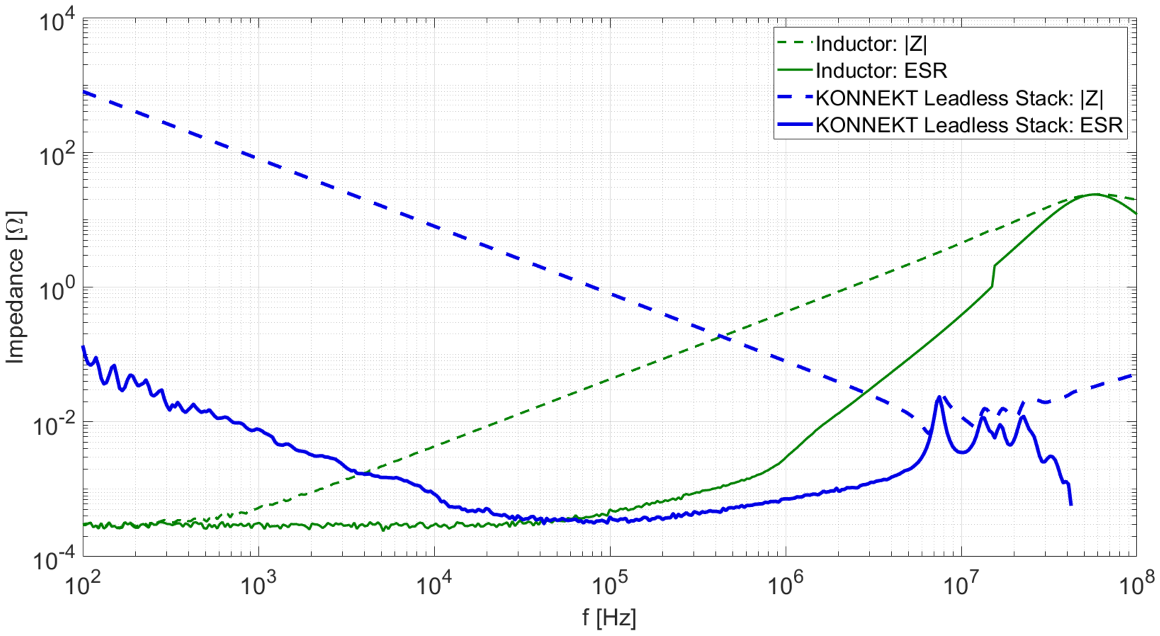
56nH SMD Chip Inductor TPI Power Series
- High switching frequency
- Low Core Loss & DCR

Assembled with KEMET KONNEKT TLPS Interface

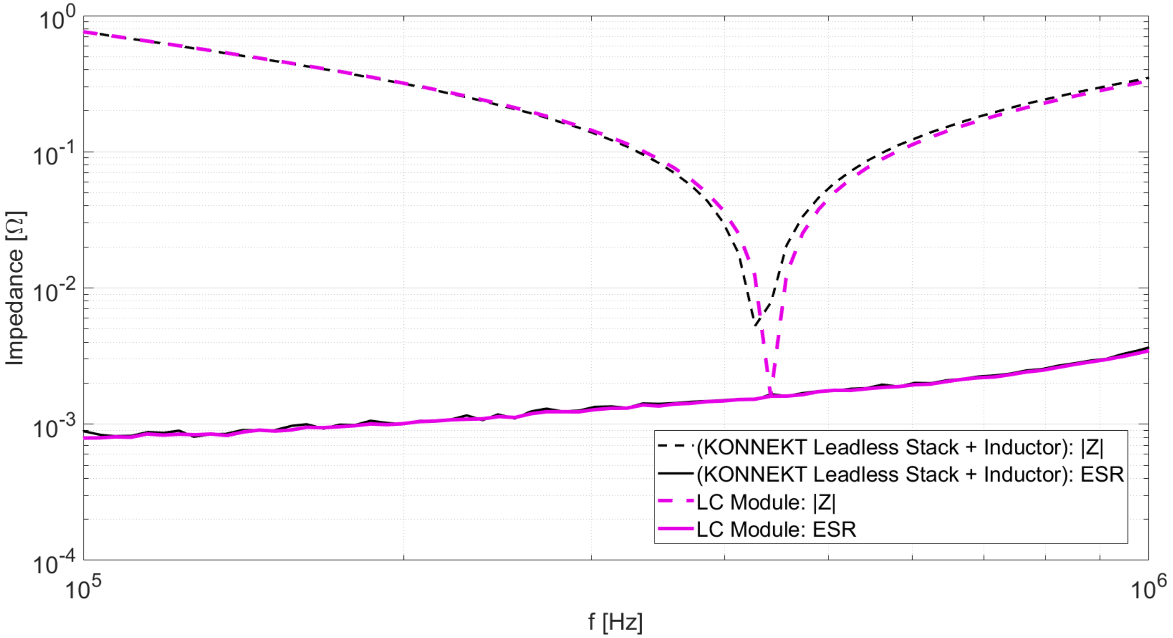


Impedance and ESR

Individual Inductor & Leadless Stack

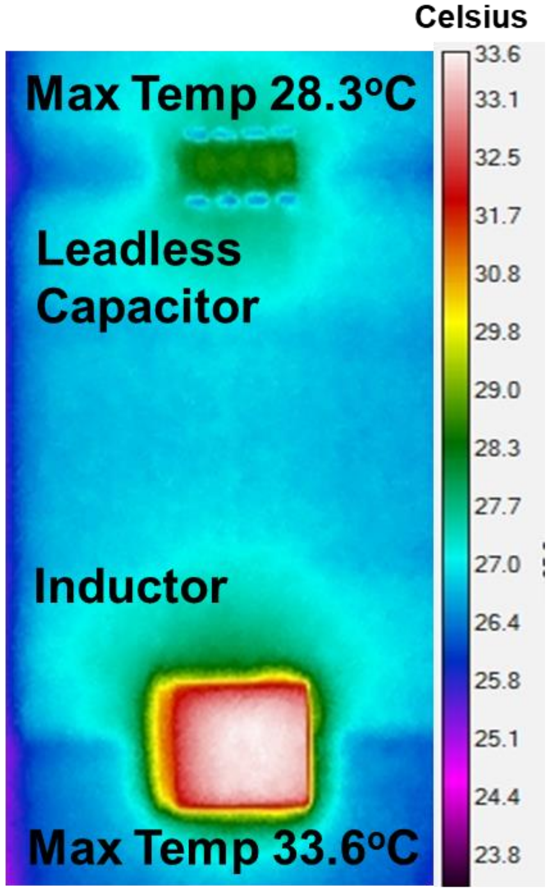


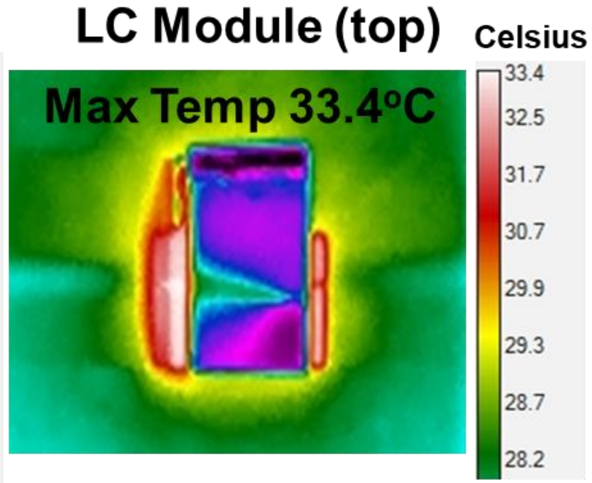
Combined Inductor & Leadless Stack Vs. LC Module

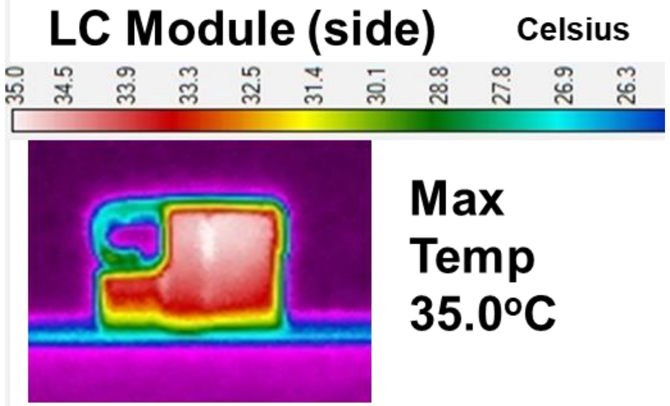


Ripple Current Heating

Leadless Capacitor & Inductor were compared to the LC Module @ 20 A_{RMS}, 270kHz







LC Module does not reach significantly higher temperatures

Capacitor Requirements for Higher Power

KEMET CHARGED.®

Higher Switching Frequencies
20kHz → 100kHz → 10 MHz

➡ **Smaller, low ESR, low ESL low loss capacitors with high dV/dt, dI/dt & current handling capability**

Higher Operation Voltages
450V → 900V →1200V→1700V

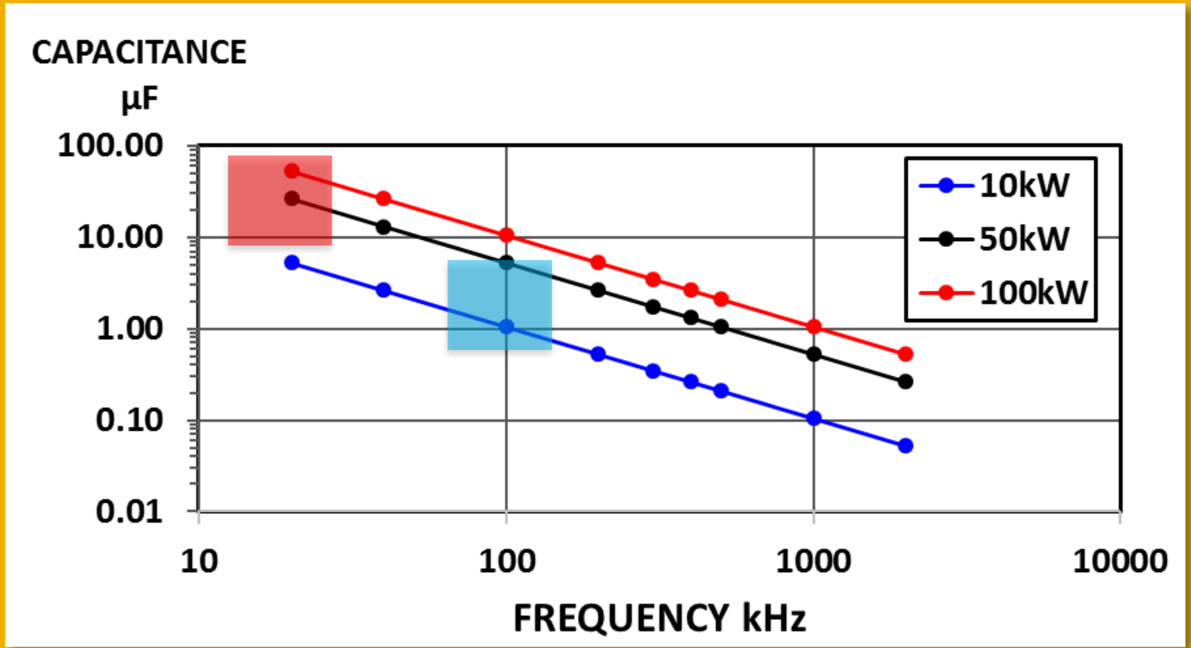
➡ **Reliable performance at higher voltages**

High Junction Temperatures
105ºC → 125ºC → 150ºC→ 200ºC+

➡ **Reliable performance at elevated temperatures ≥ 125ºC with robust mechanical performance**

- **Packaging close to the hot semiconductor to:**
  - **Lower ESL**
  - **Minimize cooling costs**

$$C = \frac{P_{load}}{U_{ripple}\left(U_{max} - \frac{U_{ripple}}{2}\right) 2\,\pi\, f_{rectifier}}$$



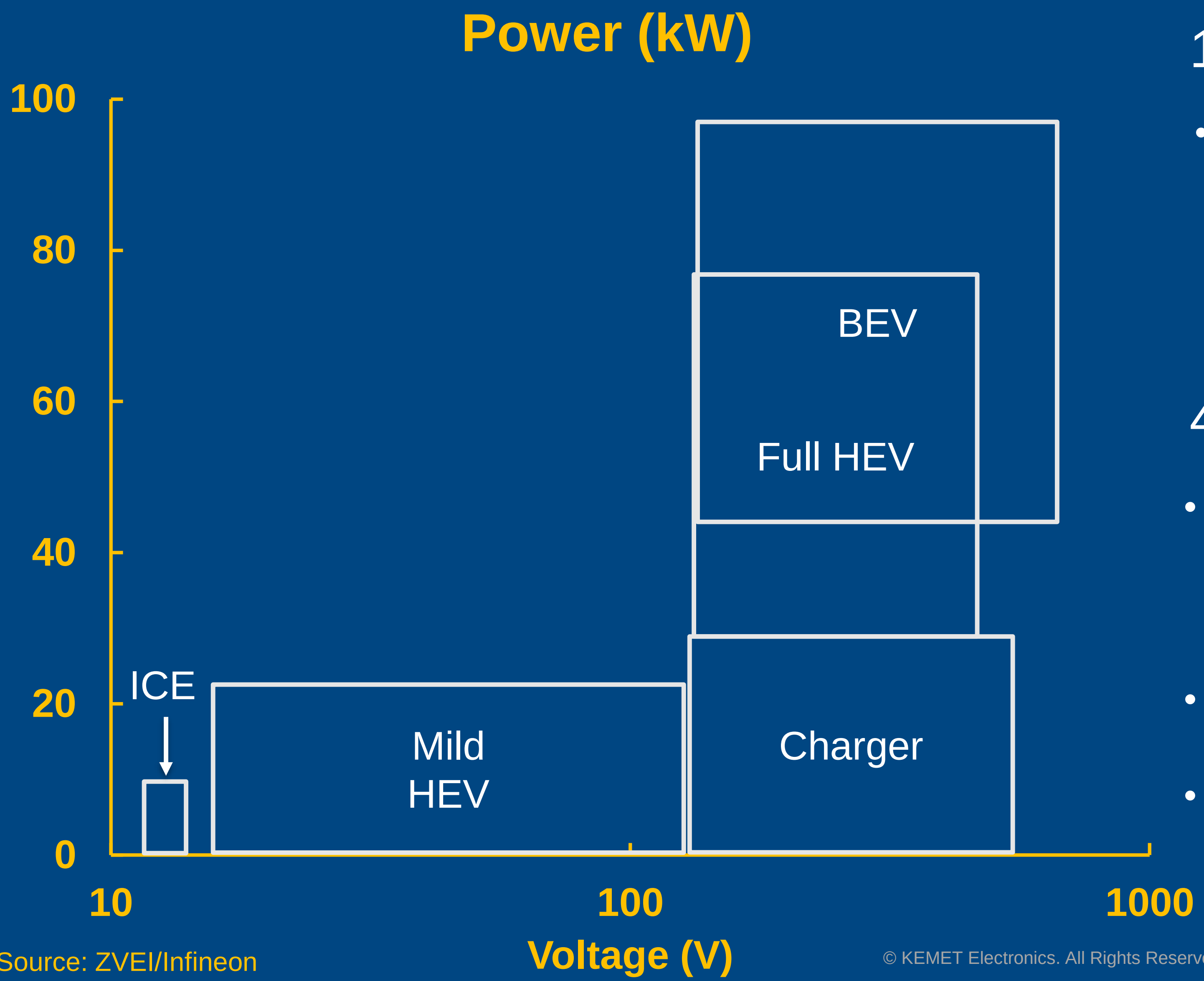
Example: DC Link for 400V with 10% Ripple

Film or Electrolytic

Ceramic

Source: Modified from Prof. R. Kennel, Technical University Munich, Germany

Higher Voltages - Automotive Power Requirements



Source: ZVEI/Infineon

12V → 48V

- Provide higher power
  - While current lowered
  - Brake recuperation
  - Air and heaters
  - Hybrid motor

450V → 900V

- Provide higher power
  - While current lowered
  - Faster charging

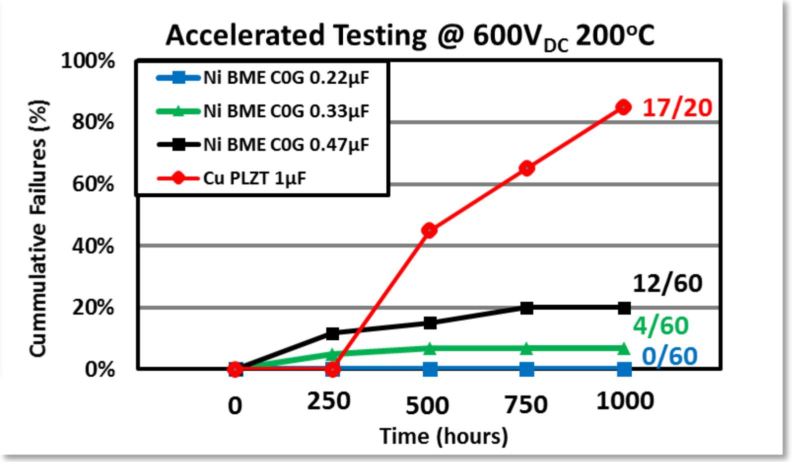
- MLCC using U2J dielectric are currently limited to < 200V temperatures to 125^{o}C
- Development of C0G Ni BME MLCC

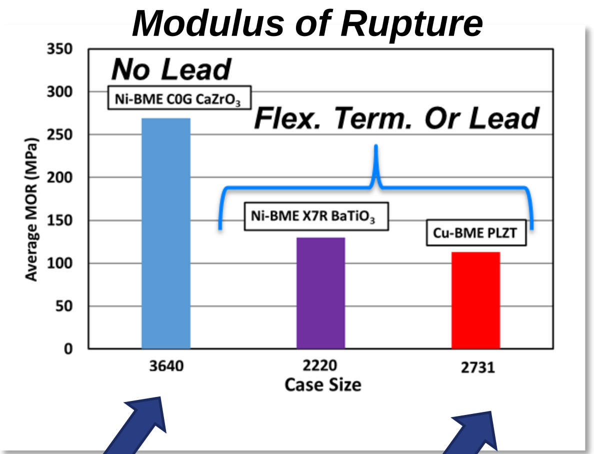
Performance Comparison

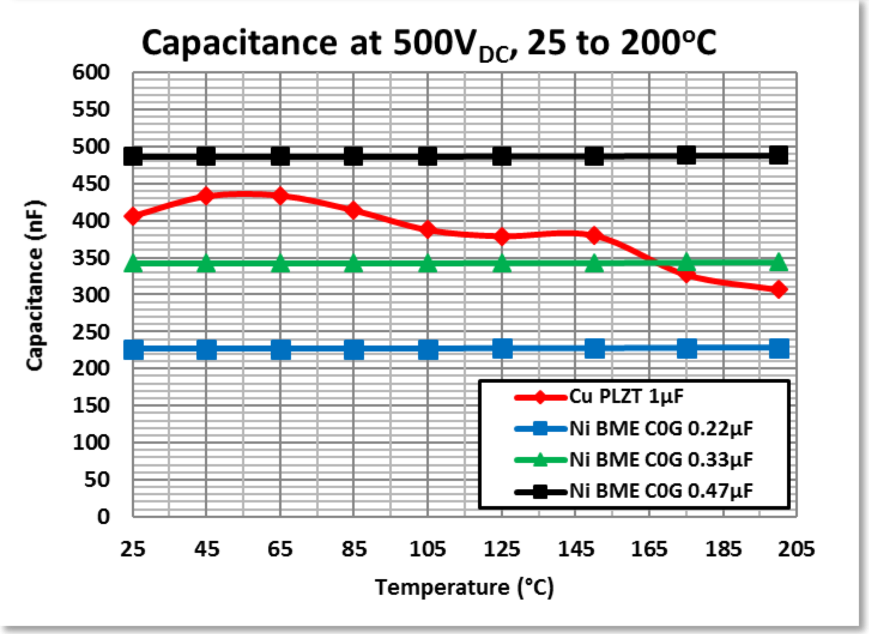
3640 Ni BME C0G vs. Competitor Cu PLZT

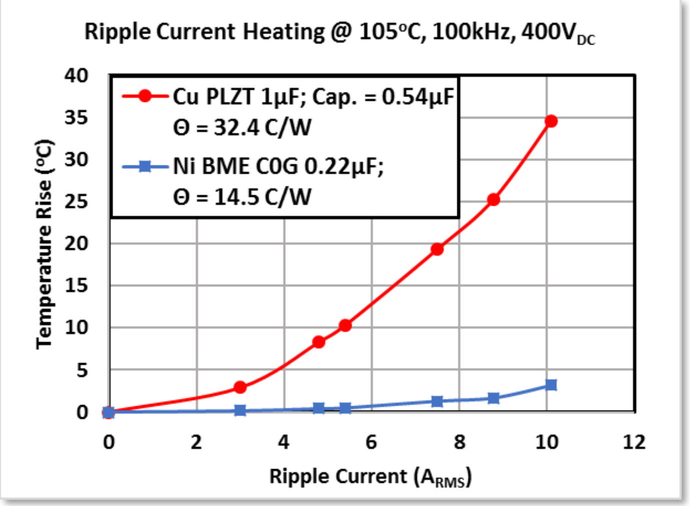
3640 0.22µF Ni BME C0G has:

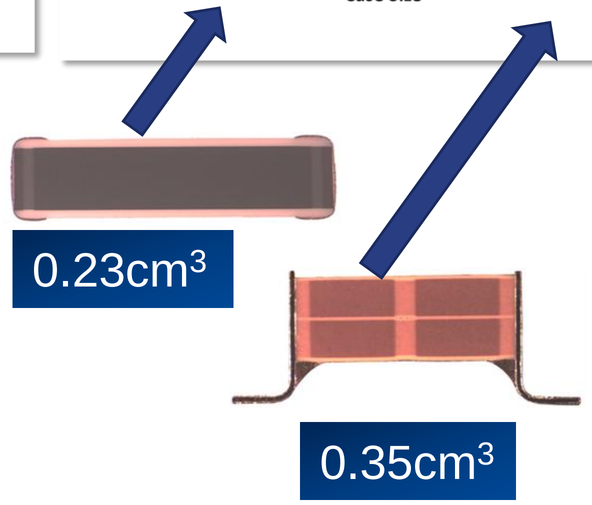
- Better accelerated life
- Stable cap. with temp. & voltage
- Less ripple heating
- High MOR
- > 0.22µF with Leadless Stack Solutions











[3] ***J. Bultitude et al, "An evaluation of BME C0G multilayer ceramic capacitors as building blocks for DC-Link capacitors in 3-D power electronics", Proceedings 3D Power Electronics Integration and Manufacturing, June 13-15, 2016, Rayleigh, NC, USA.***

Ni BME C0G MLCC 3640 0.22µF 500V 150ºC

ESR & Current Handling @ 150ºC 100kHz

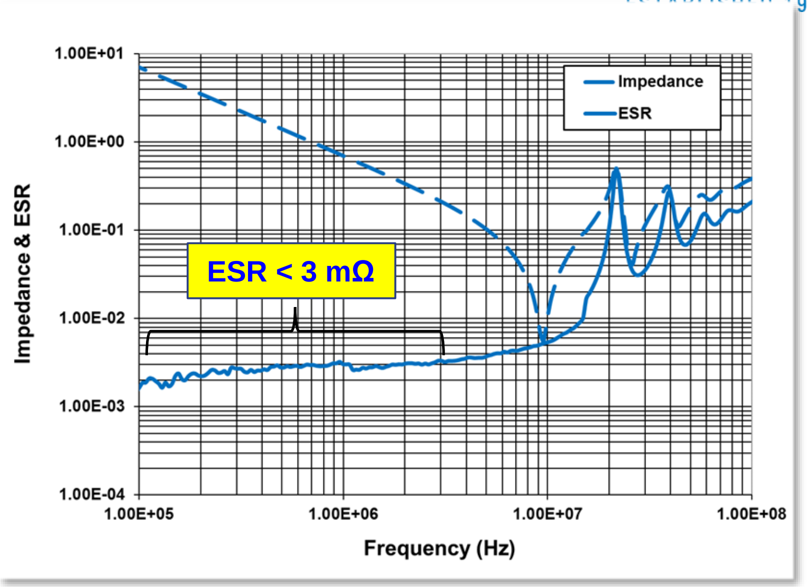
- Lower DF & ESR reduce the power dissipated

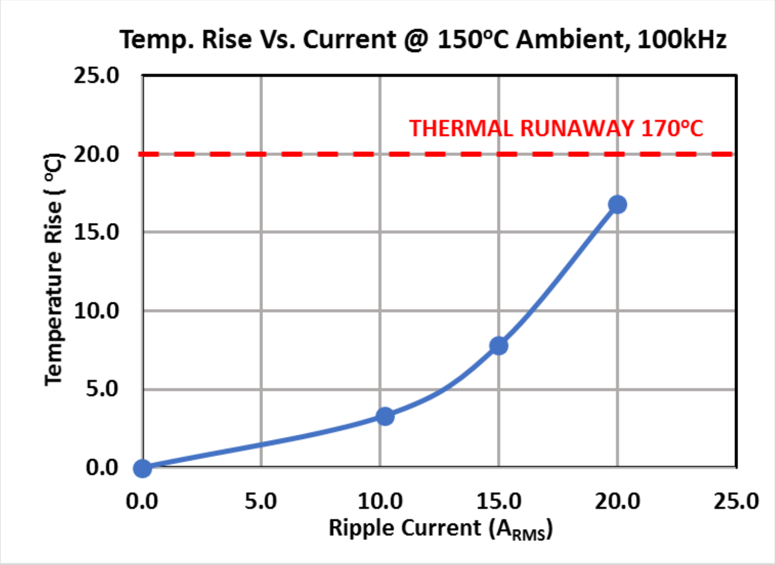
$$P = \frac{i^2 d}{2\pi f C} = i^2 R$$

P = power dissipated
i = current
d = dissipation factor
f = frequency
C = capacitance
R = resistance, ESR

Ripple Current Life Testing

- No failures after 1000hrs @150ºC
  - 15A_{RMS} 100kHz
  - 10A_{RMS} 100kHz with 400V_{DC} Bias

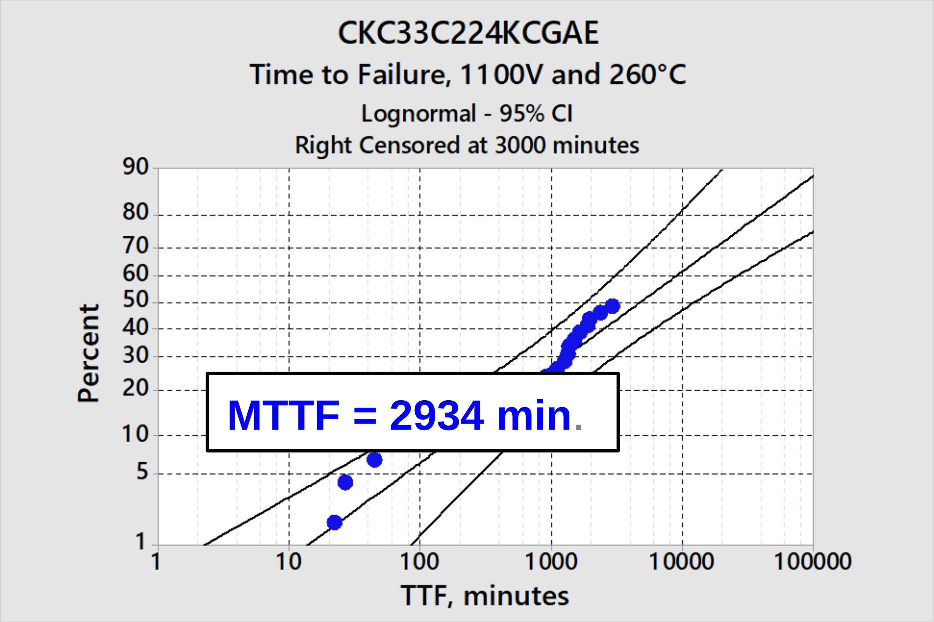


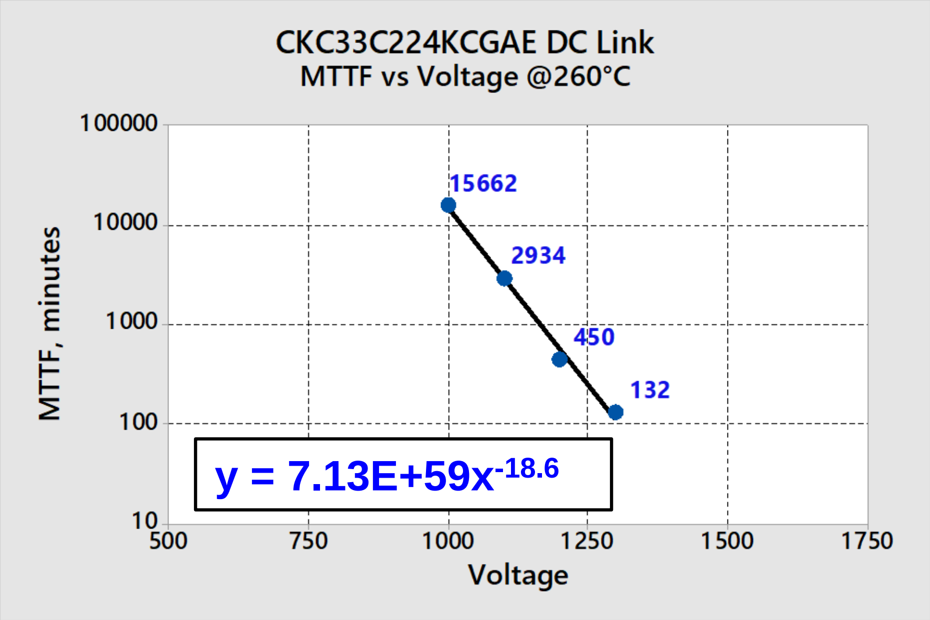


3640 0.22µF 500V Ni BME C0G for 150ºC

Temperature Accelerated HALT

- MLCC were HALT tested at 260ºC at 1000, 1100, 1200 & 1300V_{DC} (n = 40, with Au term.)
- MTTF Vs. Voltage was recorded
- Voltage exponent ~ 19 @ 260°C
- Calc. MTTF @ 500V_{DC} ~ 8500 years

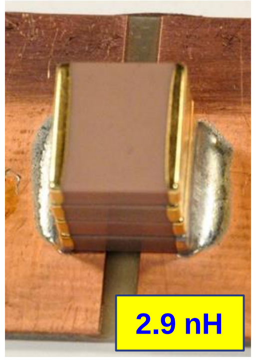


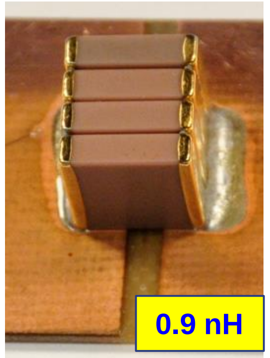


0.88µF Leadless Stacks (4 X 3640 0.22µF 500V)

Orientation: Traditional Vs. Low Power Loss

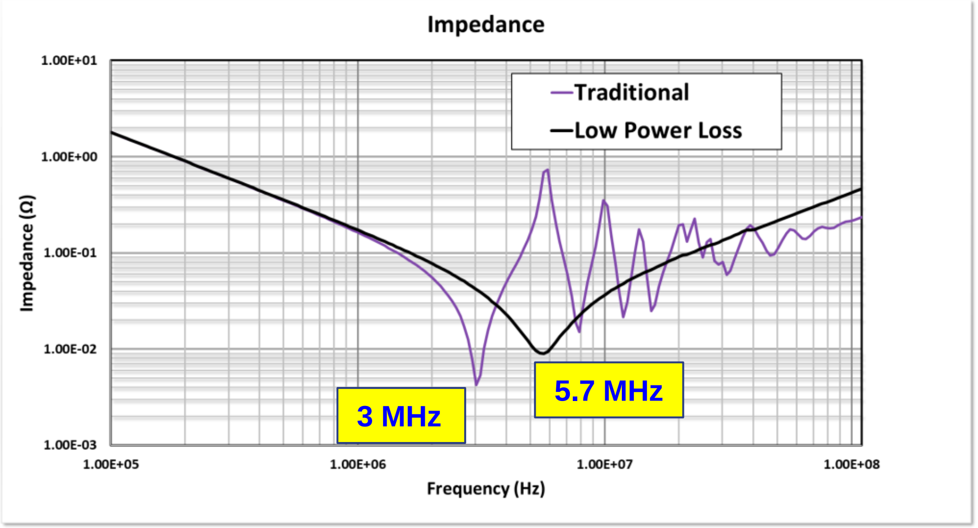
Traditional | **Low Power Loss**

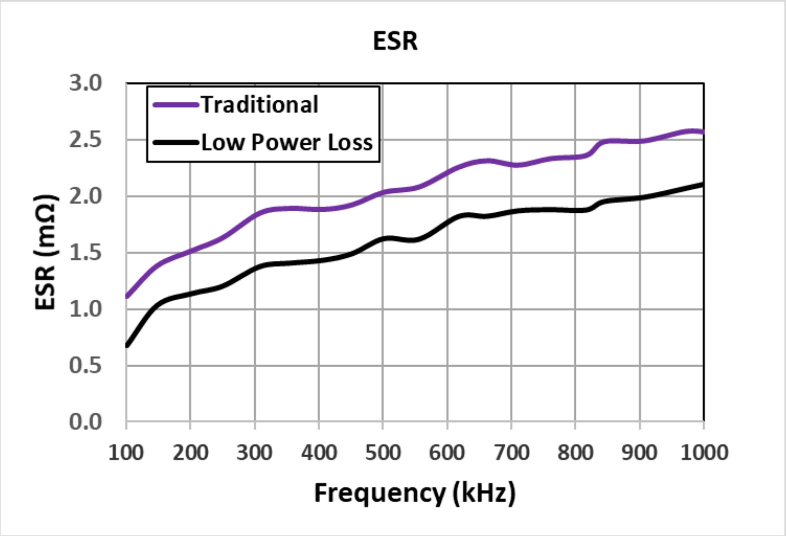




Low Loss Orientation has:

- Higher SRF
- Lower ESR





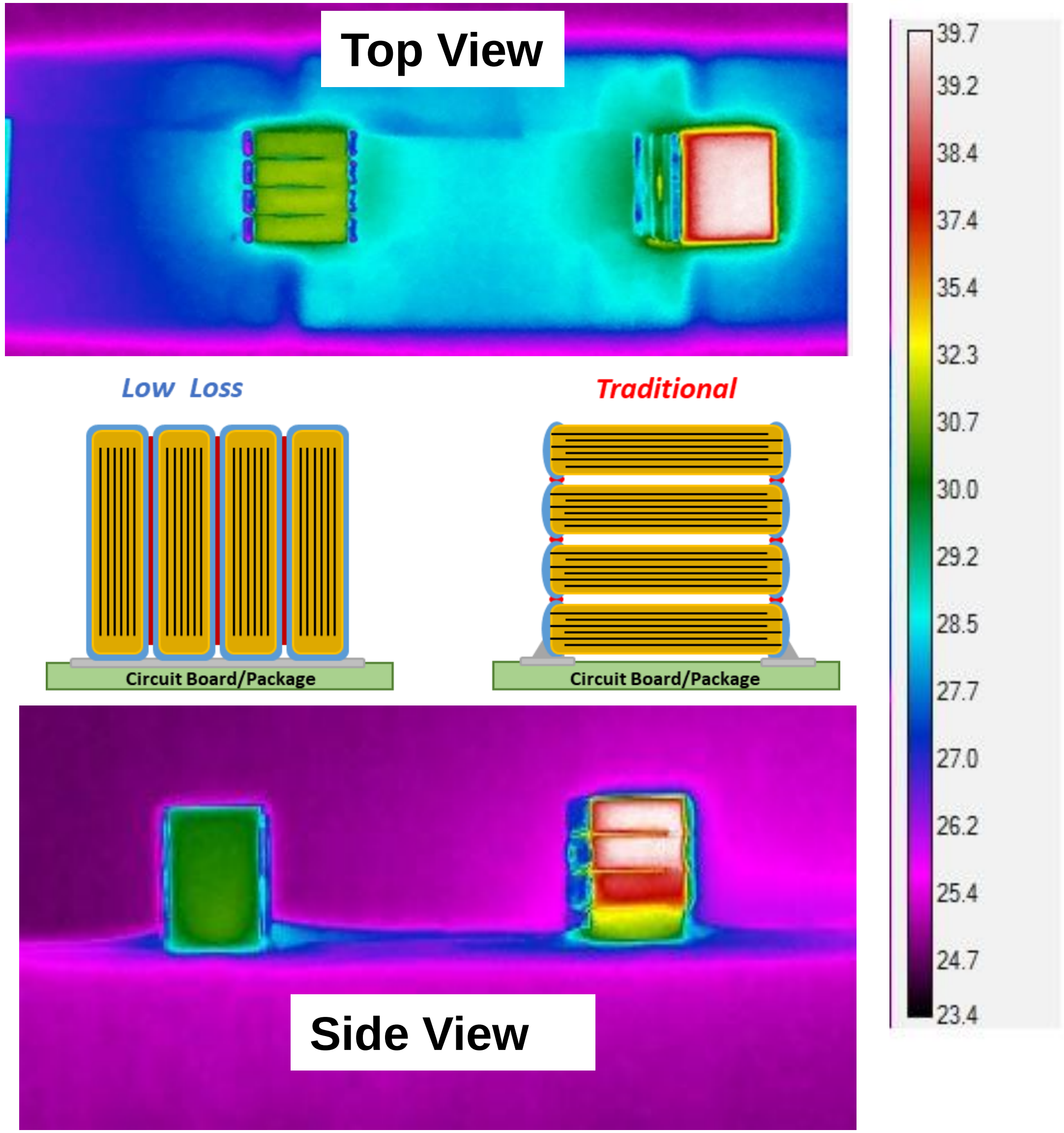
[4] J. Bultitude et al, "Development Challenges for DC-Link Capacitors for Wide Band Gap Semiconductor Applications", 3D Power Packaging Industry Session, APEC 2017, March 26-30, Tampa, FL, USA.

0.88µF Leadless Stacks (4 X 3640 0.22µF 500V)

Ripple Current Heating: Traditional Vs. Low Loss Mounting

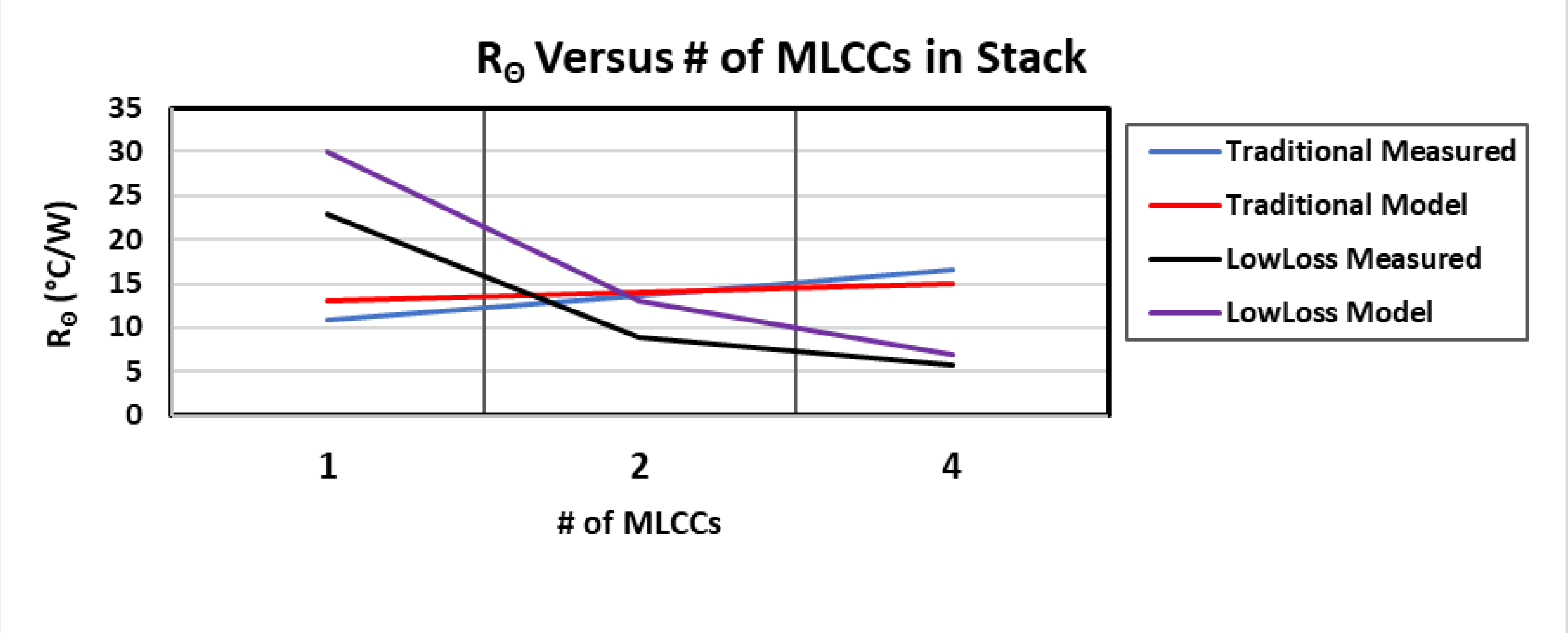
At $20A_{RMS}$ @ 300kHz Low Loss Orientation has:

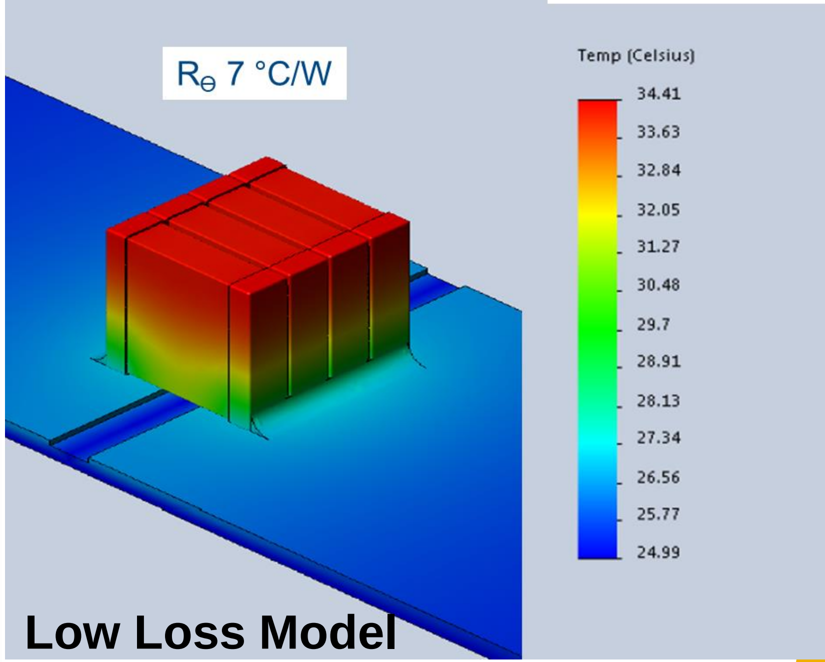
- Lower Temperature
- More even heating



Thermal Modeling

3640 0.22µF 500V; 2 & 4 chip Leadless Stacks





Study thermal resistance with other boundary conditions

- Forced air cooling or dielectric fluids
- Embedded in package

UNDER DEVELOPMENT KEMET

*[5] **A. Templeton et al, "Thermal Modeling Challenges for Multilayer Ceramic Capacitors (MLCCs) in High Power Density Assemblies", To be presented 3D Power Packaging Industry Session, APEC 2019, March 17-21, Anaheim, CA, USA.***

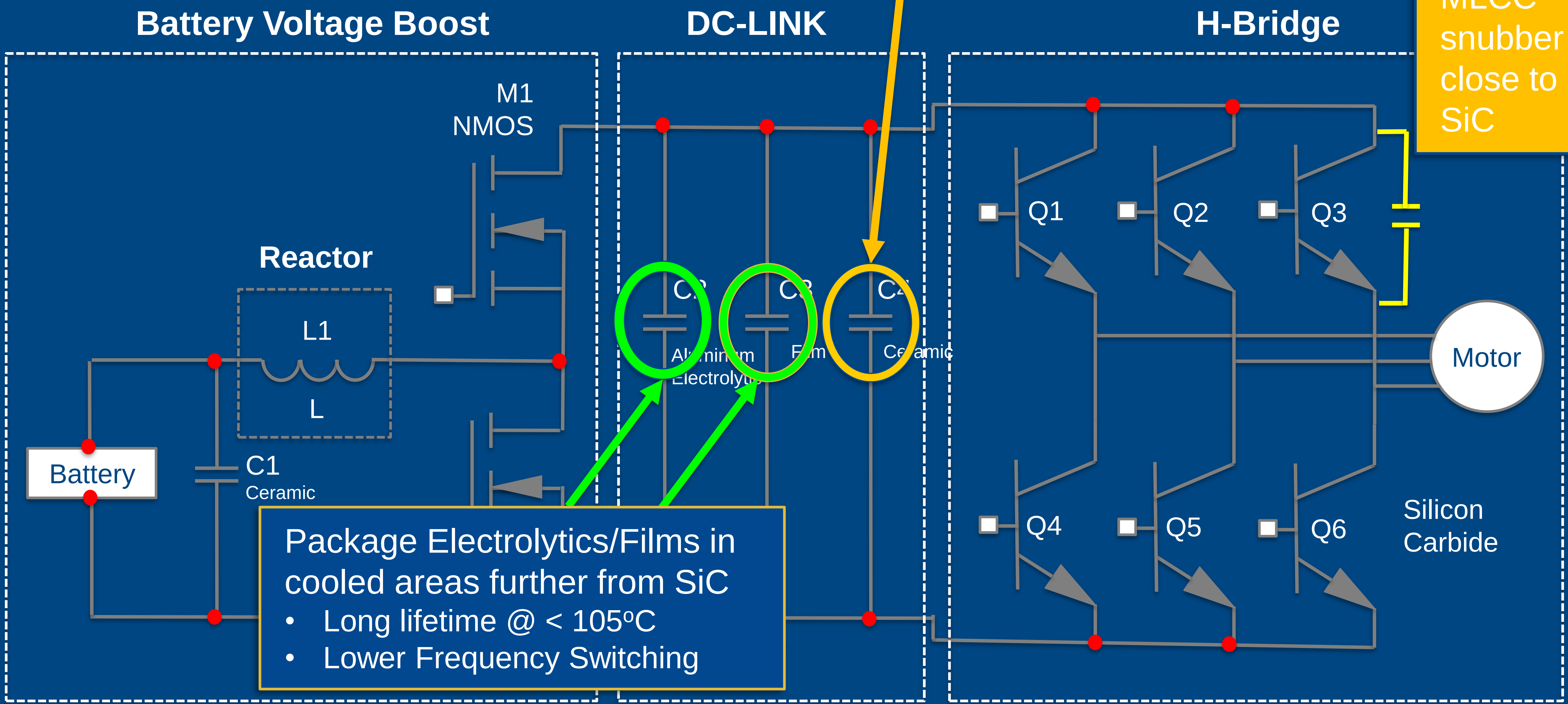
Inverter Capacitor Trends

DC-Link Hybrid Inverter & Snubber

Package MLCC close to SiC

- Long lifetime @ 150°C
- Higher Frequency Switching

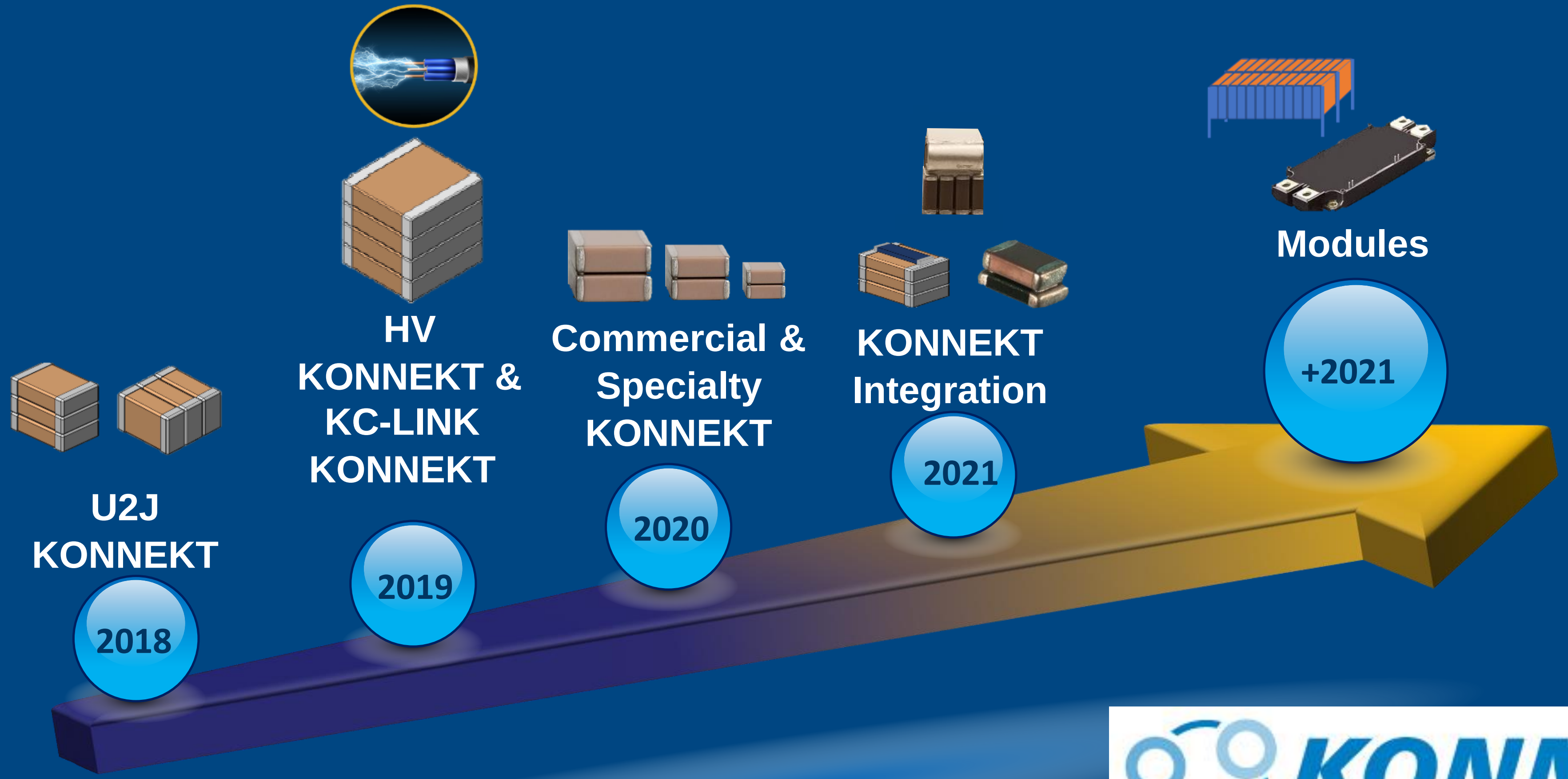
MLCC snubber close to SiC



Package Electrolytics/Films in cooled areas further from SiC

- Long lifetime @ < 105°C
- Lower Frequency Switching

Packaging Roadmap



KONNEKT™
High Density Packaging

Thank You!

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