3D-PEIM 2016

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Novel Packaging and Thermal Measurement for 3D Heterogeneous Stacks

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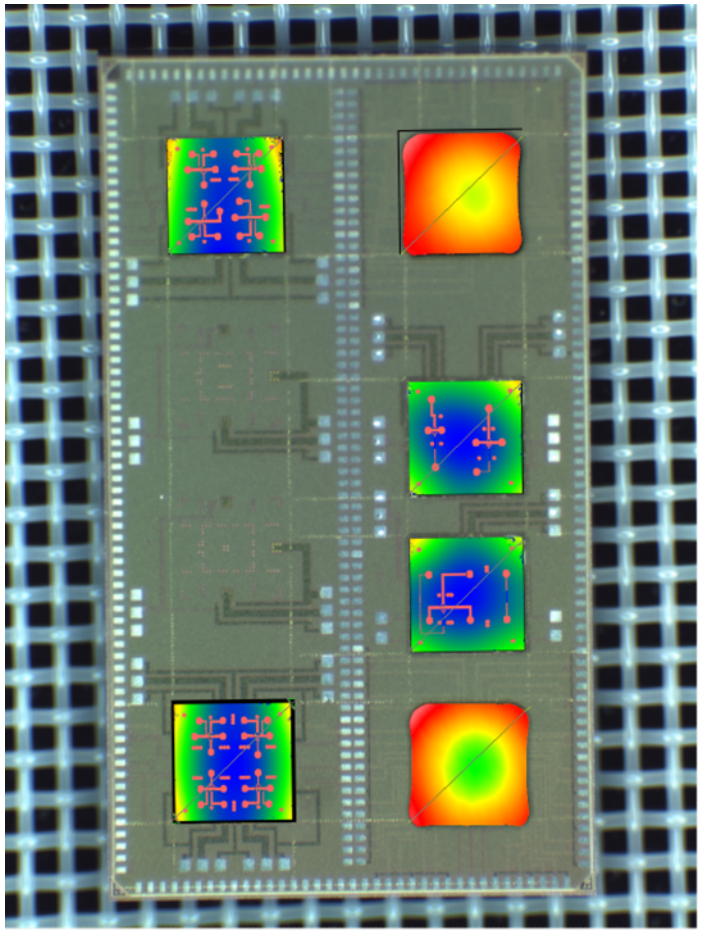
Outline

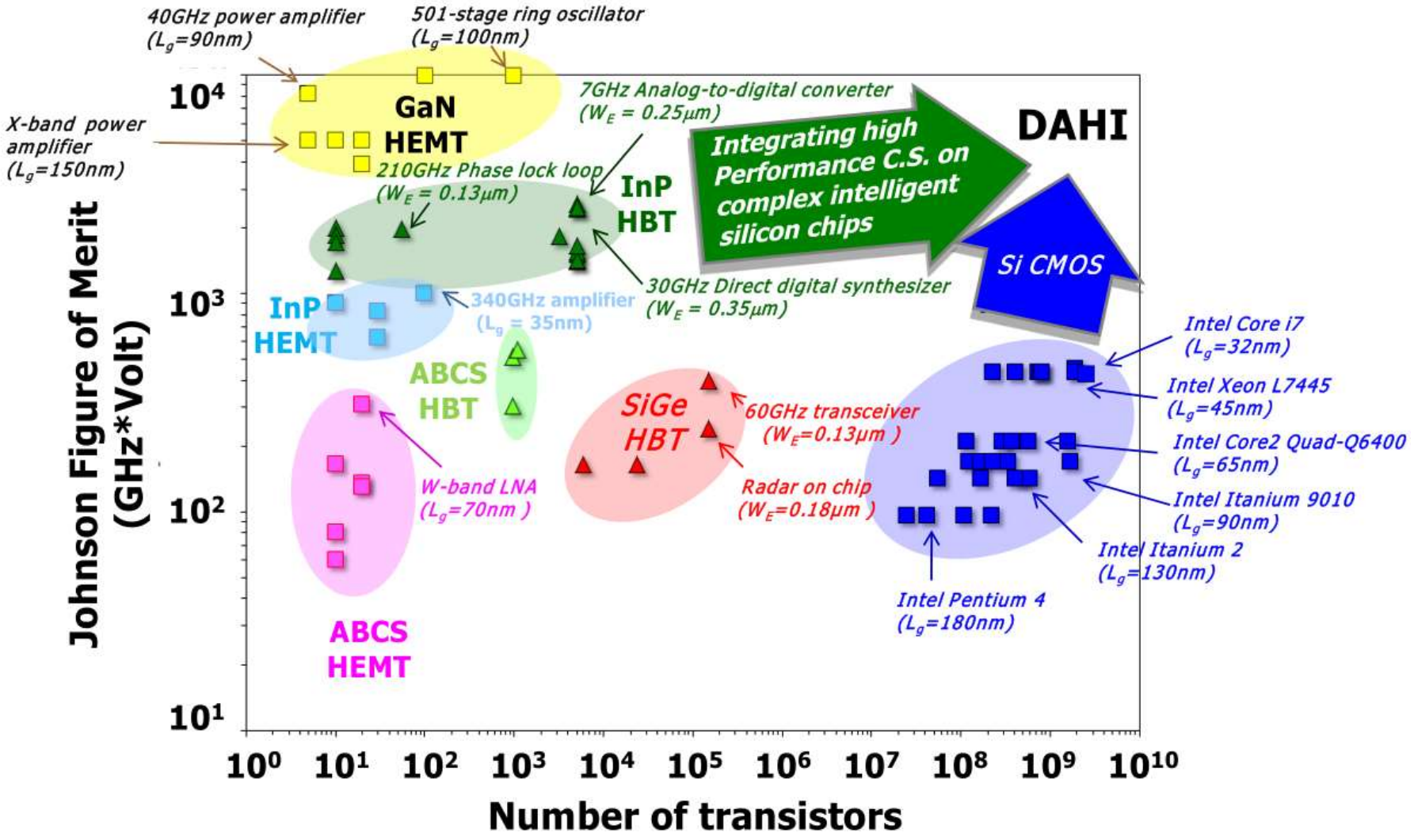
DAHI Program

I. Background
II. Heterogeneous Interconnect
III. Thermal Modeling
IV. Stress Strain Modeling
V. Measurements

Summary



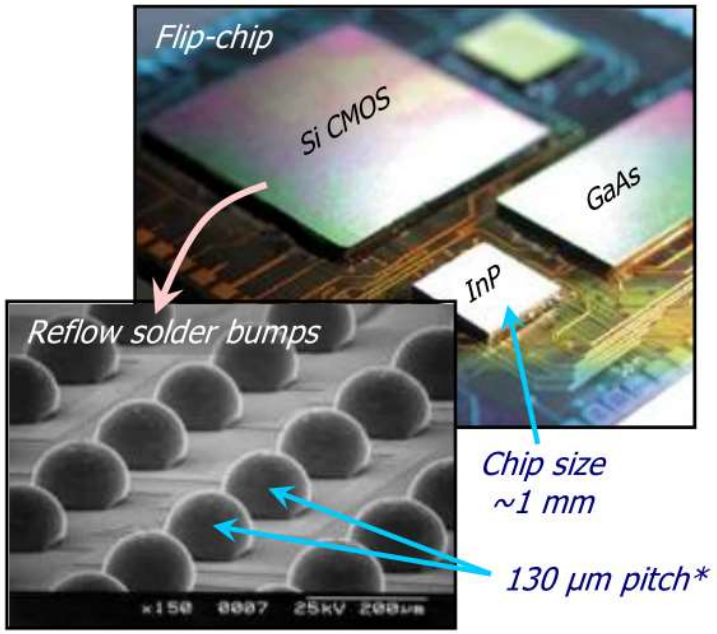
Johnson Figure of Merit Motivation for DAHI Capability



Slide Source: DARPA Public BAA

Diverse Accessible Heterogeneous Integration (DAHI): Objective

SM BGA



Practical heterogeneous integration historically limited to package level (multi-chip modules) for high-speed RF/mixed-signal applications. Drawbacks:

- I/O parasitics between chips degrade performance.

Source: DARPA Public BAA

DAHI: Heterogeneous InterConnect (HIC)

Why study the HIC?

- Mechanical attachment
- Source of stress/strain
- Thermal bottleneck

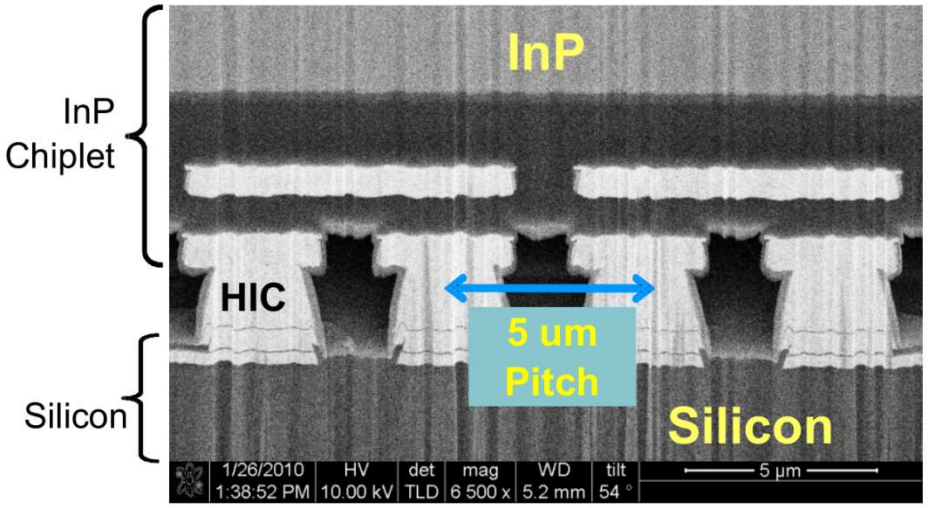
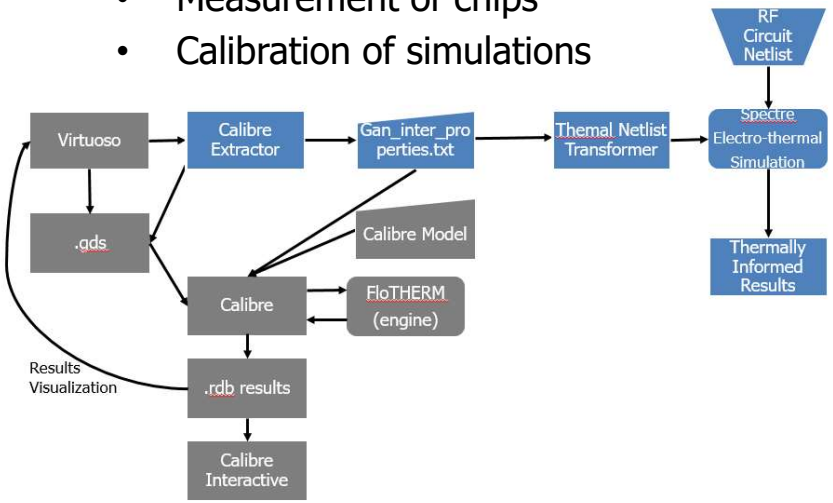


Image Source: Advanced Heterogeneous Integration of InP HBT and CMOS Si Technologies, Augusto Gutierrez, *et. al.*

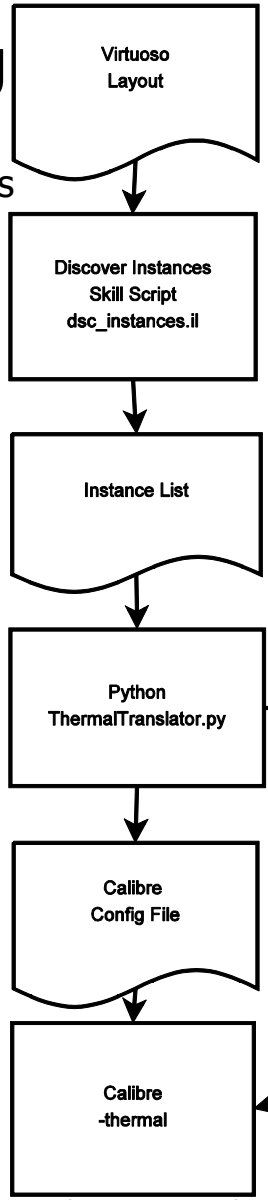
Flow development for HIC and power source placement and simulation

Our Role in Thermal Modeling

- Flow development
- Act as an intermediary between designers and software developers
- Develop scripts for automation
- Produce DAHI thermal simulations
- Validate software models against other methods
- Measurement of chips
- Calibration of simulations

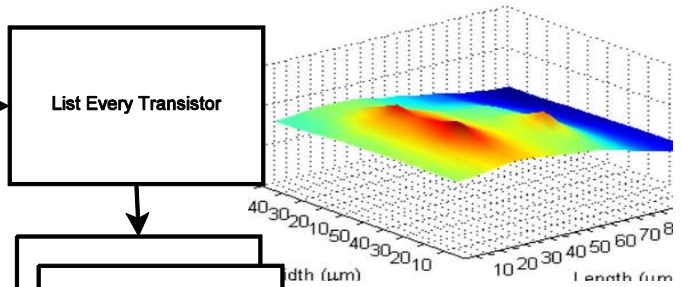


Current CAD Flow



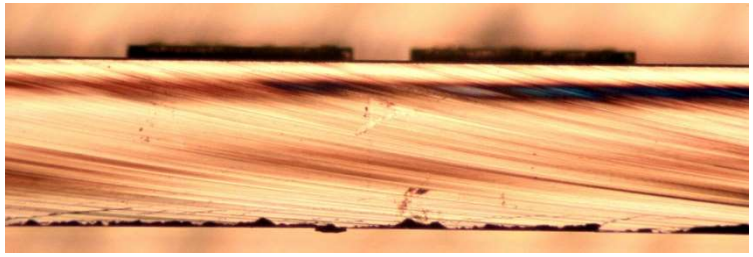
Flow Example

- Two approaches to HIC simulation placement:
  - HIC locations can be automatically placed with correct thermal properties.
  - Extracted material properties are mapped by layer.
- Most important factors are taken into account: HIC and transistor locations.

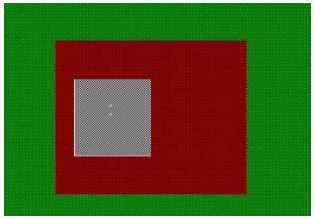


Project Sahara flow description

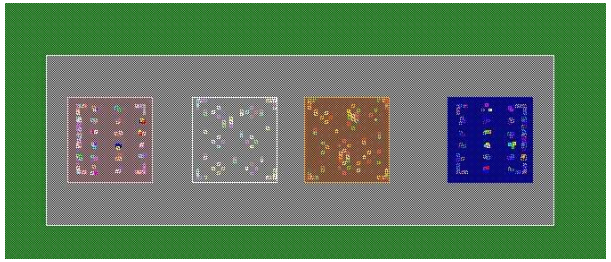
Importance of Whole Chip Analysis



DAHI Stack

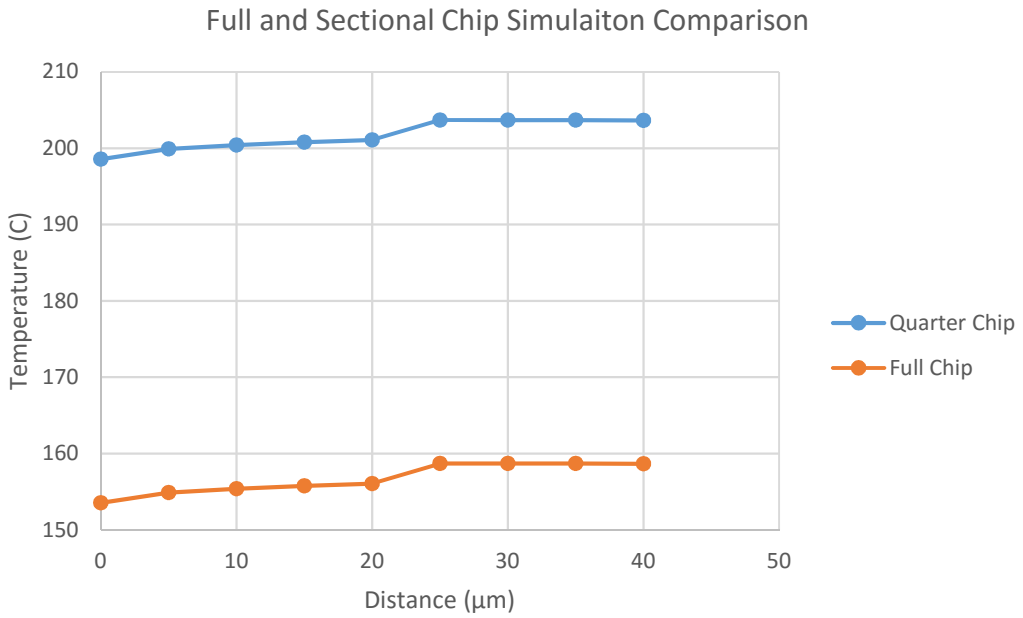


Partial model saves CPU time



Full model takes far-field effects into account

Detailed FEM analysis may not be suitable for layout design iteration



Simulated data of a section of a simplified DAHI chip compared with a full chip simulation results in incomplete results due to heat spreading effects.

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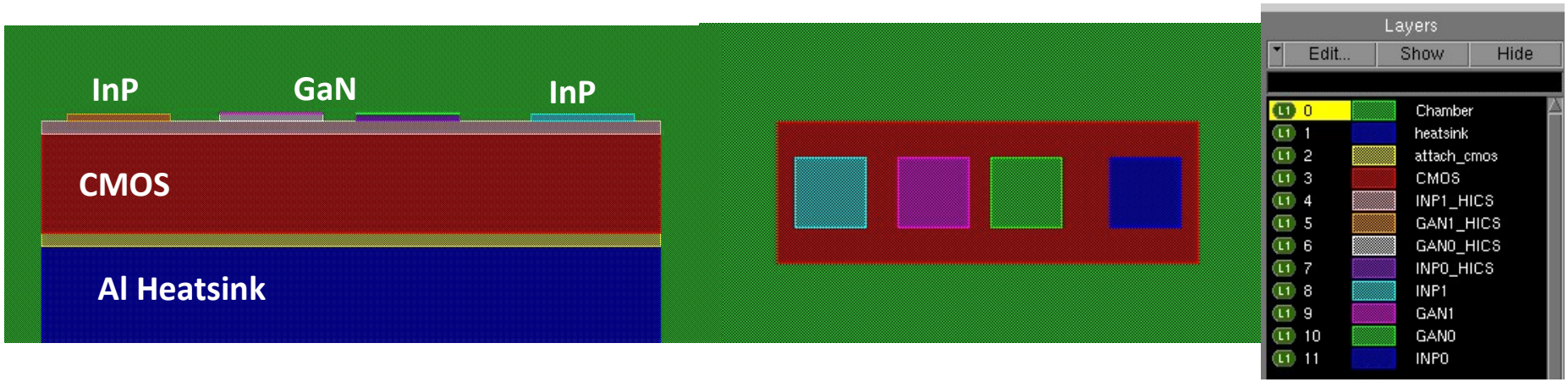
NCSU Thermal Test Vehicle

Simulate -> Electrical Measurement -> Thermal Measurement



Simulate ⇨ Electrical Measurements ⇨ IR Emissivity Measurements

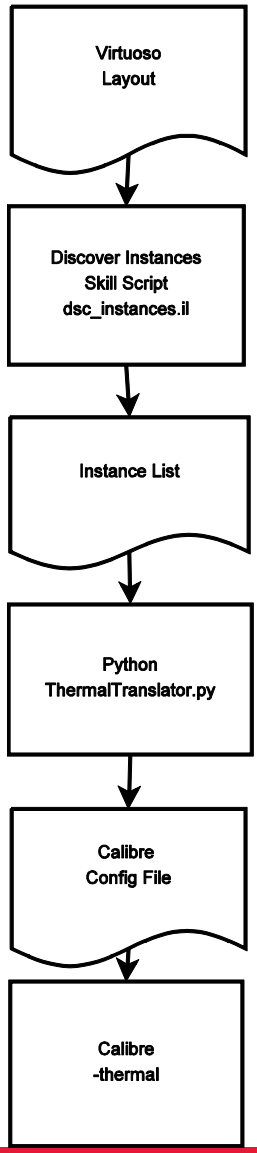
- Diode sensors from AFRL
- IV Curves are temp dependent

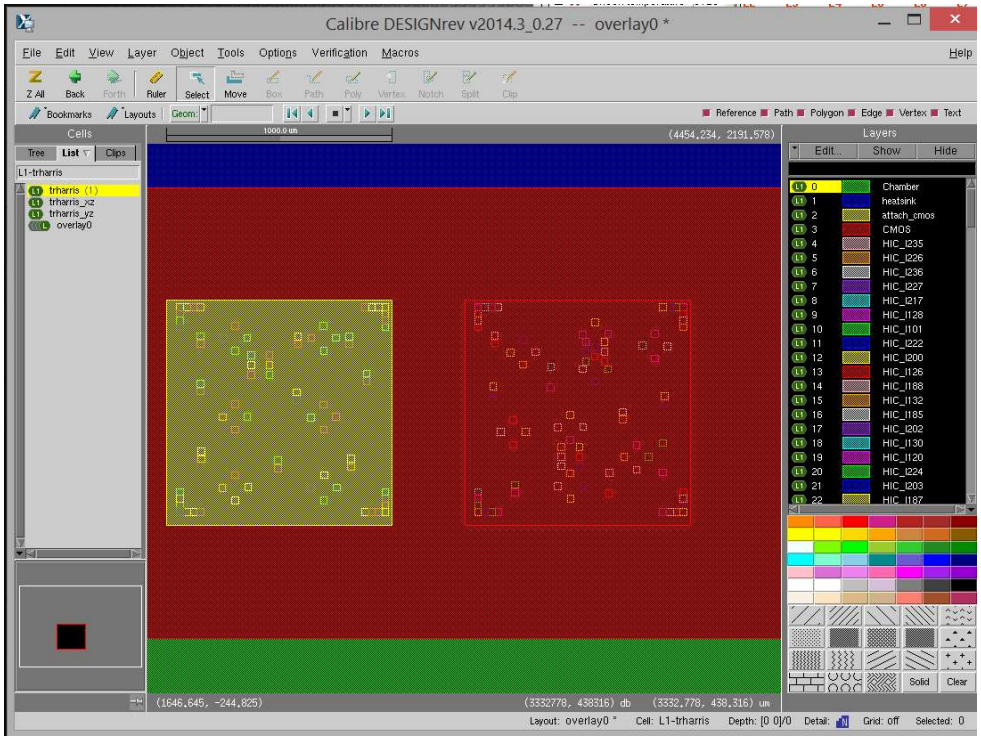
- Surface temperature

Improvement of Simulations

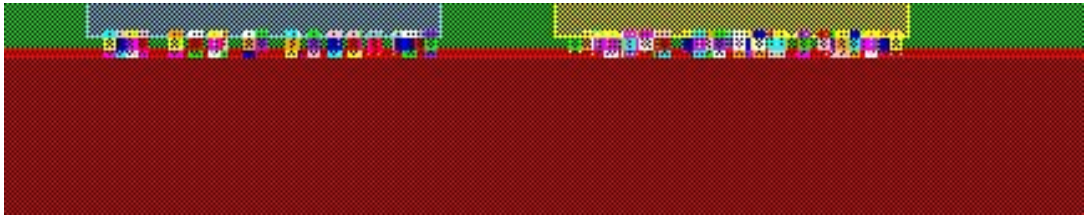
Accurate Predictions

HIC Locations Included by ThermalTranslator.py





Top down view



Cross-sectional view, with HIC placement

In this approach, HIC locations can be accurately placed with correct thermal properties

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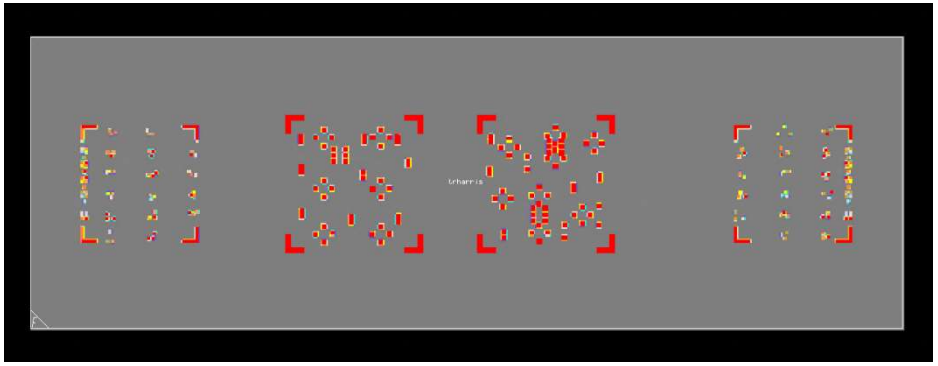
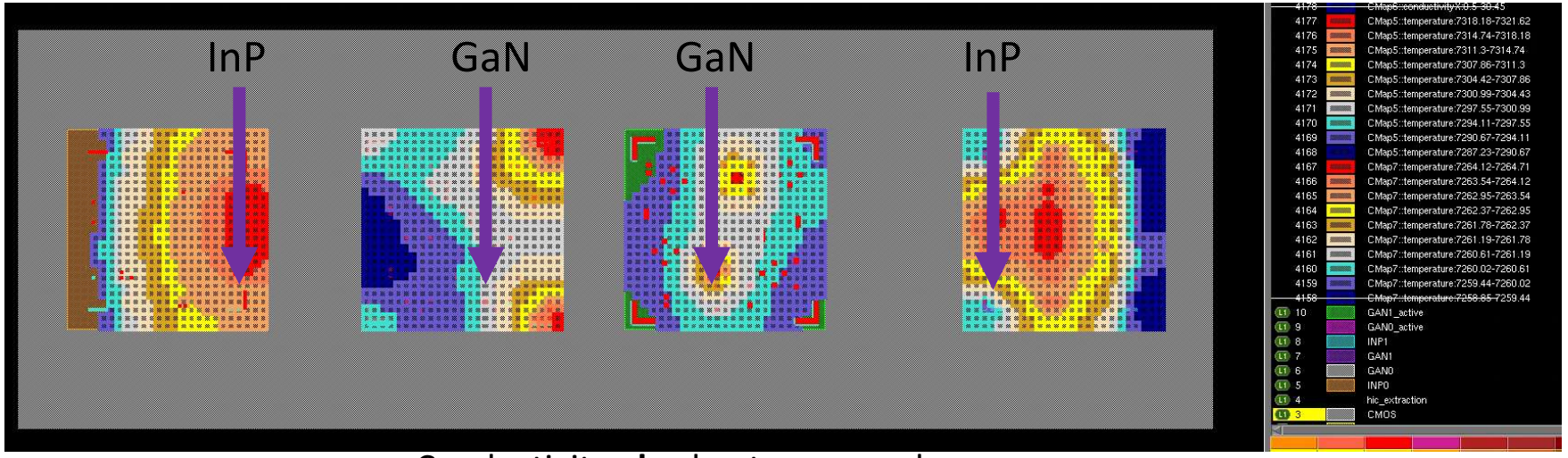
EFFP Thermal property extraction



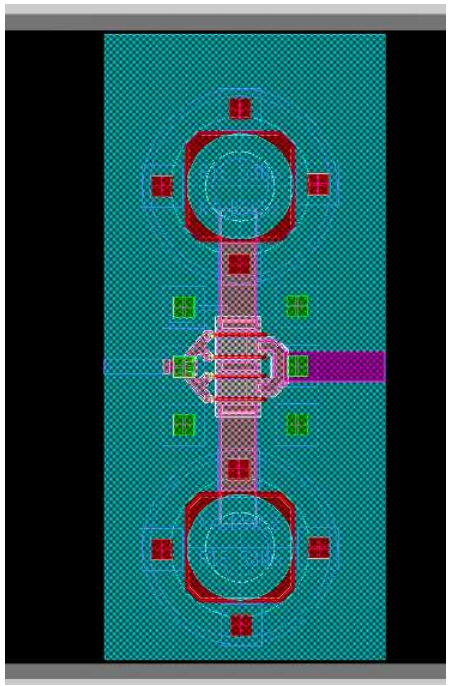
Extracted CMOS metal layer x-conductivities reveal HICs



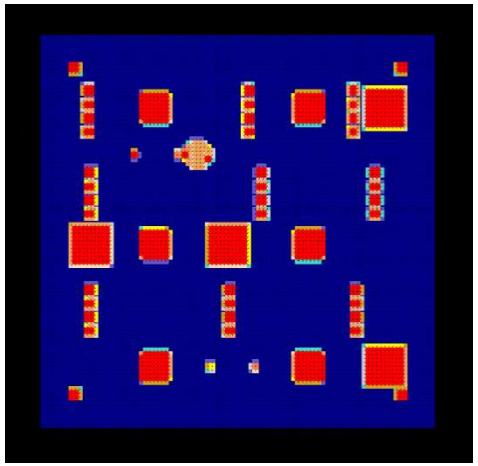
Conductivity **plus** heat map overlay

Extending EFFP Thermal Property Extraction

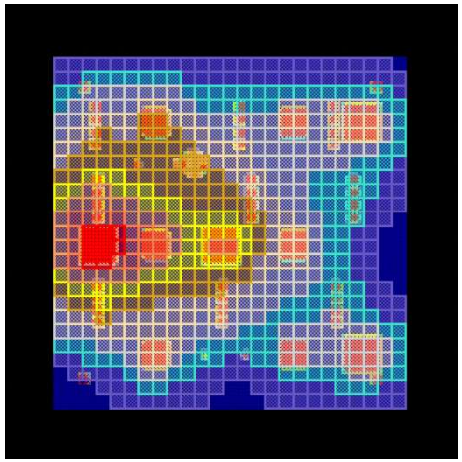
- Using Sahara® FloTHERM ® to extract GaN20 chiplet
- Cross-referencing with layout in Cadence® to verify layers
- Thicknesses come from NGAS process spreadsheets
- Properties of materials from online reference tables, including nonlinearity



Extracted section of GaN chiplet



High thermal conductivity areas above the SiC bulk



Thermal simulation results

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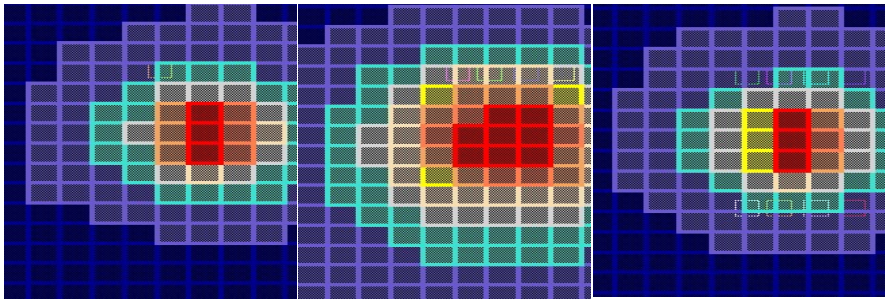
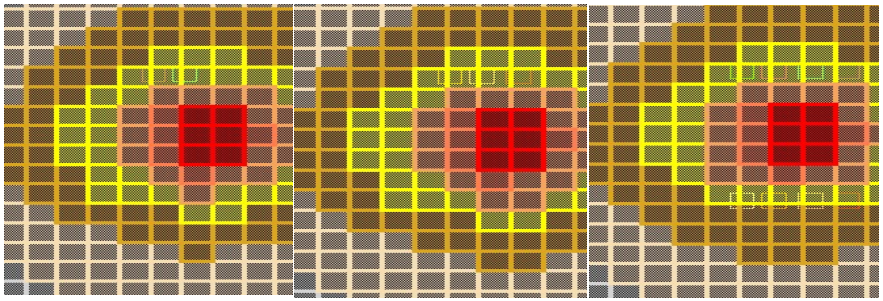
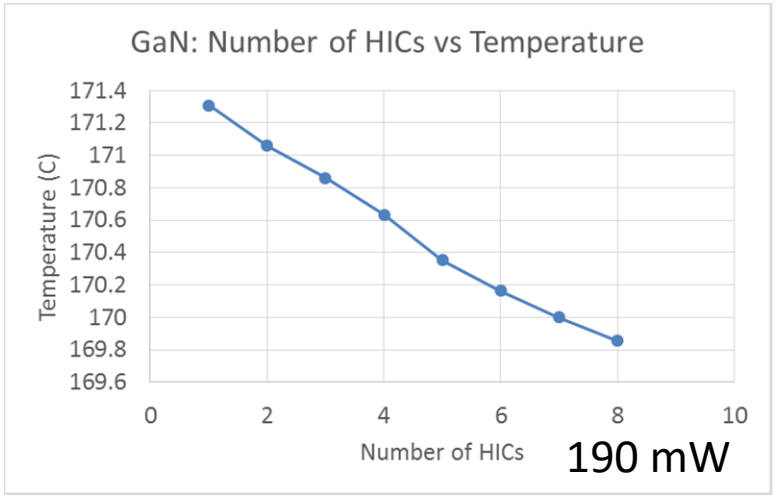
GaN vs InP HIC Number Variation with Corner HICS and Hotspot Averages

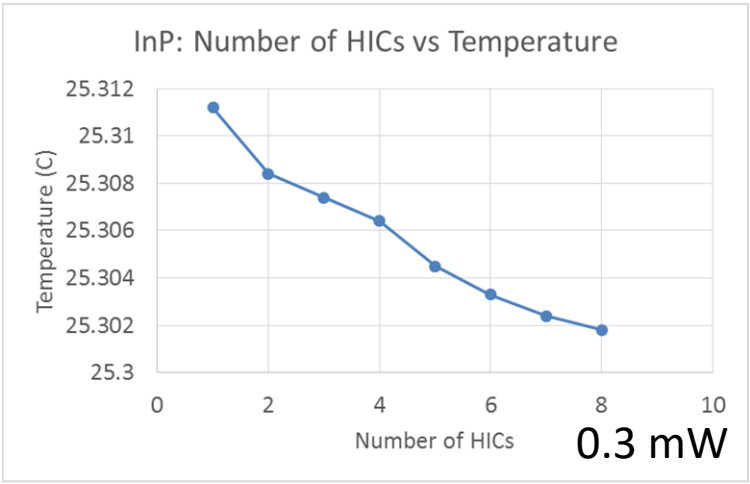


GaN Heat Maps

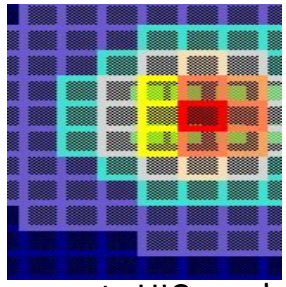


InP Heat Maps





- GaN and InP: increasing number of HICs are simulated 1-8.
- A default res (25x25 grid). 50x50 gridding also tested.
- Corner HIC regions were included for realistic completion per design rule requirements. In addition, they provide another far-field thermal path.



GaN supports HICs under the transistor: 142.8 ºC

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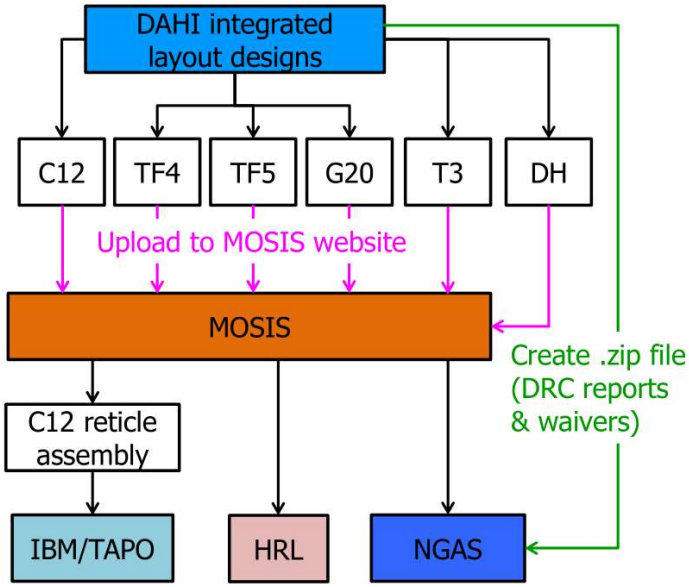
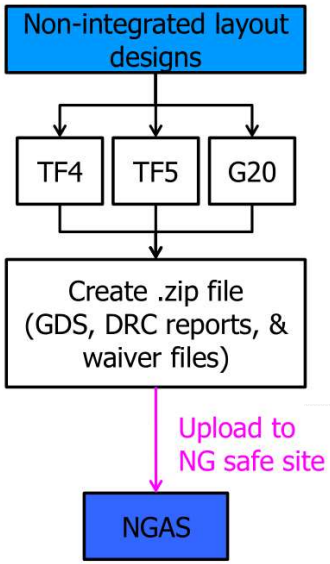
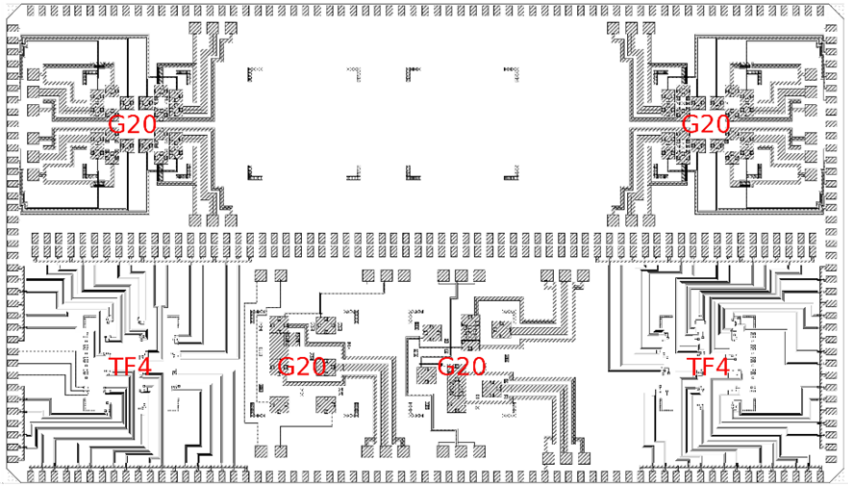
DAHI Tapeout Steps and Bonding

Design Flow

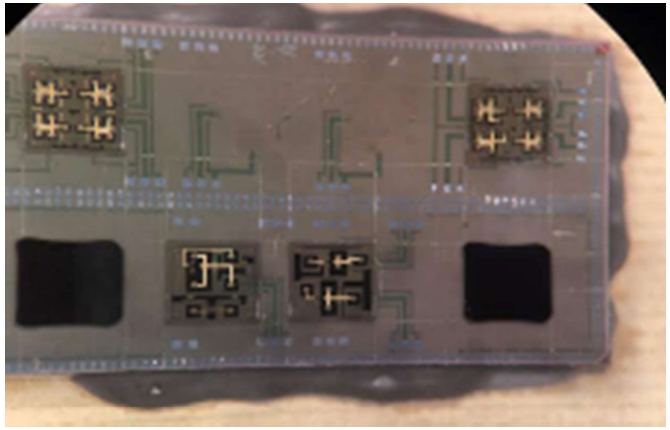




Source: NGAS

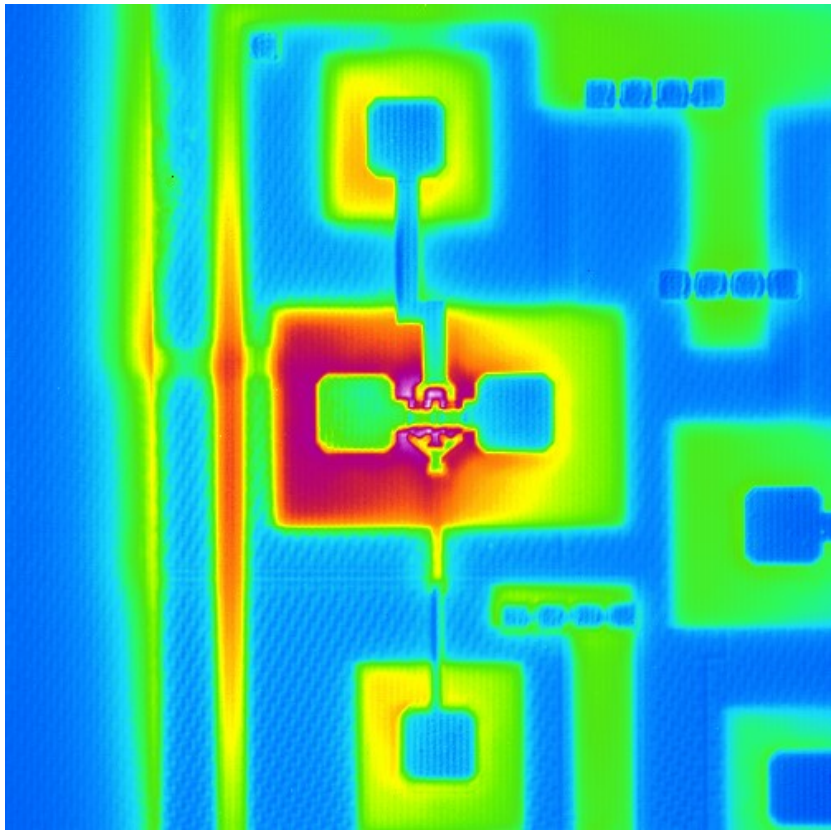


Final Layout Example

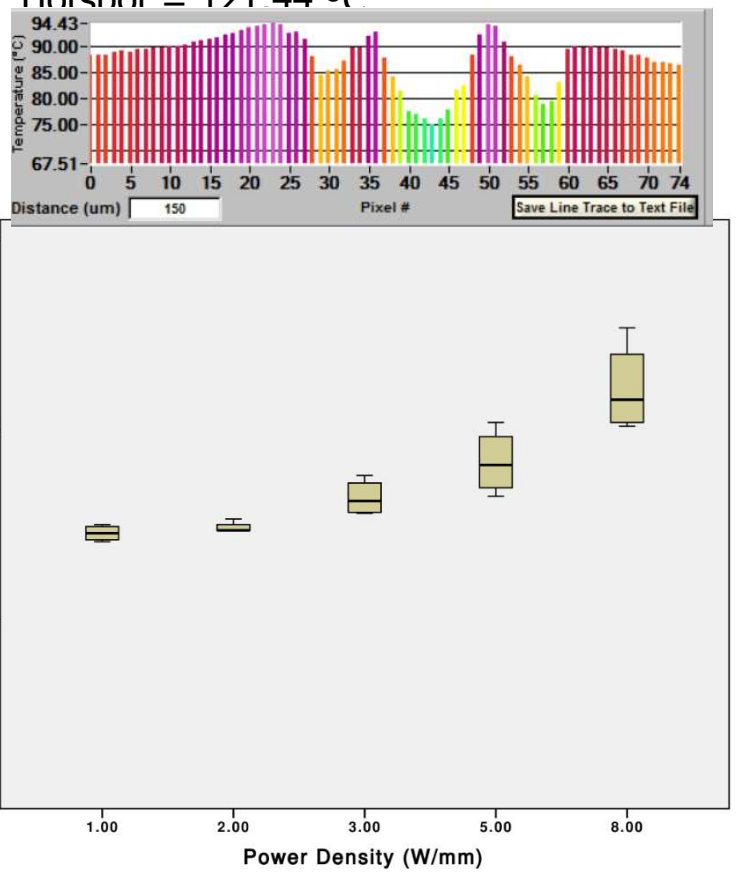


Delivery and Bonding

Thermal Measurement: GaN HEMT 10x



- Device ID: 02-Z7-1
- Vd = 10 V
- Id = 100.1 mA
- P = 1 W
- D dens = 8.34 W/mm
- Hotspot = 121.44 °C
-



Measurements: AFRL RYDD support
B. Poling, J. Peach

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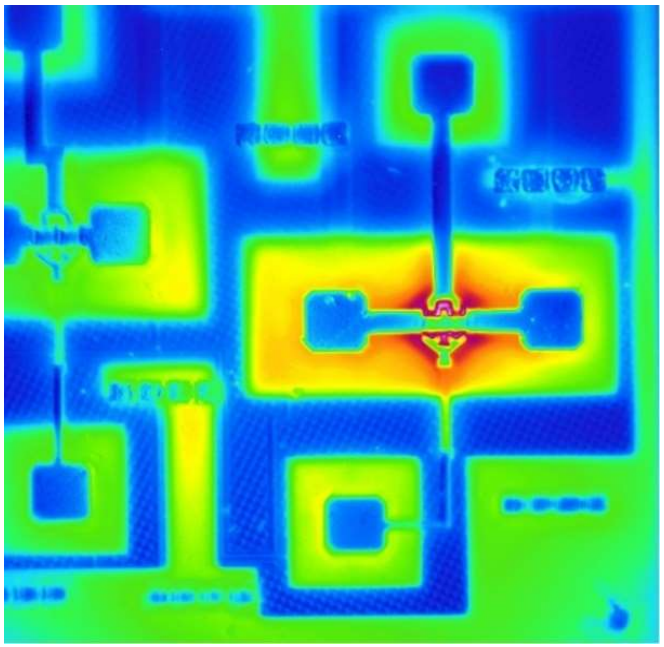
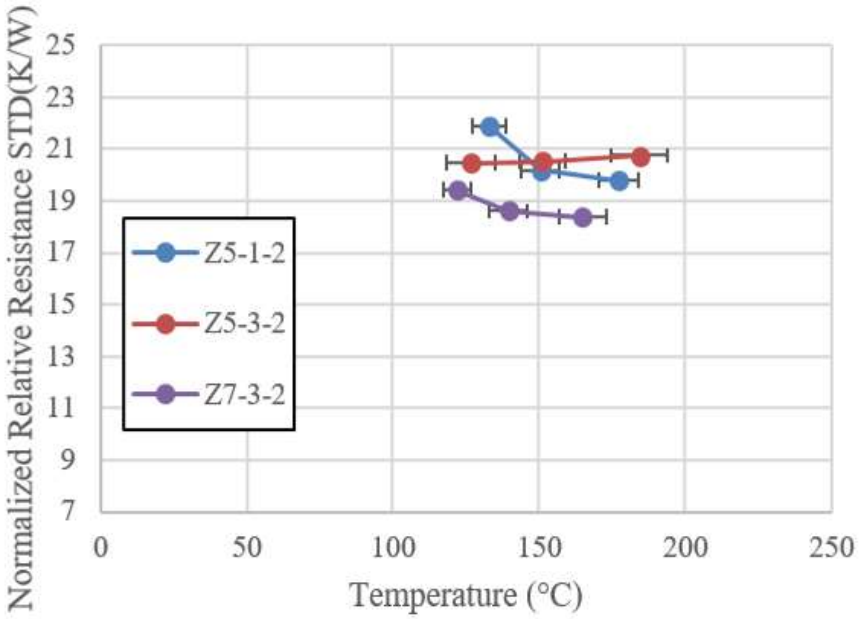
Calibration of R_{th}

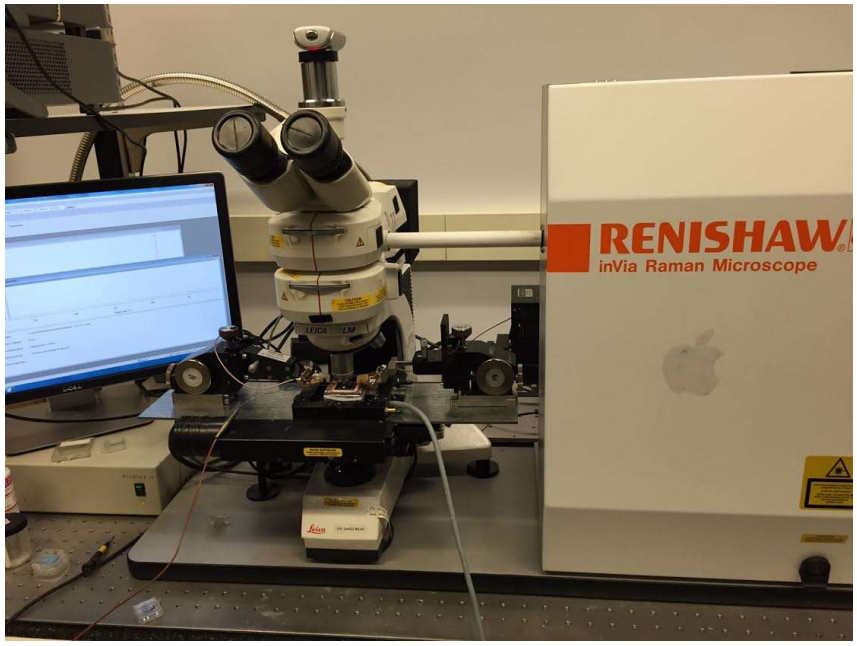


An emissivity adjusted IR heat map for a GaN HEMT assembled over CMOS is used for simulation calibration.



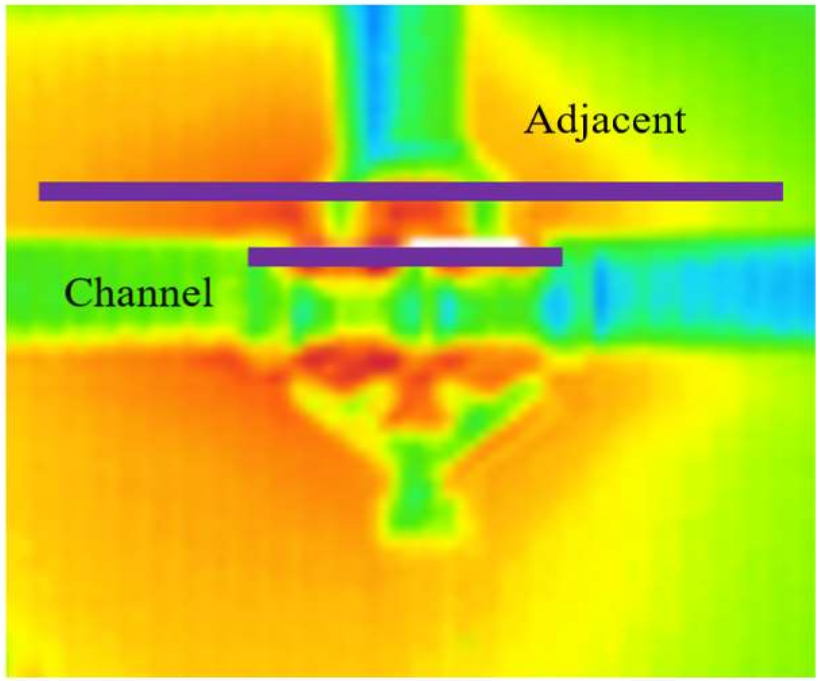
Thermal resistance vs temperature back-calculated from thermal Raman measurements in the channel. Individual samples sourced from different wafers (Z5 and Z7) are indicated.

Thermal Raman

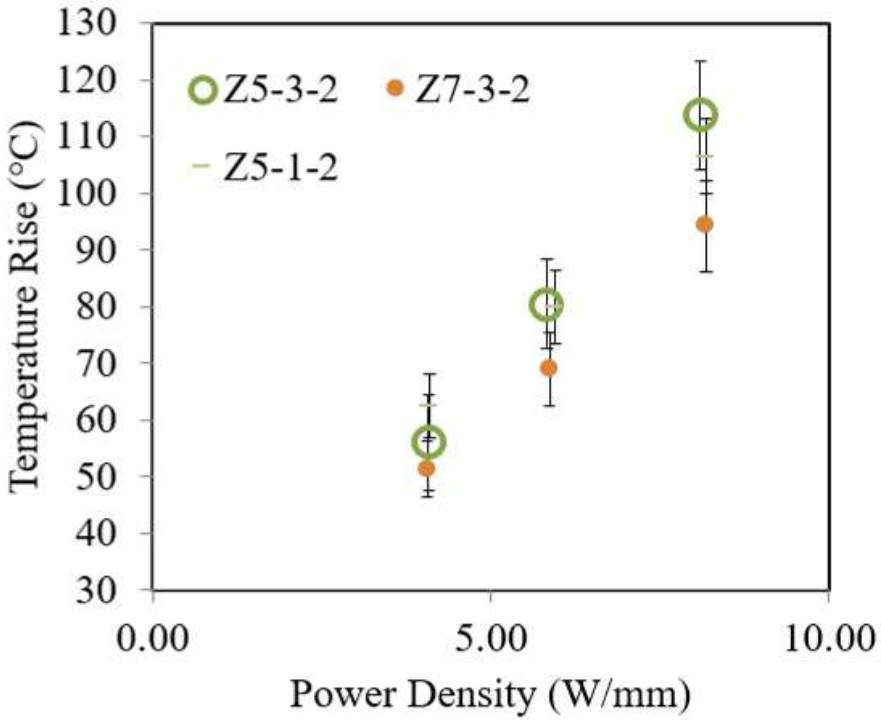


- Renishaw
- 488 nm Ar laser
- 1 μm dia. Spot
- 50X and 100X objectives used
- 95% confidence intervals
- Ave of 20 measurements made per power condition
- Calibrated with thermocouple and applied base temp.
- 32 nm anatase TiO2 Aesar® nanopowder used

GaN HEMT Measurement Sites and Results

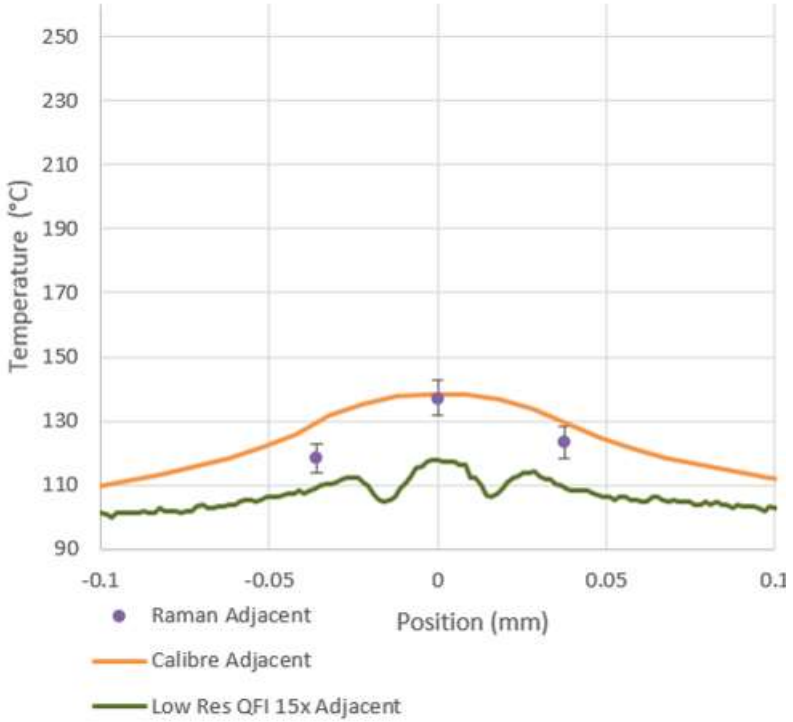


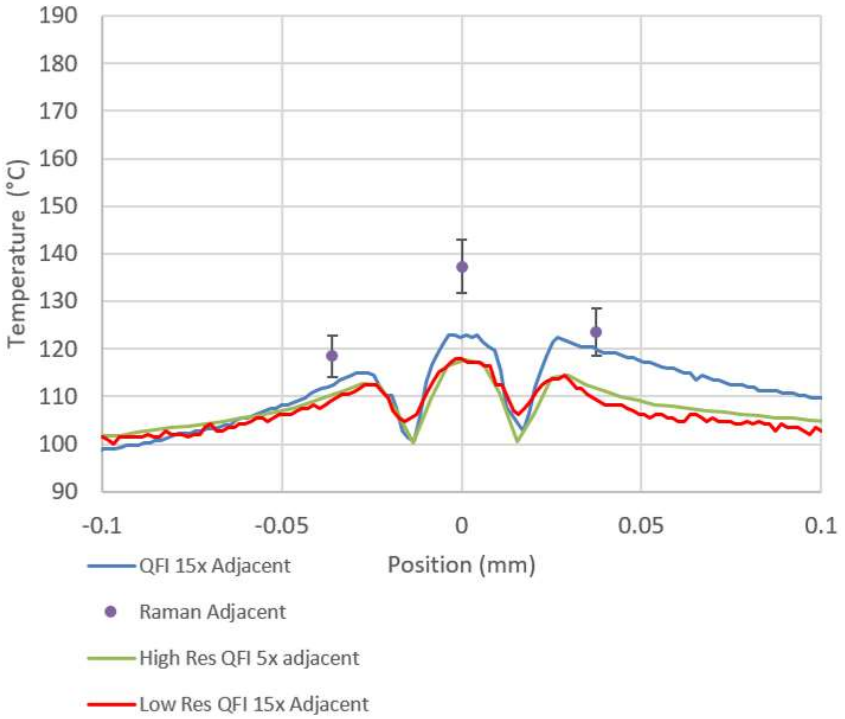
Measurement sites laterally along the HEMT channel are shown for comparison as labeled, adjacent to the channel and over the channel.



Thermal Raman results of the GaN channel through a range of different power densities.

Thermal Raman Result Comparison





Comparison of IR and Raman measurements with simulated results for device type 1 with 1 W applied and a 70 ºC base temperature.

Comparison between two different QFI IR measurement systems with differing CCD resolutions and thermal Raman measurements.

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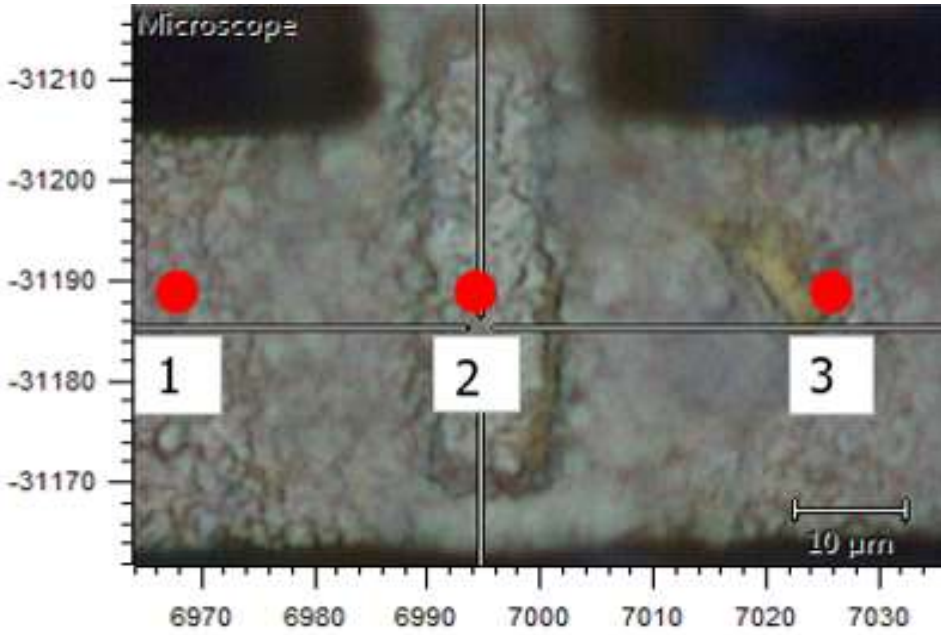
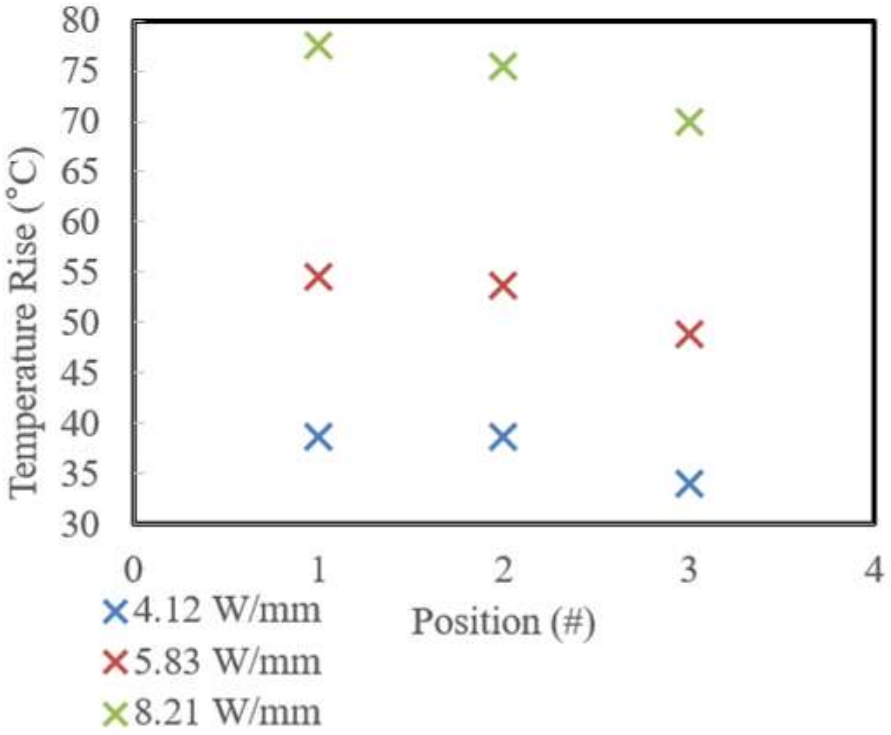
TiO_2 Air Bridge Metal Measurement



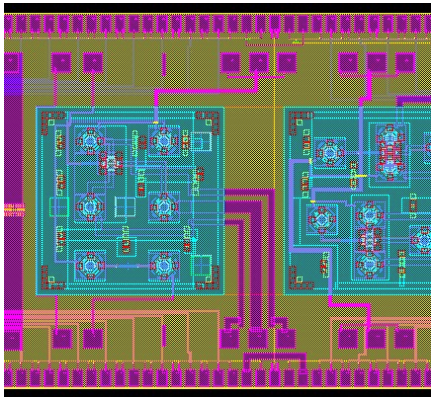
HEMT air bridge particle point measurement locations.



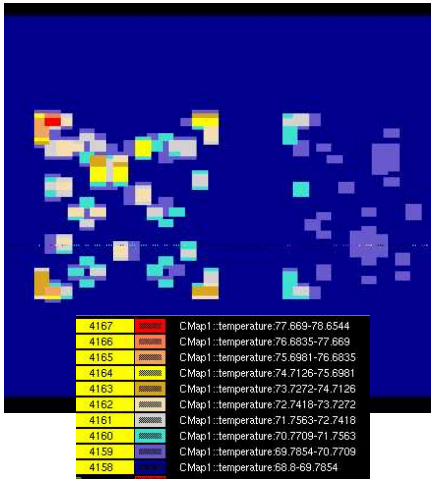
Thermal point measurements using micro-Raman of TiO_2 particles placed on HEMT gate metal which show a rise in temperature with power and asymmetric heating.

Sahara EFFP Extraction with GaN and CMOS

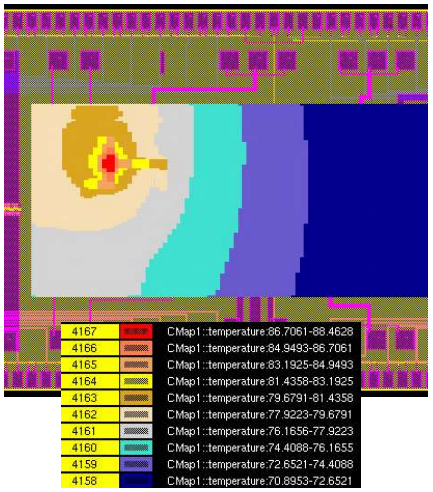
Layout



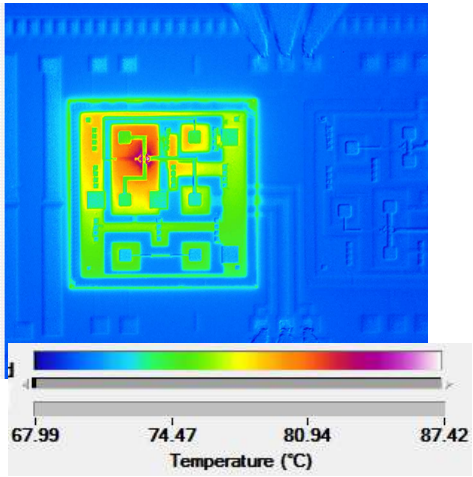
Simulated CMOS Top

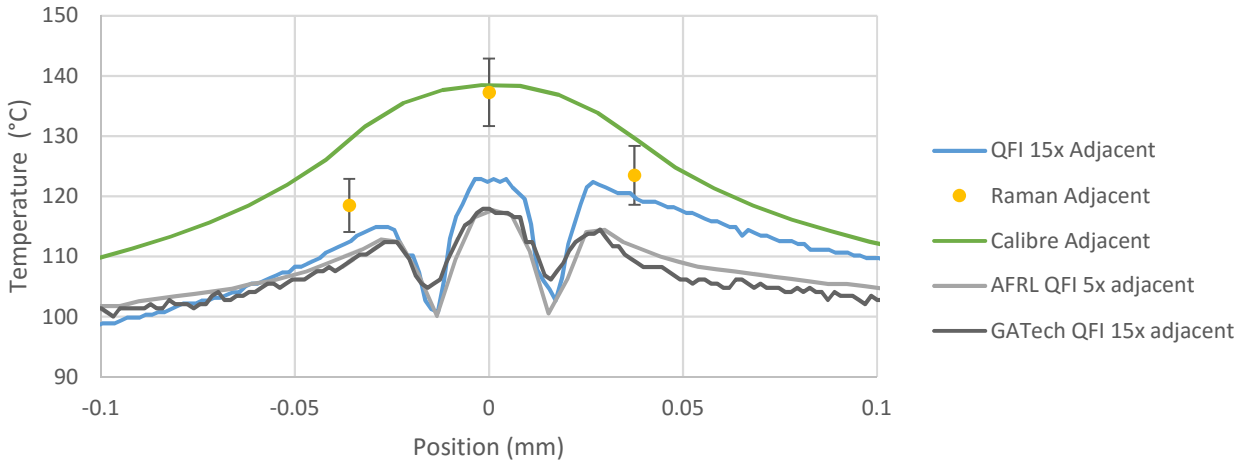


Simulated GaN Top



IR Measured





Raman Measured

Conclusions

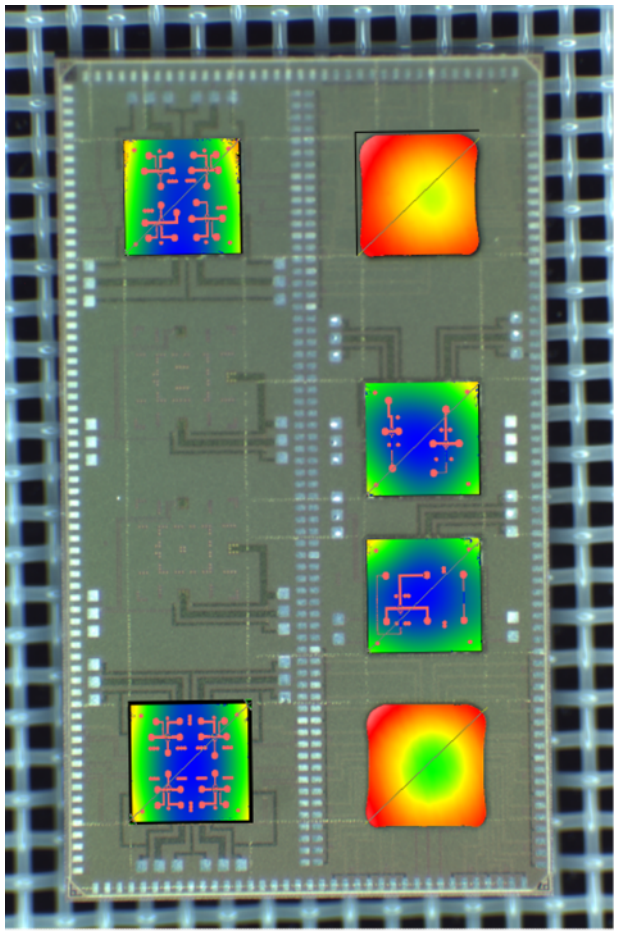
I. Thermal measurements of operating chip stacks have been presented.

II. Thermal micro-Raman using the Stokes shift method has been shown to be an effective tool for more detailed maximum gate temperatures in addition to baseline temperatures acquired by IR microscopy.

III. Thermal Raman results in and adjacent to the AlGaN channel are consistently higher, but in agreement at a distance **suggesting intense localized heating is not detectable by IR** due to area averaging or limitations due to material.

IV. Concerns of IR **transparency and metal roughness** of materials used have been mitigated by micro-Raman and furthermore a comparison of IR microscopy tools with differing CCD resolutions has been made

V. Computer simulations of HEMT gates have been shown to be largely in agreement with these measurements.



Thank You

Acknowledgments

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T. Robert Harris, Ph.D.