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Metrology Considerations for Accurate Characterization of High-Bandwidth Power Electronics Components & Applications

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MONOLITH SEMICONDUCTOR INC.

Acknowledgments - Collaborators

Collaborating U.A. Faculty

Dr. Aaron Brovont, Assistant Professor

Students (Current & Former)

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Overview

- Introduction
- Metrological Challenges for WBG Systems
  - Example 1: Voltage measurements
  - Example 2: Current measurements
  - Example 3: Packaging Impedance measurements
- Look Ahead & Conclusion

INTRODUCTION

Motivating Example

Littelfuse Power Semiconductors

SiC MOSFET

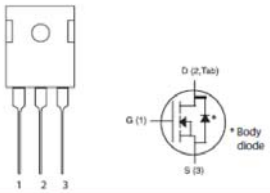
LSIC1MO120E0080, 1200 V, 80 mOhm, TO-247-3L

LSIC1MO120E0080 1200 V N-channel, Enhancement-mode SiC MOSFET HF RoHS

Product Summary

Characteristics	Value	Unit
V_{DS}	1200	V
Typical $R_{DS(ON)}$	80	mΩ
I_D ($T_C \leq 100$ °C)	25	A

Circuit Diagram TO-247-3L



Features

- Optimized for high-frequency, high-efficiency applications
- Extremely low gate charge and output capacitance
- Low gate resistance for high-frequency switching
- Normally-off operation at all temperatures
- Ultra-low on-resistance

Environmental

- Littelfuse "RoHS" logo = RoHS conform
- Littelfuse "HF" logo = HF Halogen Free
- Littelfuse "Pb-free" logo = Pb-free lead plating

Applications

- High-frequency applications
- Solar Inverters
- Switch Mode Power Supplies
- UPS
- Motor Drives
- High Voltage DC/DC Converters
- Battery Chargers
- Induction Heating

1.2 kV SiC MOSFET

Infineon

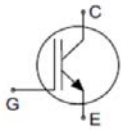
IGW15N120H3

High speed switching series third generation

High speed IGBT in Trench and Fieldstop technology

Features:

TRENCHSTOP™ technology offering
- very low turn-off energy
- low V_{CEsat}
- low EMI
- maximum junction temperature 175°C
- qualified according to JEDEC for target applications
- Pb-free lead plating, halogen-free mould compound, RoHS compliant
- complete product spectrum and PSpice Models: http://www.infineon.com/igbt/



Applications:

- uninterruptible power supplies
- welding converters
- converters with high switching frequency

Package pin definition:

- Pin 1 - gate
- Pin 2 & backside - collector
- Pin 3 - emitter

Green

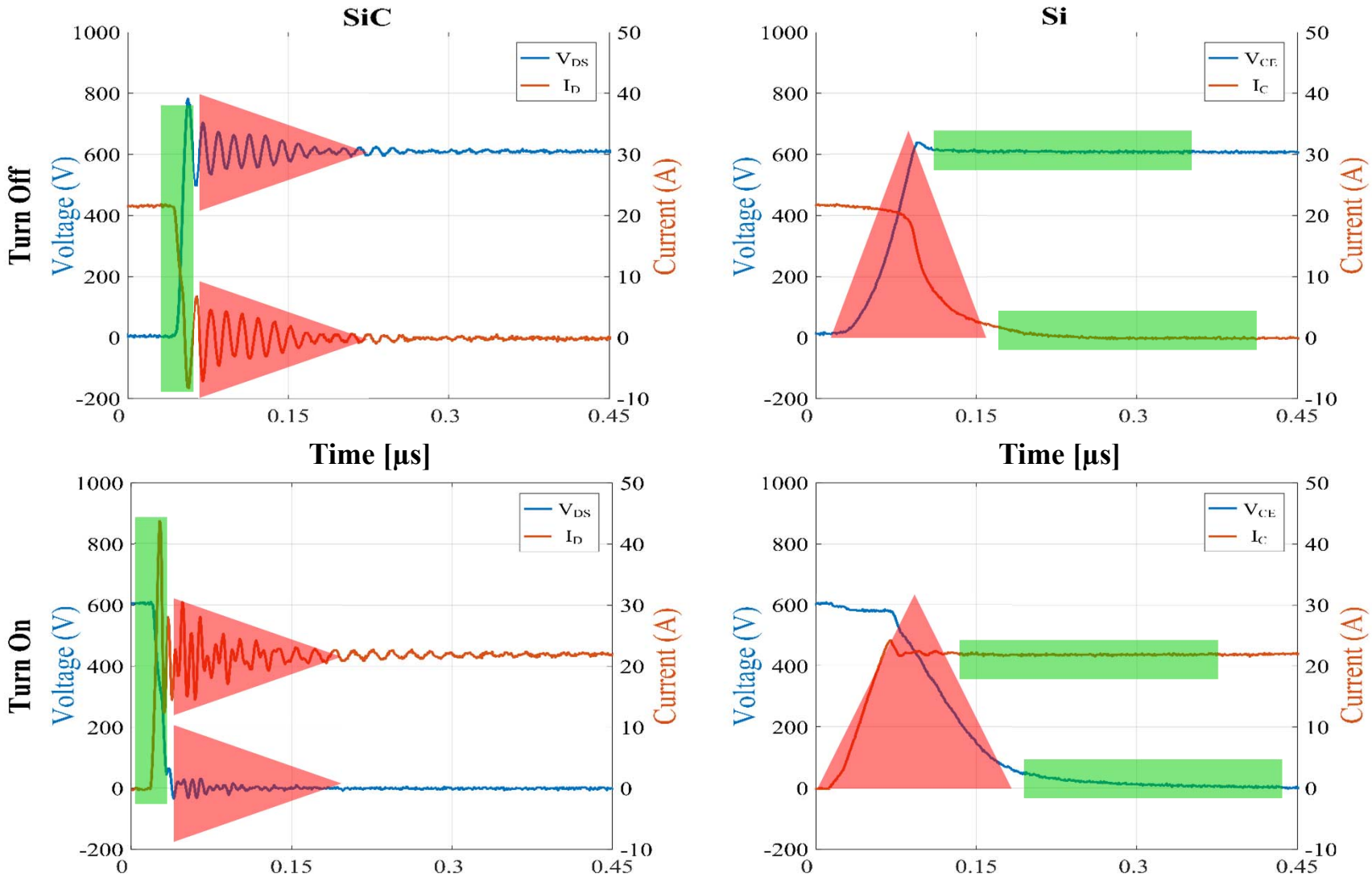
RoHS

Key Performance and Package Parameters

Type	V_{CE}	I_C	V_{CEsat}, T_{vj}=25°C	T_{vjmax}	Marking	Package
IGW15N120H3	1200V	15A	2.05V	175°C	G15H1203	PG-TO247-3

1.2 kV "High Speed" Si IGBT

SiC MOSFET vs. Si IGBT: Time Domain



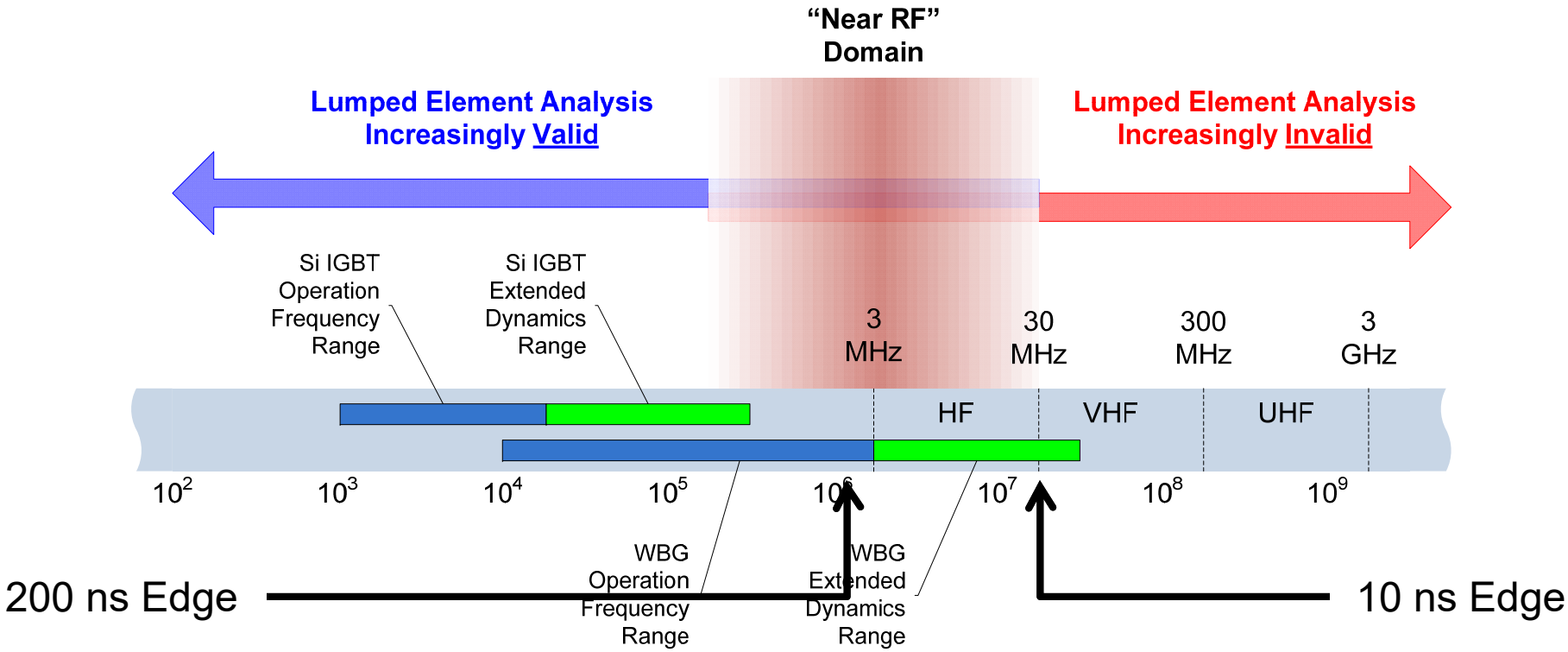
Low Switching Loss

Pronounced Ringing

High Switching Loss

Negligible Ringing

Power Electronics: Spectral Considerations



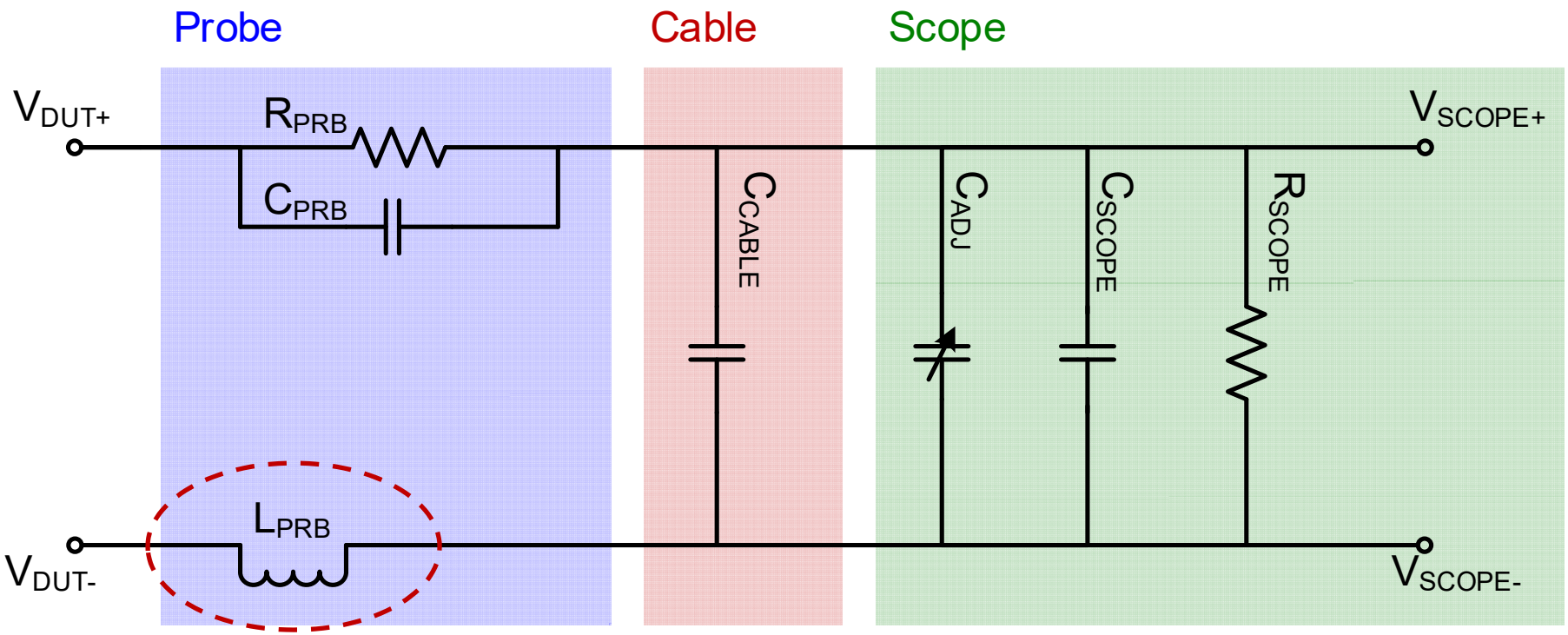
- Traditional IGBT-based systems:
  - Operation Frequencies to ~50 kHz
  - Easily-suppressed extended dynamics
  - Lumped circuit analysis works well
  - Packaging impedances are not critically important
- WBG-based systems:
  - Operation Frequencies to a few MHz
  - Extended dynamics to ~100 MHz
  - Lumped circuit analysis in question
  - Packaging impedances are critically important in "Near-RF" domain

[1] A. Lemmon, R. Cuzner, J. Gafford, R. Hosseini, A. Brovont, M. Mazzola, "Methodology for Characterization of Common-Mode Conducted Electromagnetic Emissions in Wide-Band-Gap Converters for Ungrounded Shipboard Applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 300-314, Mar. 2018.

Fast, High-Voltage Measurements

EXAMPLE 1

Case Study: "Standard" Passive 300V 10x Probe



- For DC, attenuation accomplished by R_{SCOPE} & R_{PRB}
- For AC, attenuation accomplished by (C_{PRB}) & (C_{ADJ}+C_{CABLE}+C_{SCOPE})
- Works (mostly) great, except for L_{PRB}!

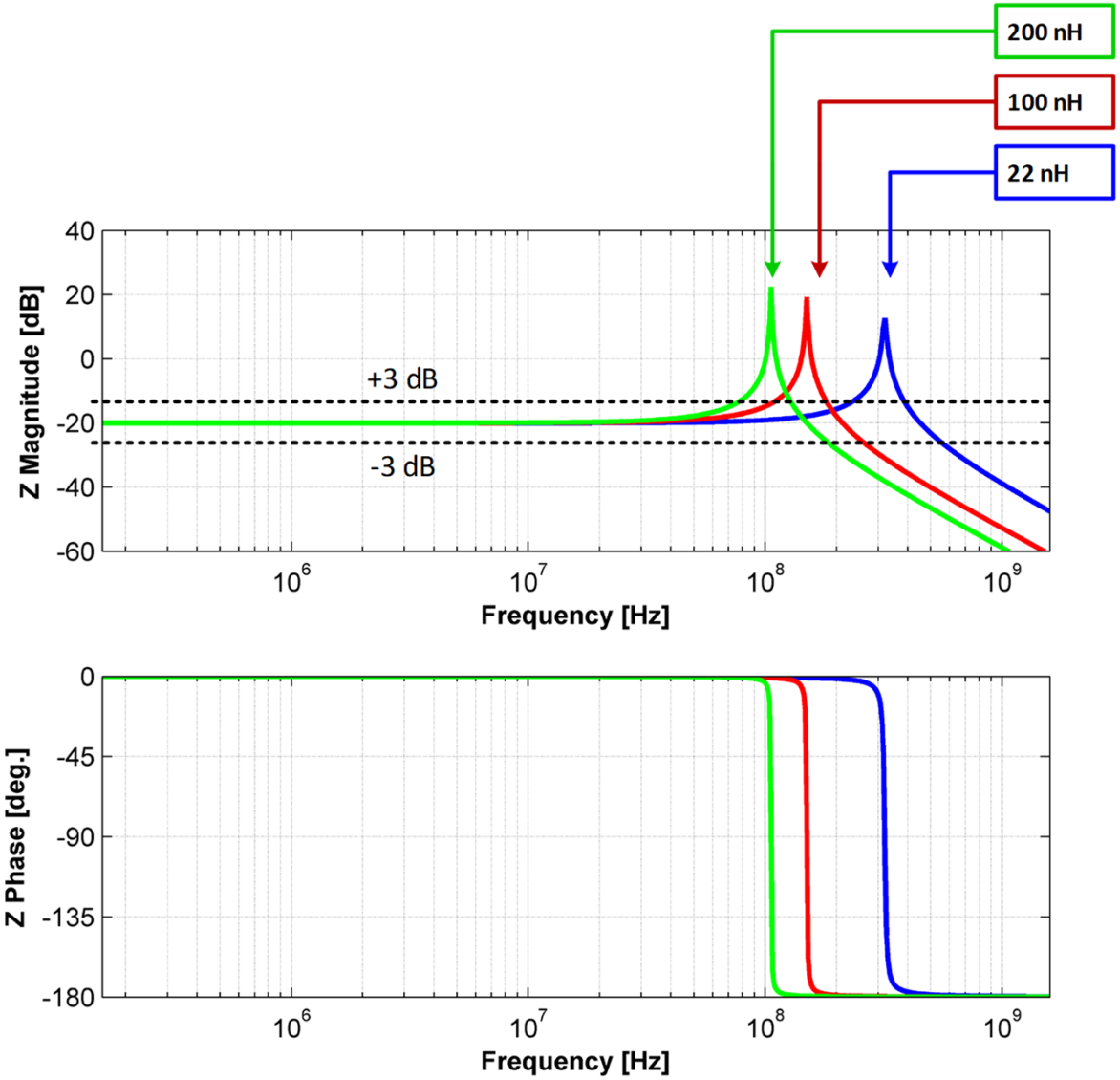
Example Probe for Test Case

- Case study based loosely on Tektronix Setup at UA:
  - Tek P5050B Probe
    - » R_{PRB}: 9 MΩ
    - » C_{PRB}: 12 pF (8 pF)
    - » C_{CABLE}: 100 pF (~3 meters)
  - Tek 4000B Oscope
    - » R_{SCOPE}: 1 MΩ
    - » C_{PRB}: 13 pF
    - » C_{ADJ}: 0-1 pF
  - L_{PRB} Varied 22 nH – 200 nH
  - Ground lead inductance is approximately 20 nH per inch [4]

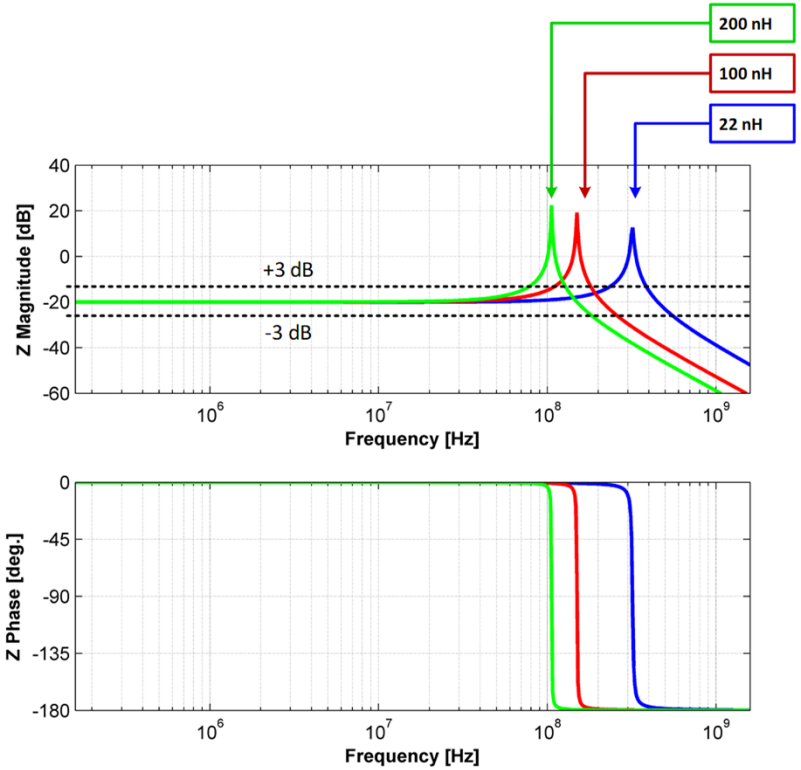
Tektronix P5050B Passive Probe (10:1)

[4] "TekConnect Probes: Signal Fidelity Issues and Modeling," Tektronix Inc., Beaverton, OR, 2004.

Effect of Ground Lead Inductance



Problem #1: Bandwidth

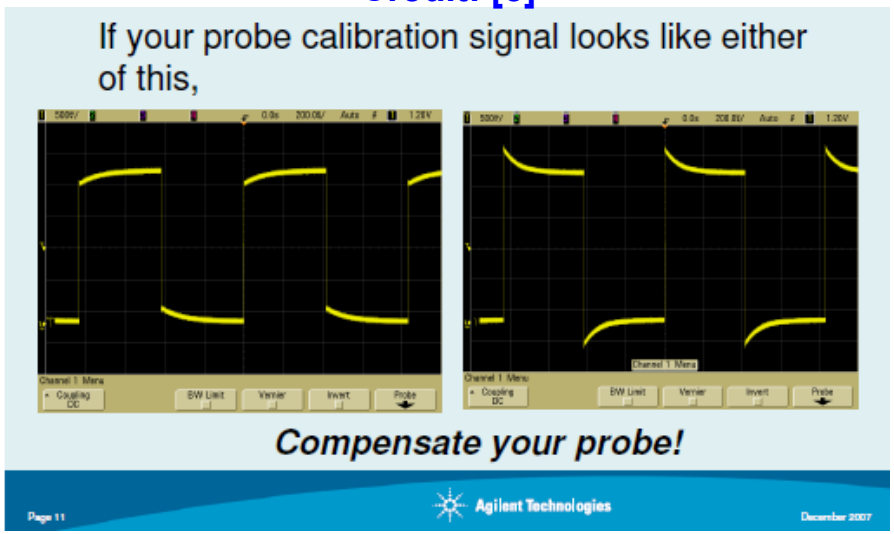


L_GND	22 nH	100 nH	200 nH
Resonant Freq.	320 MHz	150 MHz	106 MHz
Bandwidth -3 dB	500 MHz	233 MHz	165 MHz
Bandwidth +3 dB	172 MHz	80.3 MHz	56.8 MHz

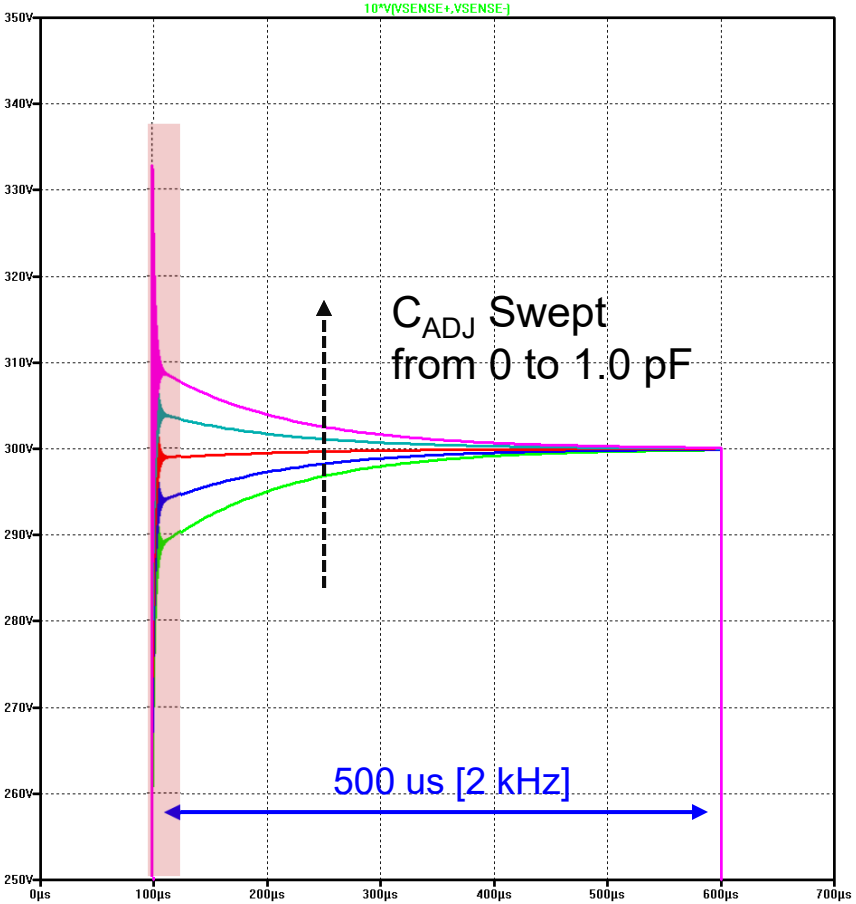
Problem #2: Probe Compensation Sensitivity

- Need for passive probe compensation is well-known
- Ensures the accuracy of transient response esp. with fast edge rates
- Common procedures
  - Manual comp. with built-in 1 kHz
  - Auto-compensation with ASIC-enabled probes

Credit: [5]



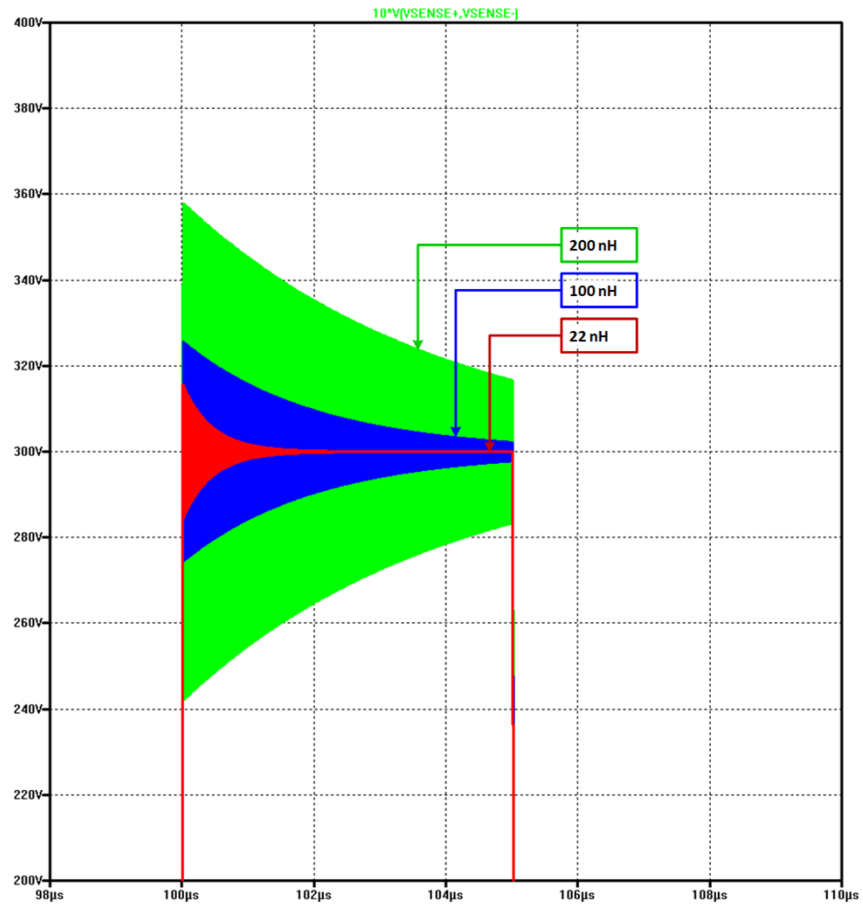
Probe Compensation Example (Simulation)



[5] J. Chang, "6 hints for better scope probing," Agilent Technologies, Inc., Santa Clara, CA, Dec. 2007.

Problem #3: Resonances

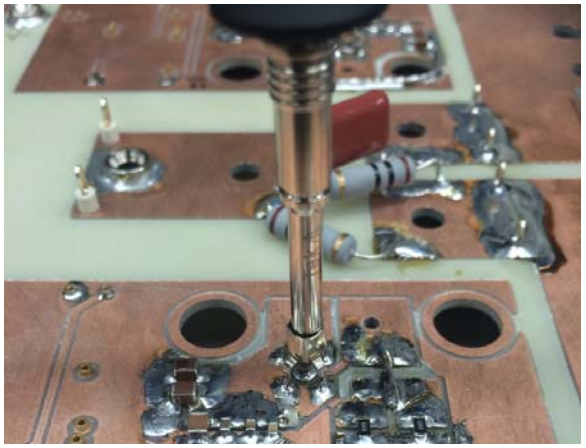
- Fast edge rates of 20-80 V/ns excite resonances in:
  - Application parasitics
  - Oscope input impedance
- Example at right shows a “slow” WBG voltage transition (20 V/ns) with <u>no application parasitics</u>
- All visible resonance is the result of probe resonance, using 10x model
- Values of GND lead inductance considered:
  - 22 nH
  - 100 nH
  - 200 nH



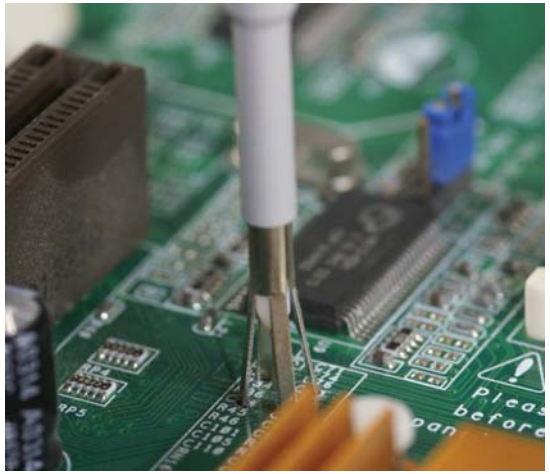
Mitigation of Ground Lead Inductance Effects

- Mitigation methods currently available:
  - Probe-tip adapters are available (Tek, Keysight, CalTest)
  - Tinned copper can make a reasonable substitute
- However, these methods have limits for WBG power electronics
  - Restricted to Ground-referenced probes
  - Not designed for measurements above ~200V
  - Things get very difficult at MVDC levels

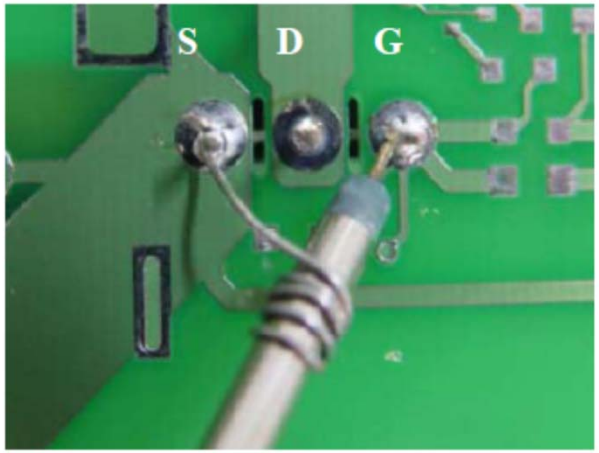
Tek Probe Tip Adapter



Keysight N2885A

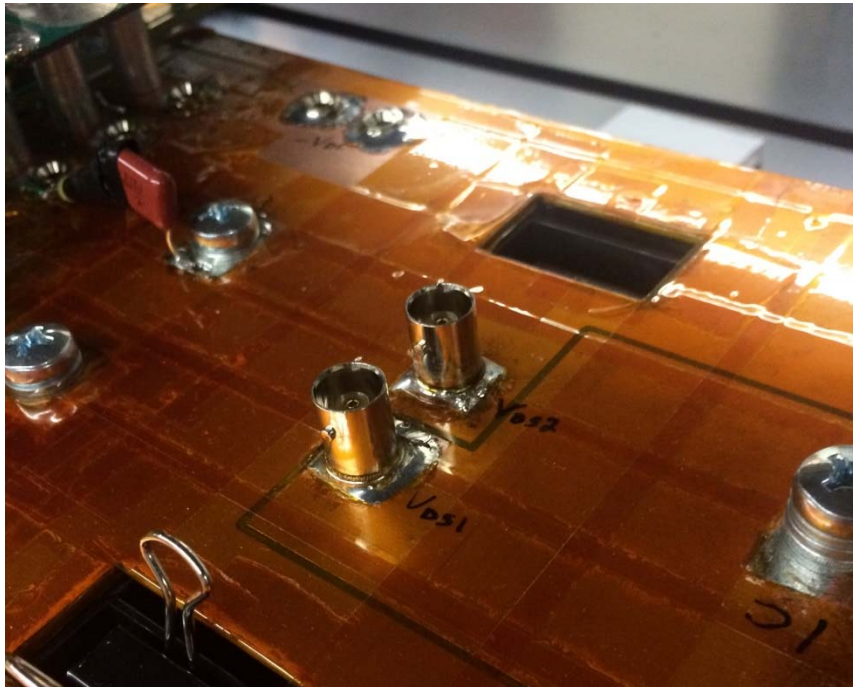


"Paper-clip Trick"



Tektronix BNC Probe-Tip Adapter

- Tek BNC Probe tip adapter effectively suppresses (most) ground-lead effects
- Problem: BNC Connectors are only rated for 500 V

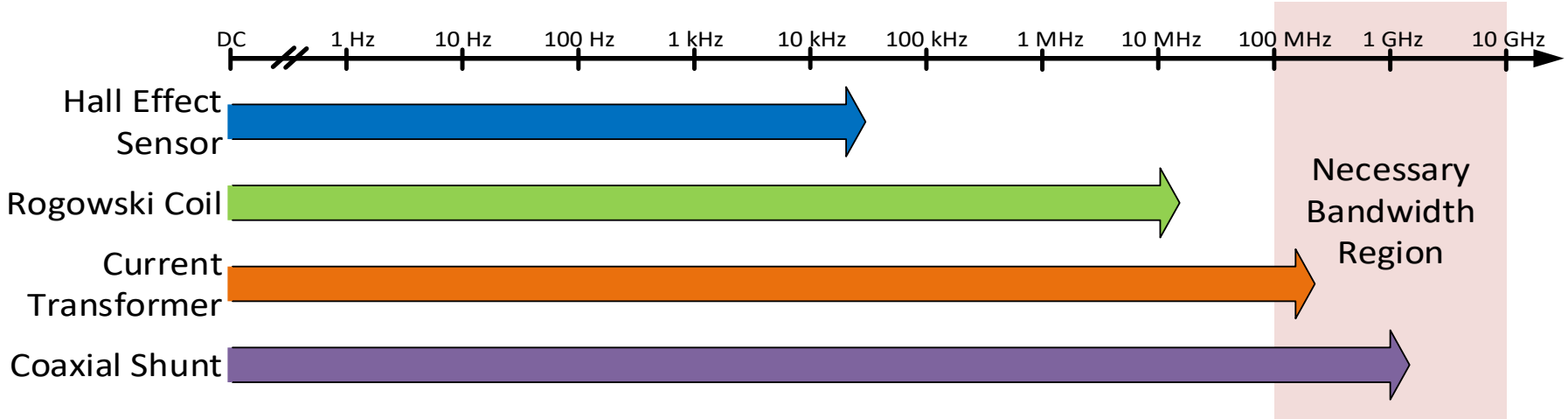


High-Bandwidth Current Measurement

EXAMPLE 2

Current Measurement Requirements - Bandwidth

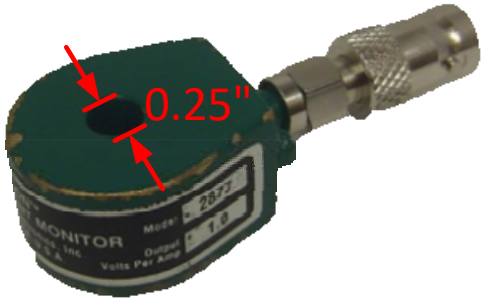
- Ringing in WBG device currents can reach 50-100 MHz
- Bandwidth requirements specified in the literature as [6]:
  - 5x bandwidth over the frequency of interest for magnitude fidelity
  - 10x bandwidth over the frequency of interest for phase fidelity
- The high bandwidth requirement eliminates techniques such as hall effect sensors and Rogowski coils



[6] J. Witcher, "Methodology for switching characterization of power devices and modules," M.S. Thesis, Virginia Polytechnic Institute, Blacksburg, VA, USA, 2003.

Current Measuring Difficulties - Inductance

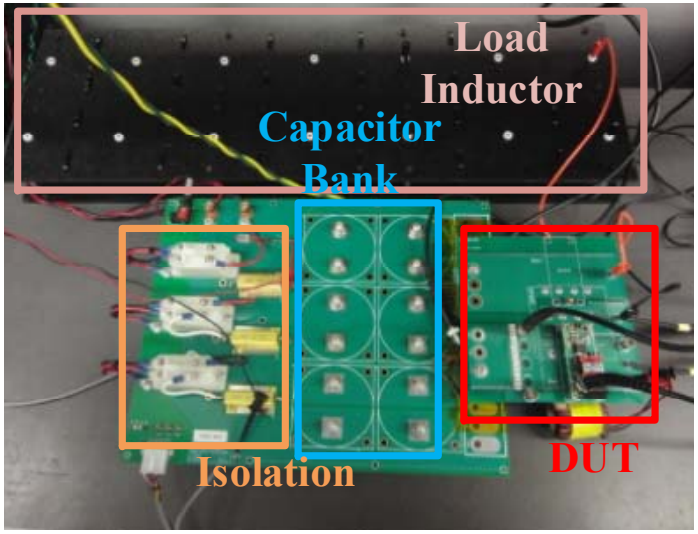
- Methods with adequate bandwidth introduce a “choke-point” into the system
- The DC bus must be routed through a small sensor aperture
- The “choke-point” causes an attendant increase in the bus inductance
- The additional parasitic inductance exacerbates undesirable ringing

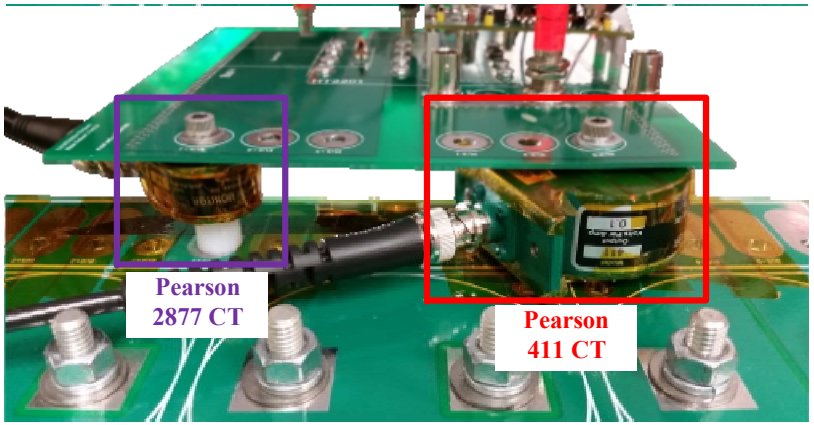


[7] C. New, A. Lemmon, and A. Shahabi, "Comparison of Methods for Current Measurement in WBG Systems," in *Proc. Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp 87-92..

Double-Pulse Testing – Method Comparison

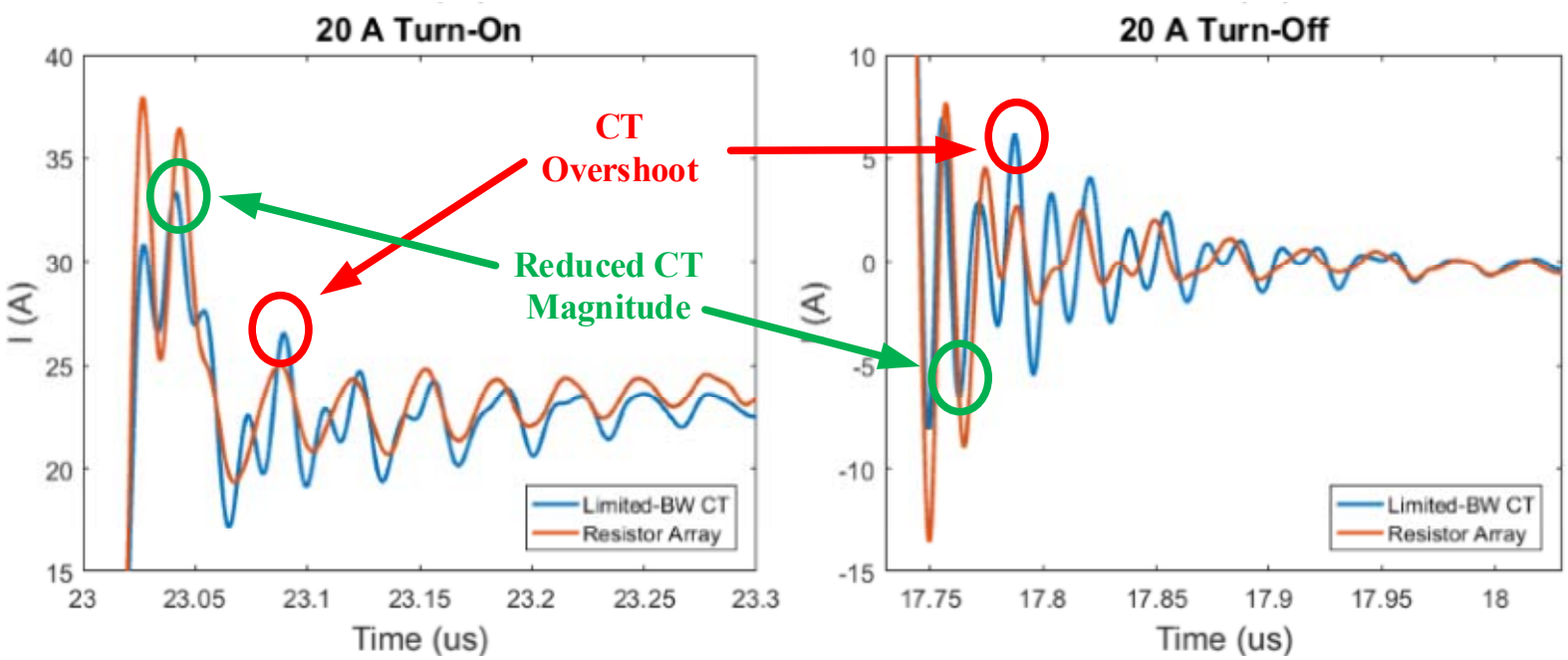
- DPT evaluations at 600 V & a range of currents were performed with this setup
- The bus was designed to allow multiple simultaneous current measurements - two CTs and one of the three custom PCBs
- The multiple measurements enabled comparisons under identical test conditions
- Before each measurement, the probes were de-skewed to ensure consistent V–I alignment





DPT Results – Coaxial Shunt vs. "Slow" CT

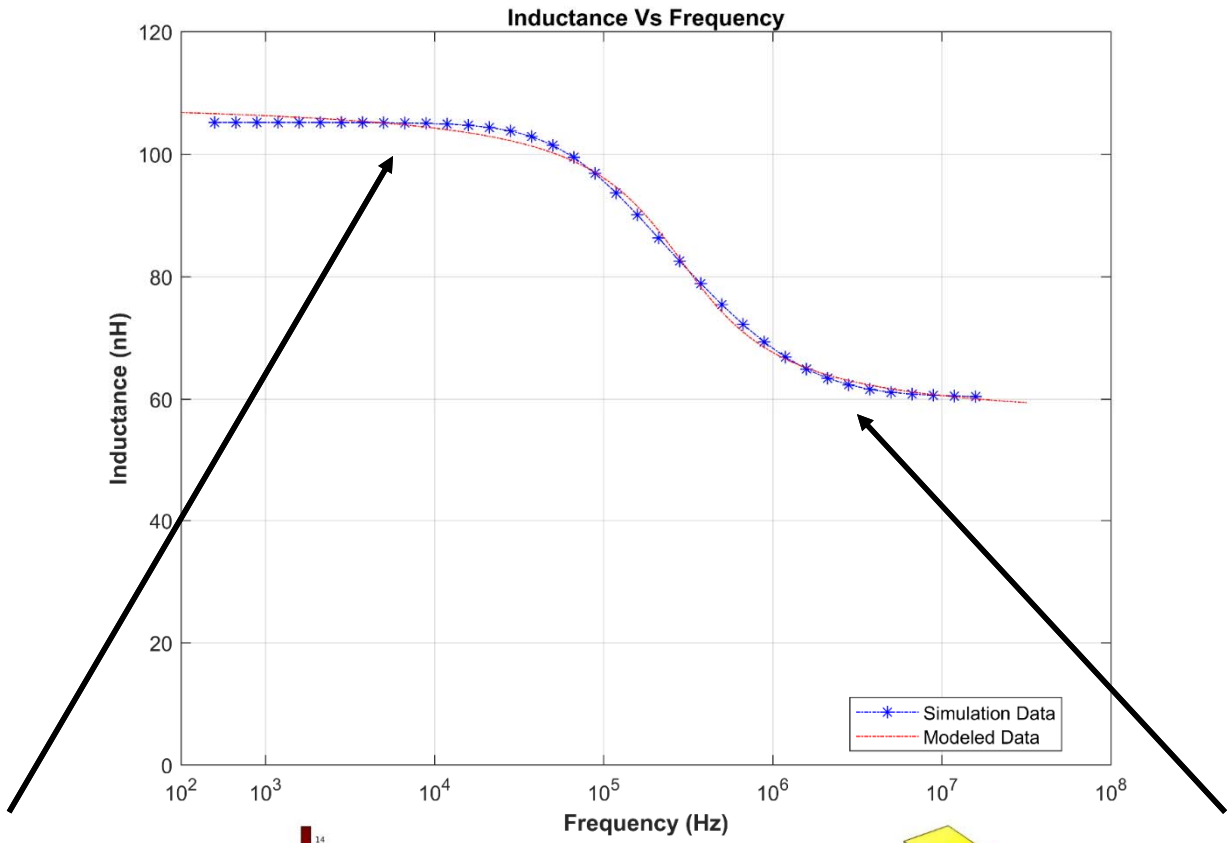
- With the discrete SiC MOSFET, the 20 MHz CT does not accurately track the device current
  - Significant magnitude errors
  - Excessive overshoot during ringing
  - Phase mismatches
- Conclusion: CT is not sufficient for discrete SiC MOSFET characterization, but may be used (cautiously) for power module characterization

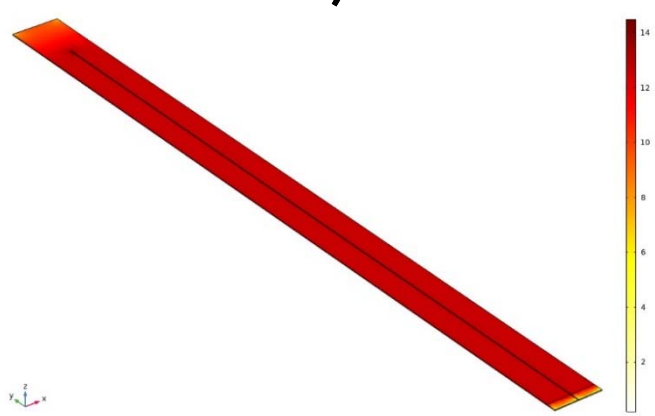


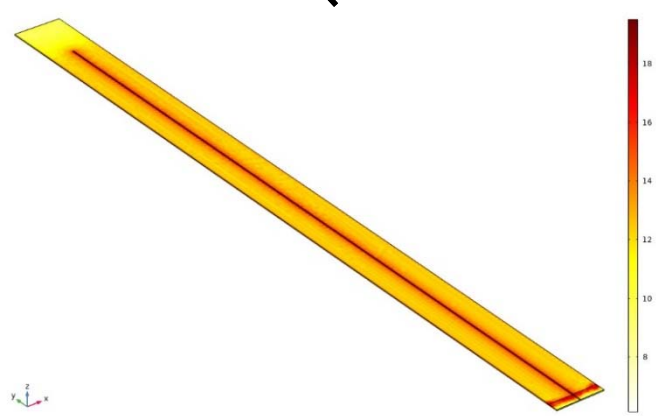
Packaging Impedance Measurement

EXAMPLE 3

Frequency Dependence of Parasitic Inductance

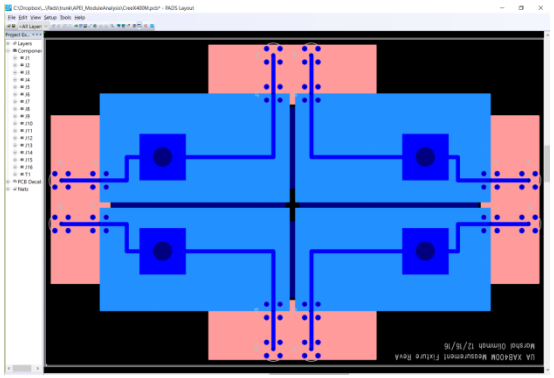






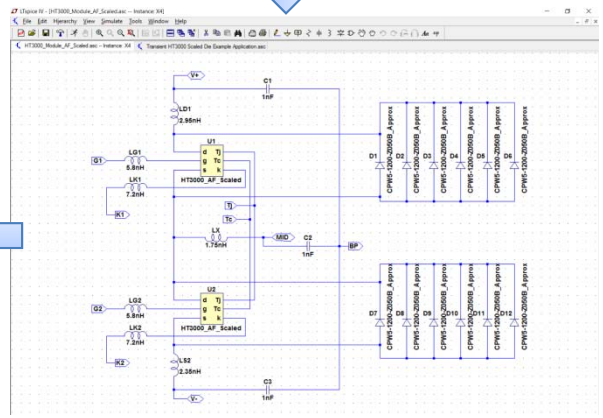
Measurement-Based Parasitic Modeling Procedure – Developed at UA

Module Adapter PCB Design

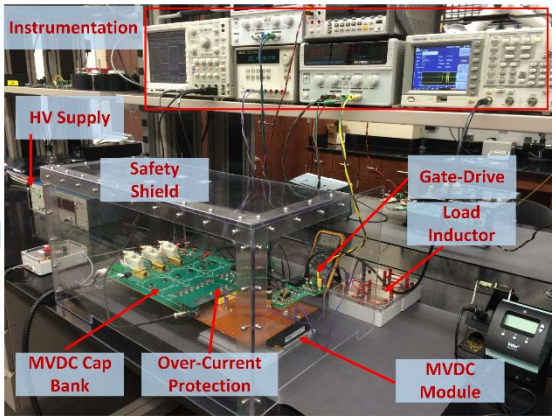


Module Adapter Fabrication

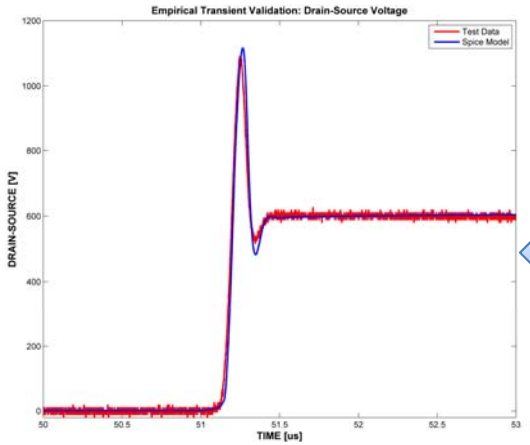
Frequency-Domain Parasitic Measurements



LTspice modeling



Double-Pulse Testing



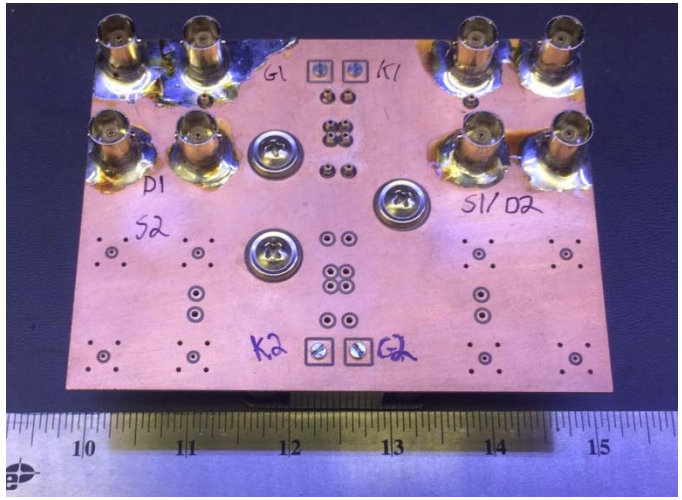
Transient Comparison / Validation

[9] A. Lemmon, T. Freeborn, A. Shahabi, “Fixturing impacts on high frequency low-resistance, low-inductance impedance measurements,” *IET Electronics Letters, vol. 52, no. 21, Oct. 2016*.
[10] A. Lemmon, R. Graves, "Characterization and Modeling of 10 kV Silicon Carbide Modules for Naval Applications," accepted to *IEEE Journal of Emerging and Special Topics in Power Electronics*.
[11] A. Lemmon, R. Graves, "Comprehensive Characterization of 10 kV Silicon Carbide Half-Bridge Modules," *IEEE Journal of Emerging and Special Topics in Power Electronics*, vol. PP, no. 99, Sep. 2016.
[12] A. Lemmon, R. Graves, “Gate Drive Development and Empirical Analysis of 10 kV SiC MOSFET Modules,” in *Proc. Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov. 2015.
[13] A. Lemmon, R. Graves, “Parasitic Extraction Procedure for Silicon Carbide Power Modules,” in *Proc. International Workshop on Integrated Power Packaging*, 2015, pp. 91-94.
[14] M. Mazzola, M. Rahmani, J. Gafford, A. Lemmon, R. Graves, “Behavioral Modeling for Stability in Multi-Chip Power Modules,” in *Proc. International Workshop on Integrated Power Packaging*, 2015, pp. 87-90.
[15] A. Lemmon, R. Graves, and J. Gafford, “Evaluation of 1.2 kV, 100A SiC Modules for High-Frequency, High-Temperature Applications,” in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 789-793.

Example SiC Module Parasitic Measurement Fixture

- Module fixture performs two functions:
  - Adapts module terminals to VNA connectors
  - Provides a mechanism to extend calibration plane to module surface
- Measured loop inductance includes module geometry, with interface adapter
- Compensation process (ideally) removes the influence of the fixture

Impedance Measurement Adapter - TOP



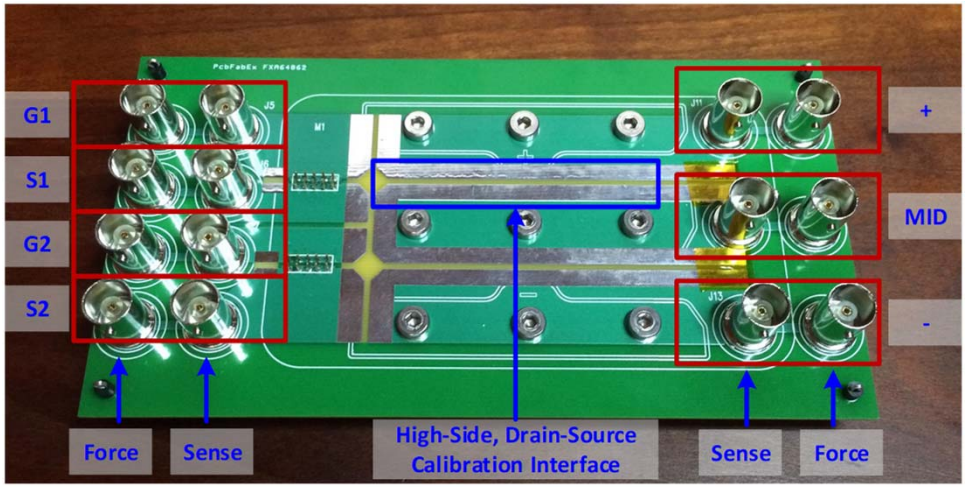
Impedance Measurement Adapter - SIDE

1.2 kV, 120A SiC MOSFET Module Test Subject

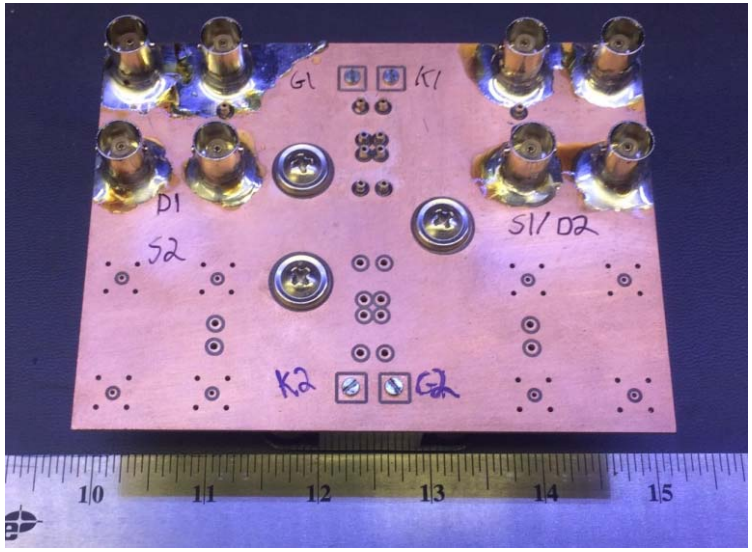
[16] A. Lemmon, R. Graves, "Parasitic Extraction Procedure for Silicon Carbide Power Modules," in *Proc. International Workshop on Integrated Power Packaging (IWIPP)*, Chicago, IL, 2015, pp. 91-94.

Power Module Fixture PCB Generations

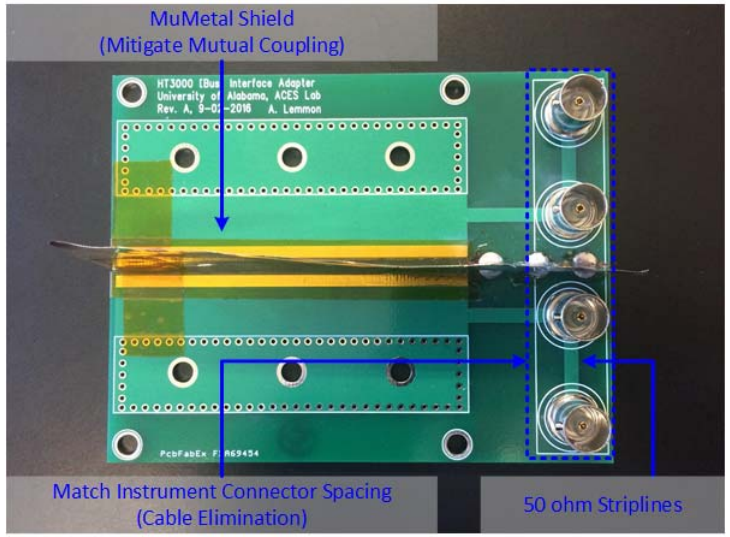
Second Generation



First Generation

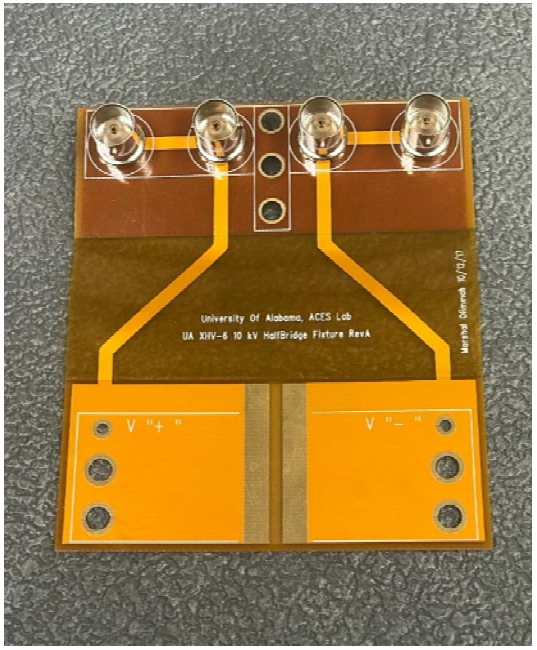


Third Generation



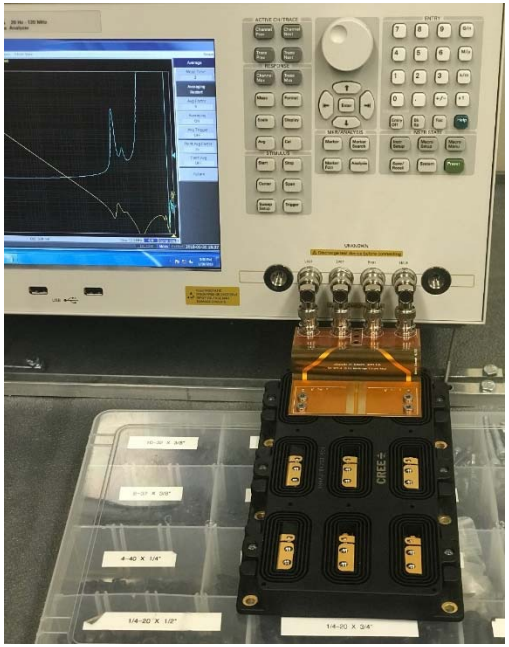
Fourth-Generation Measurement Fixture with Flex PCB

Fourth Generation Fixture



Fixture Attached to XHV-6

XHV-6 Parasitic Extraction



Article Published in IEEE TIM Based on These Findings

- UA has performed parasitic modeling for >25 modules over the last 3 years
- The fixture design process has been substantially improved during this time
- Key findings have been detailed in an article published in *IEEE Transactions on Instrumentation and Measurement*
  - All fixtures introduce some error into measurements
  - Error increases when the fixture impedance is on the same order as the DUT impedance
- Very low parasitic modules are extremely difficult to characterize properly
- What if we could get away without using a fixture?

Modeling and Validation of Fixture Induced Error for Impedance Measurements

Blake W. Nelson, *Student Member, IEEE*, Andrew N. Lemmon, *Member, IEEE*, Brian T. DeBoi, *Student Member, IEEE*, and Todd J. Freeborn, *Member, IEEE*

***Abstract*—Measuring impedance accurately requires dedicated fixturing to match the geometry of the device under test to the ports of the instrument. These fixtures introduce error into collected measurements which is rarely acknowledged. Failure to quantify measurement error can lead to over-estimation of accuracy, increase the difficulty of measurement comparisons taken with different fixtures, and increase the risk of inappropriate fixture selection and calibration. This paper presents a methodology for characterizing and modeling the error introduced into impedance data by test fixtures. The proposed method uses direct measurements of the open and short calibration standards as well as a precision resistor to quantify the total error introduced by the fixture. The error of a commercially available test fixture is studied and compared against its published values to validate this method. This validated approach can model the error introduced by commercial or custom fixtures.**

***Index Terms*—error analysis, fixturing, impedance analysis, metrology**

I. Introduction

MEASURING impedance allows the electrical characteristics of devices to be modeled quickly and succinctly. Improvements in semiconductor technologies have made accurate measurements of low impedance devices and packages a necessity. In the field of power electronics, wide bandgap (WBG) semiconductors have increased achievable switching speeds, but these systems must contend with high frequency spectral content introduced as a consequence of this behavior [1]-[5]. Such systems implement ultra-low-parasitic capacitors which require precision measurements for impedance characterization [5]. Additionally, applications with high-edge-rate-capable WBG semiconductors require filter inductors and other magnetics designed with appropriate high-frequency magnetic materials and high self-resonant frequencies (SRF), which require accurate high frequency impedance characterization [6]. Another field requiring precision impedance analysis is the design of power distribution networks (PDN's) for digital systems. Increasing gate density and clock speed of ASIC's and FPGA's has led to complex power requirements to guarantee integrity during current transients, requiring close attention to impedance both on chip and off chip [7]-[9].

Such tasks demand custom fixtures to measure unique geometries with satisfactory accuracy [10], [11]. For example, multichip power modules (MCPM) used in power electronics can have packaging impedances below 10 nH [12]. Because these devices are designed without RF coaxial terminals, custom fixtures are required to connect them to test equipment with a coaxial interface [10]. To determine the quality and understand the limitations of impedance measurements in these and other applications, it is important to quantify the error introduced by these fixtures [13]. Understanding the degree to which these impedances are known is necessary to evaluate the accuracy of models built on them.

While instrumentation vendors such as Keysight Technologies, Inc. publish error terms for specific instruments [14] and fixtures [15], there is little information available to support designers' need to quantify the error introduced by custom fixtures [16]. This increases the difficulty of improving the accuracy of measurements made with custom fixtures and reduces the validity of comparing measurements collected with different fixtures. The need for error estimates mandates a generalized methodology capable of characterizing the error introduced by fixtures.

This work reinforces several practical guidelines from the literature on fixturing [16] and presents an empirical methodology for practitioners to quantify the systematic error introduced by any fixture (not the generalized uncertainty intrinsic to impedance measurements as discussed by GUM [23]). The error-model of a commercially available fixture was determined using this methodology and compared to the manufacturer provided error to validate this procedure.

This work is organized as follows: Section II introduces the theory underlying electrical impedance measurements and the impacts of fixturing on measurement error; Section III investigates the published error of an example commercial impedance analyzer (ZA) and fixture; Section IV provides and validates the empirical method for predicting these error models, and Section V concludes the paper.

II. Auto-Balancing Bridge Theory

Precision impedance measurement is a mature field, with rudimentary impedance analysis tools called "decade bridges" commercially available as early as 1918 and auto-balancing bridges available in the 1960's [17]. One example of a modern precision impedance measurement instrument is Keysight Technologies' E4990A [14], which can measure impedance from 20 Hz to 120 MHz. In addition to the published accuracy ratings of this device, the manufacturer also details methods of calculating error based on the available device settings and configurations (including measurement time, frequency range, excitation stimulus, etc.).

The core functional component of the E4990A is an auto-

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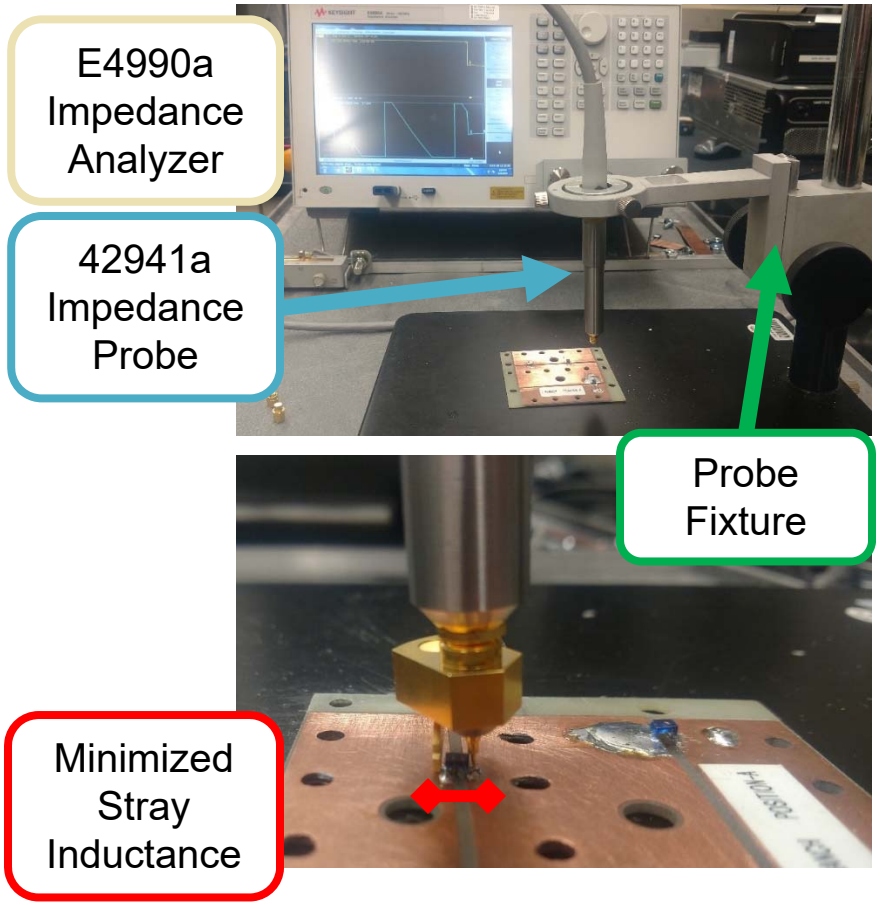
[17] B. Nelson, A. Lemmon, B. Deboi, T. Freeborn, "Modeling and Validation of Fixture Induced Error for Impedance Measurements," IEEE Transactions on Instrumentation & Measurement, vol. 68, no. 1, pp. 129-137, Jan. 2019.

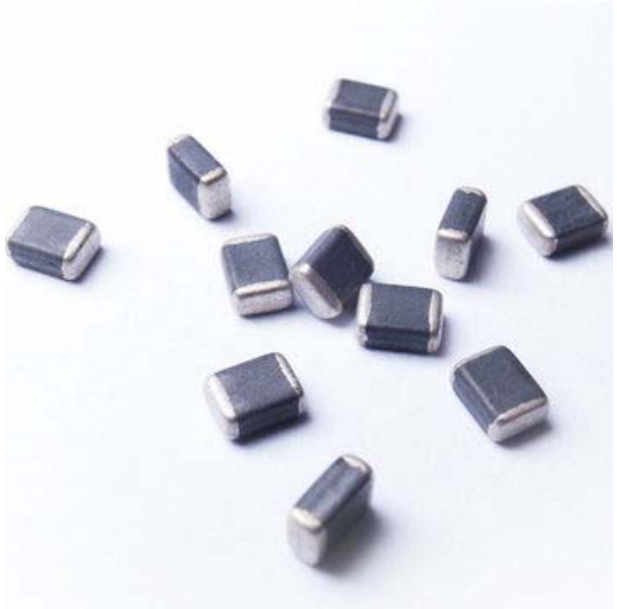
New Approach - E4990a with 42941a Impedance Probe

- Instead of using a custom fixture PCB, use a probe designed to measure PCB impedance
- Example: 42941a Impedance Probe
  - Probe jaws can be adjusted to match device under test
  - Stand steadies probe and improves repeatability
  - Ideal for measuring modules with commutation loop inductance less than 5 nH



Validation of Impedance Analysis Metrology

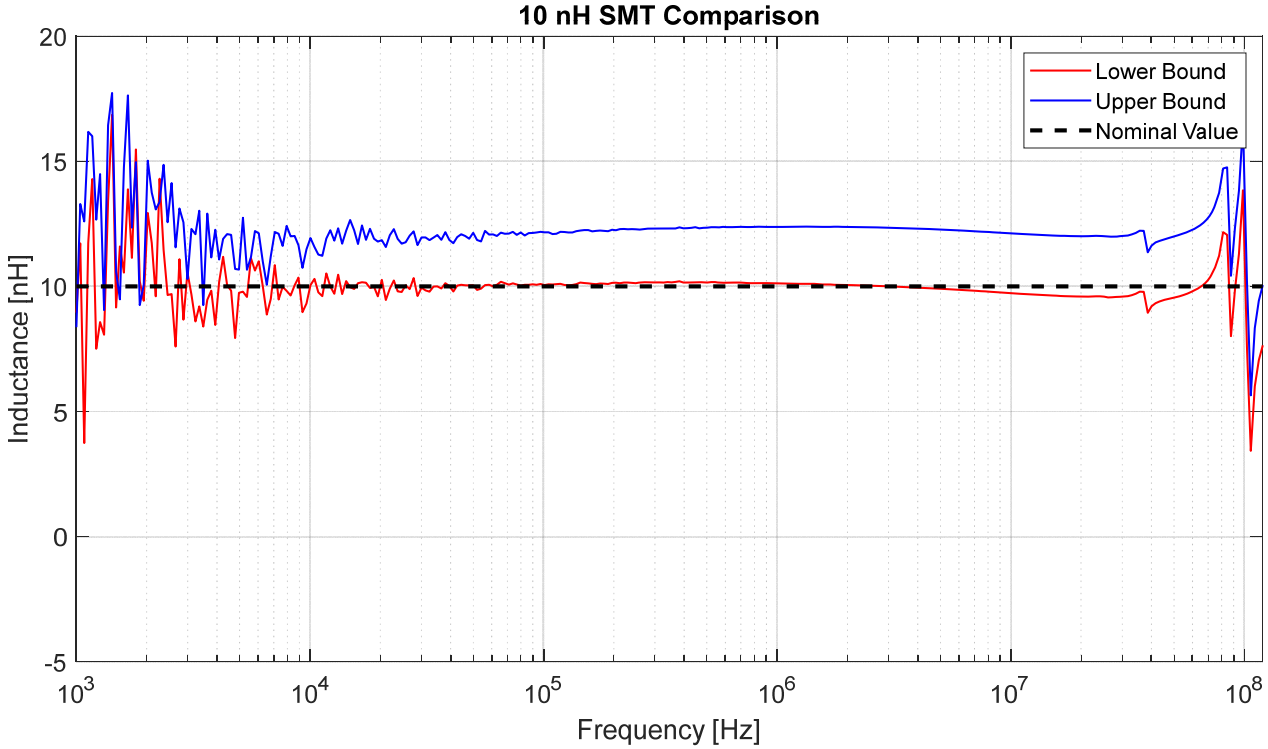
- How accurately can we measure inductances lower than 5 nH?
  - Measurements are subject to random + systematic error
  - Outliers occur due to contact impedance and other factors
- Approach: use a series of reference cases to determine an appropriate procedure and establish uncertainty ranges
- Procedure:
  - Take mean of 10 measurements and exclude outliers
  - Run two compensations: an overestimate and an underestimate of true fixture impedance
  - Use the two compensations to estimate a lower and upper measurement bound



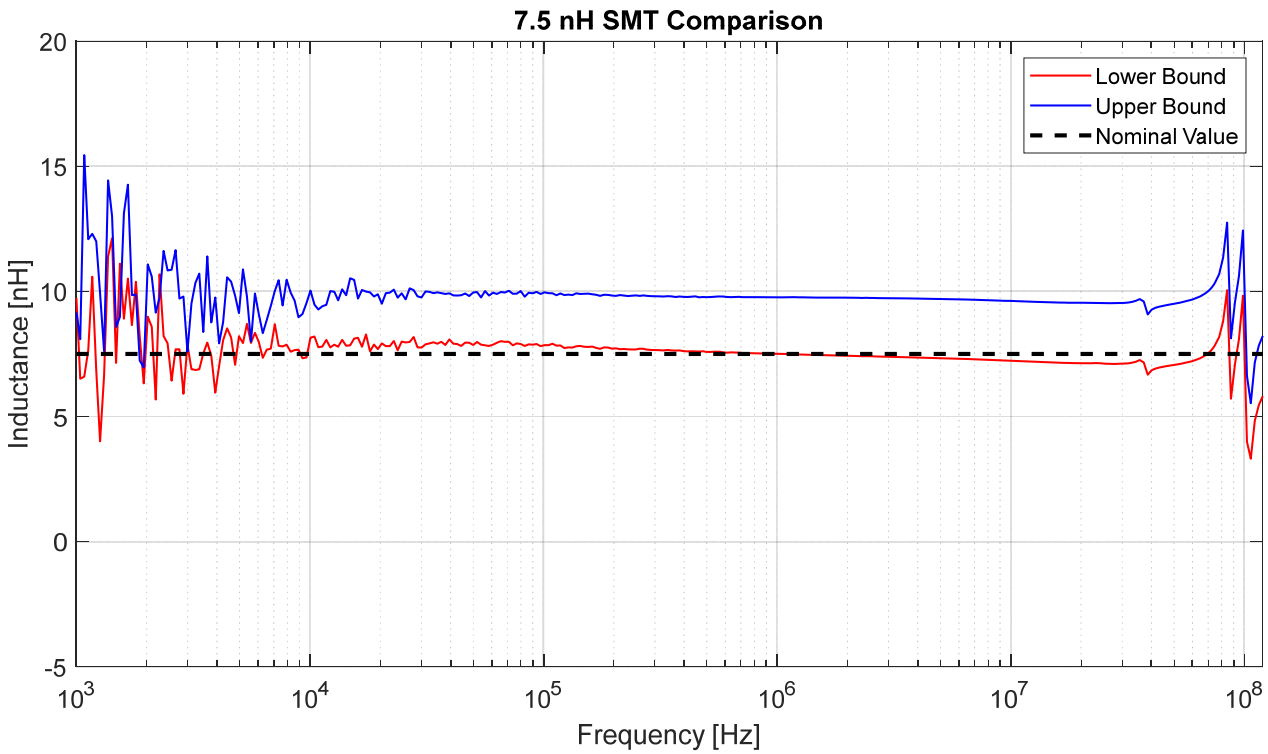
Five SMT inductors selected for reference / validation cases:

1 nH, 2.5 nH, 5 nH, 7.5 nH, 10 nH

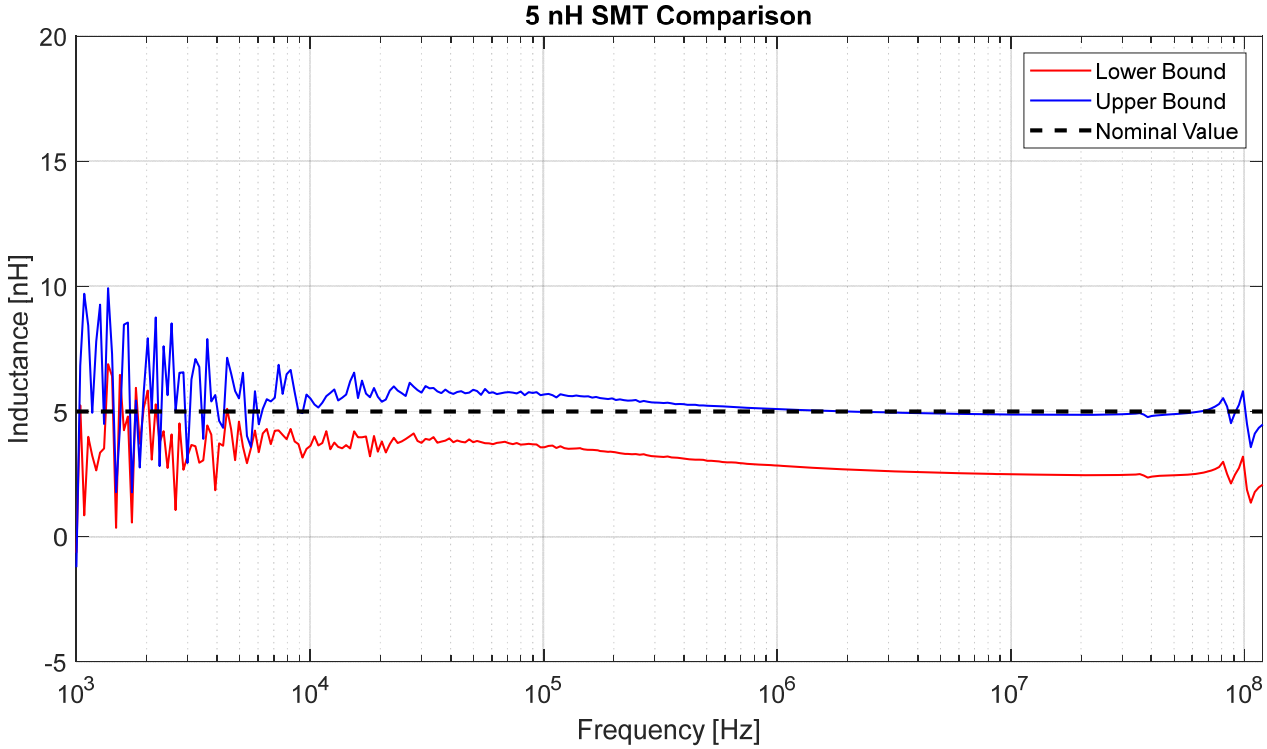
Impedance Analysis Validation: 10 nH



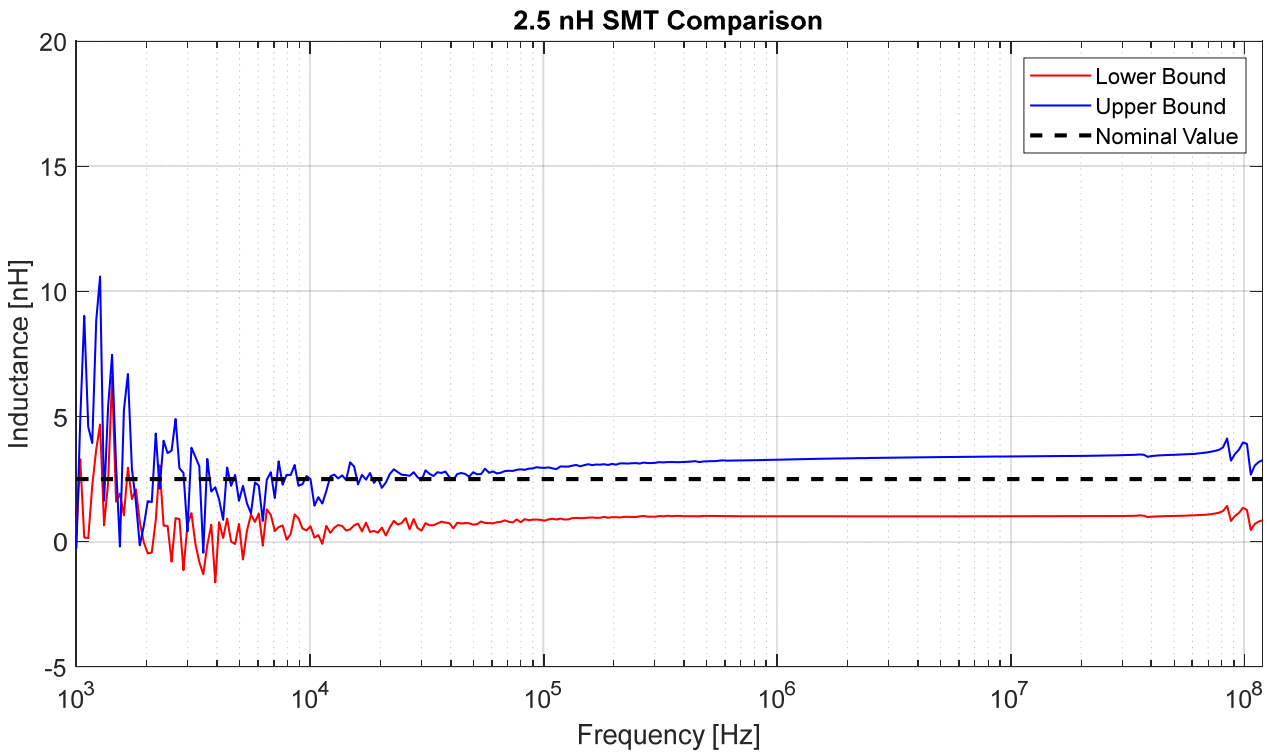
Impedance Analysis Validation: 7.5 nH



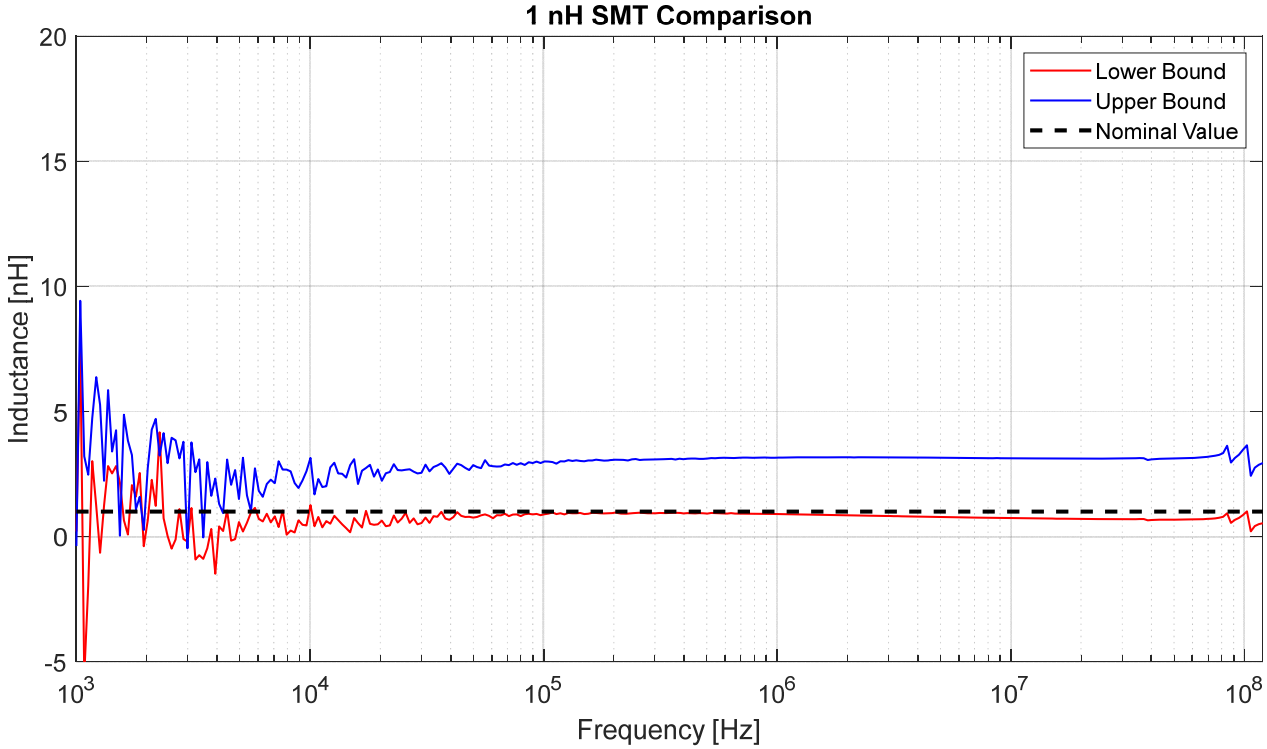
Impedance Analysis Validation: 5 nH



Impedance Analysis Validation: 2.5 nH

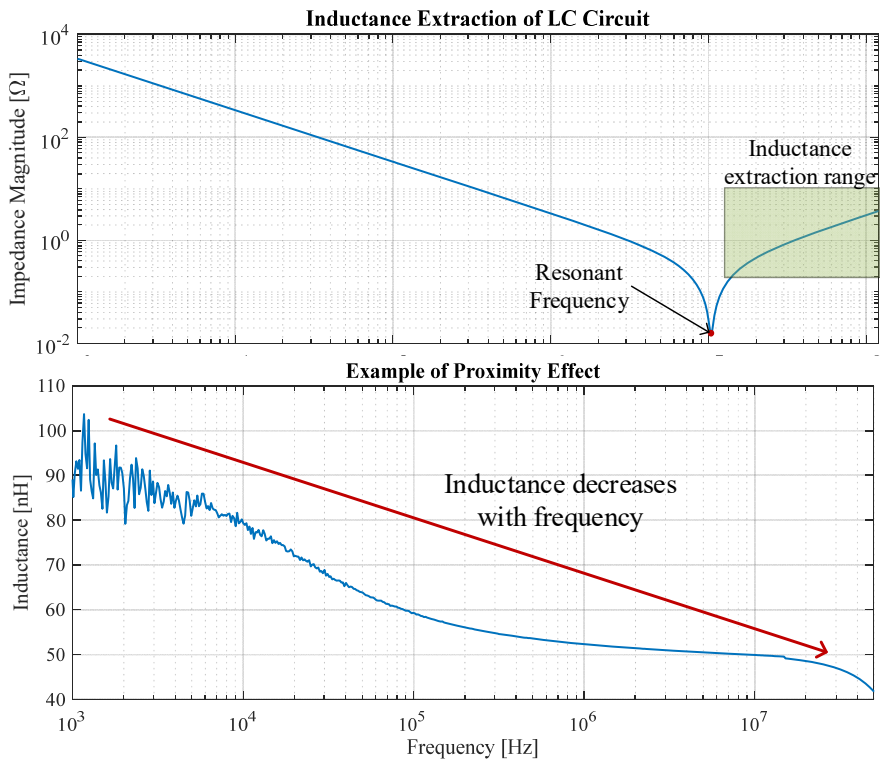


Impedance Analysis Validation: 1 nH



Module Impedance Measurement Considerations

- Using UA's new technique, uncertainty of ±1 nH can be obtained for inductances down to low single-digit nH values
- This is superior to other techniques described in the literature that involve measuring through the device capacitances
  - Inductance is **frequency dependent** due to proximity effect
  - Known techniques only support inductance estimation beyond the resonant frequency [18]



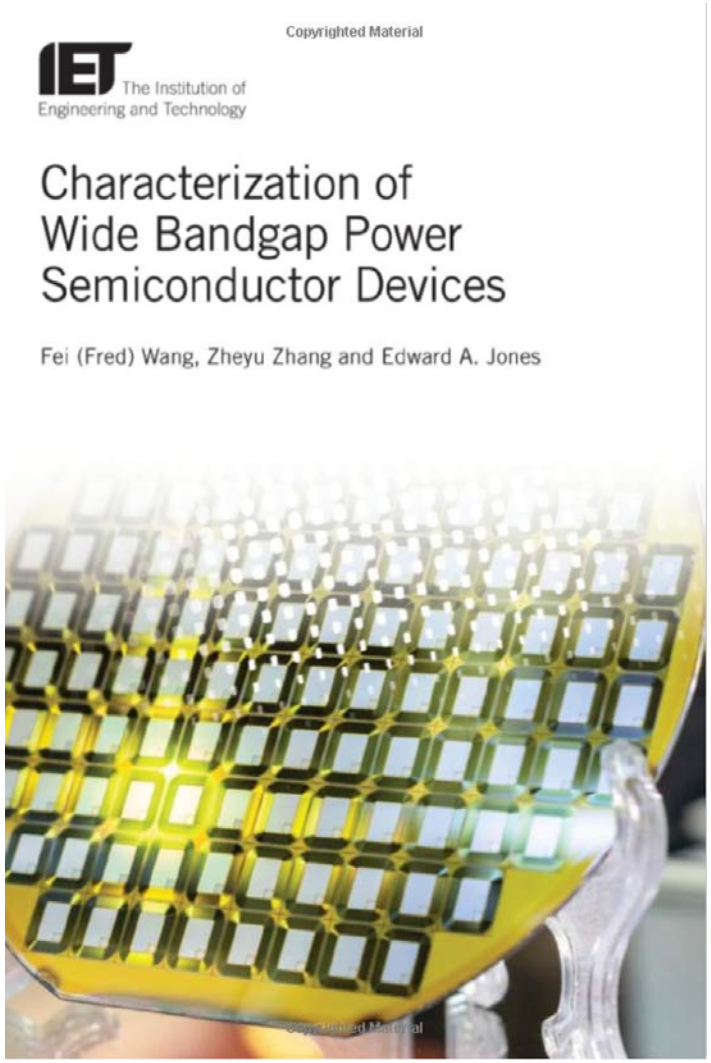
[18] T. Liu, Y. Feng, Y. Zhou, R. Ning, T. T. Y. Wong and Z. J. Shen, "Comparison of Impedance Measurement Techniques for Extracting Parasitic Inductance of SiC MOSFETs," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 7016-7023.

CONCLUSIONS

Conclusions

- WBG application design stands at the junction of power electronics & RF design
- Resulting “near-RF” behavior has significant implications for WBG-based systems
- Current metrology practices for power electronics are not adequate for measurement of these circuits
- The power electronics community is beginning to realize the implications of fast-switching for metrology
- Better metrology techniques are clearly needed at multiple “layers”:
  - Better equipment / probes
  - Better sensor attachments
- This is likely to be an active area of research for many years to come, particularly at medium voltage levels

For Further Reading



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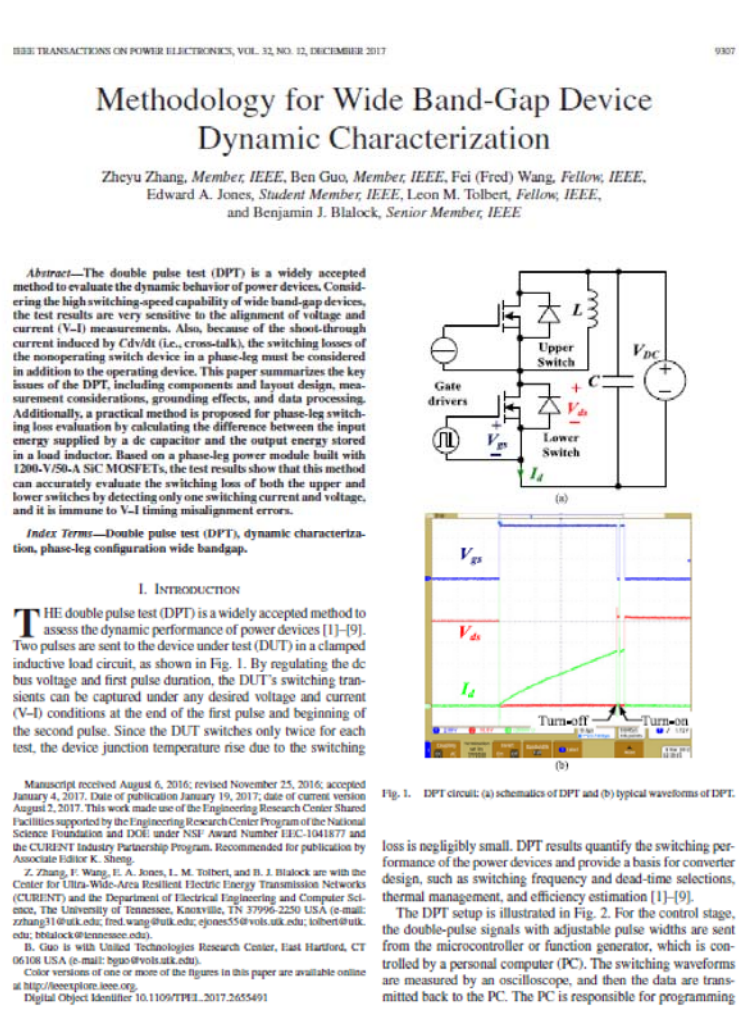
Characterization of Wide Bandgap Power Semiconductor Devices

Fei (Fred) Wang, Zheyu Zhang and Edward A. Jones



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Methodology for Wide Band-Gap Device Dynamic Characterization

Zheyu Zhang, *Member, IEEE*, Ben Guo, *Member, IEEE*, Fei (Fred) Wang, *Fellow, IEEE*, Edward A. Jones, *Student Member, IEEE*, Leon M. Tolbert, *Fellow, IEEE*, and Benjamin J. Blalock, *Senior Member, IEEE*

***Abstract*—The double pulse test (DPT) is a widely accepted method to evaluate the dynamic behavior of power devices. Considering the high switching-speed capability of wide band-gap devices, the test results are very sensitive to the alignment of voltage and current (V–I) measurements. Also, because of the shoot-through current induced by *Cdv/dt* (i.e., cross-talk), the switching losses of the nonoperating switch device in a phase-leg must be considered in addition to the operating device. This paper summarizes the key issues of the DPT, including components and layout design, measurement considerations, grounding effects, and data processing. Additionally, a practical method is proposed for phase-leg switching loss evaluation by calculating the difference between the input energy supplied by a dc capacitor and the output energy stored in a load inductor. Based on a phase-leg power module built with 1200-V/50-A SiC MOSFETs, the test results show that this method can accurately evaluate the switching loss of both the upper and lower switches by detecting only one switching current and voltage, and it is immune to V–I timing misalignment errors.**

***Index Terms*—Double pulse test (DPT), dynamic characterization, phase-leg configuration wide bandgap.**

I. Introduction

THE double pulse test (DPT) is a widely accepted method to assess the dynamic performance of power devices [1]–[9]. Two pulses are sent to the device under test (DUT) in a clamped inductive load circuit, as shown in Fig. 1. By regulating the dc bus voltage and first pulse duration, the DUT's switching transients can be captured under any desired voltage and current (V–I) conditions at the end of the first pulse and beginning of the second pulse. Since the DUT switches only twice for each test, the device junction temperature rise due to the switching loss is negligibly small. DPT results quantify the switching performance of the power devices and provide a basis for converter design, such as switching frequency and dead-time selections, thermal management, and efficiency estimation [1]–[9].

The DPT setup is illustrated in Fig. 2. For the control stage, the double-pulse signals with adjustable pulse widths are sent from the microcontroller or function generator, which is controlled by a personal computer (PC). The switching waveforms are measured by an oscilloscope, and then the data are transmitted back to the PC. The PC is responsible for programming

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Fig. 1. DPT circuit: (a) schematics of DPT and (b) typical waveforms of DPT.