Metrology Considerations for Accurate Characterization of High-Bandwidth Power Electronics Components & Applications

Andy Lemmon, Ph.D., P.E.
Assistant Professor
Dept. of Electrical & Computer Engineering
The University of Alabama
lemmon@eng.ua.edu
Acknowledgments - Sponsors

Research Sponsors - Government

- Department of the Navy
- ARL
- Air Force Research Laboratory

Research Sponsors - Industry

- Wolfspeed
- Microchip
- Microsemi
- Cree

U.S. Department of Energy

Monolith Semiconductor Inc.
Acknowledgments - Collaborators

Collaborating U.A. Faculty
Dr. Aaron Brovont, Assistant Professor

Students (Current & Former)
Overview

• Introduction
• Metrological Challenges for WBG Systems
  – Example 1: Voltage measurements
  – Example 2: Current measurements
  – Example 3: Packaging Impedance measurements
• Look Ahead & Conclusion
INTRODUCTION
Motivating Example

1.2 kV SiC MOSFET

1.2 kV “High Speed” Si IGBT
SiC MOSFET vs. Si IGBT: Time Domain

- **SiC**
  - Turn Off
    - Voltage (V)
    - Current (A)
  - Turn On
    - Voltage (V)
    - Current (A)

- **Si**
  - Turn Off
    - Voltage (V)
    - Current (A)
  - Turn On
    - Voltage (V)
    - Current (A)

**Low Switching Loss**: 😊
**Pronounced Ringing**: 😞
**High Switching Loss**: 😞
**Negligible Ringing**: 😊
**Power Electronics: Spectral Considerations**

- **Traditional IGBT-based systems:**
  - Operation Frequencies to ~50 kHz
  - Easily-suppressed extended dynamics
  - Lumped circuit analysis works well
  - Packaging impedances are not critically important

- **WBG-based systems:**
  - Operation Frequencies to a few MHz
  - Extended dynamics to ~100 MHz
  - Lumped circuit analysis in question
  - Packaging impedances are critically important in “Near-RF” domain

---

Fast, High-Voltage Measurements

EXAMPLE 1
Case Study: “Standard” Passive 300V 10x Probe

- For DC, attenuation accomplished by $R_{SCOPE}$ & $R_{PRB}$
- For AC, attenuation accomplished by $(C_{PRB})$ & $(C_{ADJ} + C_{CABLE} + C_{SCOPE})$
- Works (mostly) great, except for $L_{PRB}$!
Example Probe for Test Case

- Case study based loosely on Tektronix Setup at UA:
  - Tek P5050B Probe
    » $R_{PRB}: 9 \, \text{M}\Omega$
    » $C_{PRB}: 12 \, \text{pF} \,(8 \, \text{pF})$
    » $C_{CABLE}: 100 \, \text{pF} \,(\sim 3 \, \text{meters})$
  - Tek 4000B Oscope
    » $R_{SCOPE}: 1 \, \text{M}\Omega$
    » $C_{PRB}: 13 \, \text{pF}$
    » $C_{ADJ}: 0-1 \, \text{pF}$
  - $L_{PRB}$ Varied 22 nH – 200 nH
  - Ground lead inductance is approximately 20 nH per inch [4]

Effect of Ground Lead Inductance

![Graph showing the effect of ground lead inductance on magnitude and phase at different frequencies. The graph compares the performance for different values of inductance (200 nH, 100 nH, 22 nH). The magnitude is measured in dB, and the phase is measured in degrees. At 1 MHz, 10 MHz, and 100 MHz, the plots show significant variation due to the inductance value.](image)
**Problem #1: Bandwidth**

<table>
<thead>
<tr>
<th></th>
<th>L_GND 22 nH</th>
<th>100 nH</th>
<th>200 nH</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Resonant Freq.</strong></td>
<td>320 MHz</td>
<td>150 MHz</td>
<td>106 MHz</td>
</tr>
<tr>
<td><strong>Bandwidth -3 dB</strong></td>
<td>500 MHz</td>
<td>233 MHz</td>
<td>165 MHz</td>
</tr>
<tr>
<td><strong>Bandwidth +3 dB</strong></td>
<td>172 MHz</td>
<td>80.3 MHz</td>
<td>56.8 MHz</td>
</tr>
</tbody>
</table>
Problem #2: Probe Compensation Sensitivity

- Need for passive probe compensation is well-known
- Ensures the accuracy of transient response esp. with fast edge rates
- Common procedures
  - Manual comp. with built-in 1 kHz
  - Auto-compensation with ASIC-enabled probes

Credit: [5]

If your probe calibration signal looks like either of this,

Compensate your probe!

Problem #3: Resonances

- Fast edge rates of 20-80 V/ns excite resonances in:
  - Application parasitics
  - Oscilloscope input impedance
- Example at right shows a “slow” WBG voltage transition (20 V/ns) with no application parasitics
- All visible resonance is the result of probe resonance, using 10x model
- Values of GND lead inductance considered:
  - 22 nH
  - 100 nH
  - 200 nH
Mitigation of Ground Lead Inductance Effects

- Mitigation methods currently available:
  - Probe-tip adapters are available (Tek, Keysight, CalTest)
  - Tinned copper can make a reasonable substitute
- However, these methods have limits for WBG power electronics
  - Restricted to Ground-referenced probes
  - Not designed for measurements above ~200V
  - Things get very difficult at MVDC levels
Tektronix BNC Probe-Tip Adapter

- Tek BNC Probe tip adapter effectively suppresses (most) ground-lead effects
- Problem: BNC Connectors are only rated for 500 V
High-Bandwidth Current Measurement

EXAMPLE 2
• Ringing in WBG device currents can reach 50-100 MHz
• Bandwidth requirements specified in the literature as [6]:
  – 5x bandwidth over the frequency of interest for magnitude fidelity
  – 10x bandwidth over the frequency of interest for phase fidelity
• The high bandwidth requirement eliminates techniques such as hall effect sensors and Rogowski coils

Current Measuring Difficulties - Inductance

- Methods with adequate bandwidth introduce a “choke-point” into the system
- The DC bus must be routed through a small sensor aperture
- The “choke-point” causes an attendant increase in the bus inductance
- The additional parasitic inductance exacerbates undesirable ringing

• DPT evaluations at 600 V & a range of currents were performed with this setup
• The bus was designed to allow multiple simultaneous current measurements - two CTs and one of the three custom PCBs
• The multiple measurements enabled comparisons under identical test conditions
• Before each measurement, the probes were de-skewed to ensure consistent V–I alignment
DPT Results – Coaxial Shunt vs. “Slow” CT

- With the discrete SiC MOSFET, the 20 MHz CT does not accurately track the device current
  - Significant magnitude errors
  - Excessive overshoot during ringing
  - Phase mismatches

- Conclusion: CT is not sufficient for discrete SiC MOSFET characterization, but may be used (cautiously) for power module characterization
Packaging Impedance Measurement

EXAMPLE 3
Frequency Dependence of Parasitic Inductance
Measurement-Based Parasitic Modeling Procedure – Developed at UA

Module Adapter PCB Design → Module Adapter Fabrication → Frequency-Domain Parasitic Measurements

Transient Comparison / Validation → Double-Pulse Testing → LTspice modeling

Example SiC Module Parasitic Measurement Fixture

- Module fixture performs two functions:
  - Adapts module terminals to VNA connectors
  - Provides a mechanism to extend calibration plane to module surface
- Measured loop inductance includes module geometry, with interface adapter
- Compensation process (ideally) removes the influence of the fixture

1.2 kV, 120A SiC MOSFET
Module Test Subject

Power Module Fixture PCB Generations

Second Generation

First Generation

Third Generation

Match Instrument Connector Spacing (Cable Elimination)
Fourth-Generation Measurement Fixture with Flex PCB

Fourth Generation Fixture

Fixture Attached to XHV-6

XHV-6 Parasitic Extraction
• UA has performed parasitic modeling for >25 modules over the last 3 years
• The fixture design process has been substantially improved during this time
• Key findings have been detailed in an article published in *IEEE Transactions on Instrumentation and Measurement*
  – All fixtures introduce some error into measurements
  – Error increases when the fixture impedance is on the same order as the DUT impedance
• Very low parasitic modules are extremely difficult to characterize properly
• What if we could get away without using a fixture?

New Approach - E4990a with 42941a Impedance Probe

• Instead of using a custom fixture PCB, use a probe designed to measure PCB impedance
• Example: 42941a Impedance Probe
  – Probe jaws can be adjusted to match device under test
  – Stand steadies probe and improves repeatability
  – Ideal for measuring modules with commutation loop inductance less than 5 nH
Validation of Impedance Analysis Metrology

• How accurately can we measure inductances lower than 5 nH?
  – Measurements are subject to random + systematic error
  – Outliers occur due to contact impedance and other factors

• Approach: use a series of reference cases to determine an appropriate procedure and establish uncertainty ranges

• Procedure:
  – Take mean of 10 measurements and exclude outliers
  – Run two compensations: an overestimate and an underestimate of true fixture impedance
  – Use the two compensations to estimate a lower and upper measurement bound

Five SMT inductors selected for reference / validation cases:
1 nH, 2.5 nH, 5 nH, 7.5 nH, 10 nH
Impedance Analysis Validation: 10 nH
Impedance Analysis Validation: 7.5 nH
Impedance Analysis Validation: 5 nH
Impedance Analysis Validation: 2.5 nH
Impedance Analysis Validation: 1 nH
Module Impedance Measurement Considerations

• Using UA’s new technique, uncertainty of ±1 nH can be obtained for inductances down to low single-digit nH values
• This is superior to other techniques described in the literature that involve measuring through the device capacitances
  – Inductance is **frequency dependent** due to proximity effect
  – Known techniques only support inductance estimation beyond the resonant frequency

CONCLUSIONS
Conclusions

- WBG application design stands at the junction of power electronics & RF design
- Resulting “near-RF” behavior has significant implications for WBG-based systems
- Current metrology practices for power electronics are not adequate for measurement of these circuits
- The power electronics community is beginning to realize the implications of fast-switching for metrology
- Better metrology techniques are clearly needed at multiple “layers”:
  - Better equipment / probes
  - Better sensor attachments
- This is likely to be an active area of research for many years to come, particularly at medium voltage levels
Methodology for Wide Band-Gap Device Dynamic Characterization

Zheyu Zhang, Member, IEEE, Ben Guo, Member, IEEE, Fei (Fred) Wang, Fellow, IEEE, Edward A. Jones, Student Member, IEEE, Leon M. Tolbert, Fellow, IEEE, and Benjamin J. Blalock, Senior Member, IEEE

Advantages—The double pulse test (DPT) is a widely accepted method to evaluate the dynamic behavior of power devices. Considering the high switching speed capability of wide band-gap devices, the test results are very sensitive to the alignment of voltage and current (V-I) measurements. Also, because of the short duration of the switching events, the switching losses of the power semiconductor device in a phase-leg configuration must be measured in addition to the operating device. This paper summarizes the key lessons of the DPT, including components and circuit design, measurement considerations, triggering effects, and data processing. Additionally, a practical method is proposed for phase-leg switching loss evaluation by calculating the difference between the input power supplied by the dc capacitor and the output energy stored in the load inductor. Based on a phase-leg power module built with SiC MOSFETs, the test results show that this method can accurately evaluate the switching loss of both the upper and lower switches by detecting only one switching current and voltage, and it is immune to V-I timing misalignment errors.

One term—phased configuration-configuration, phase-leg configuration wide bandgap.

1. Introduction

The double pulse test (DPT) is a widely accepted method to assess the dynamic performance of power devices [1–9]. Two pulses are sent to the device under test (DUT) in a clamped inductive load circuit, as shown in Fig. 1. By regulating the dc bus voltage and first pulse duration, the DUT’s switching transients can be captured under any desired voltage and current (V-I) conditions at the end of the first pulse and beginning of the second pulse. Since the DUT switches only twice for each test, the device junction temperature rise due to the switching transients is negligible small. DPT results quantify the switching performance of the power devices and provide a basis for component design, such as switching frequency and d-c link selection, thermal management, and efficiency estimation [1–9].

The DPT setup is illustrated in Fig. 2. For the control stage, the double-pulse signals with adjustable pulse width are sent from the microcontroller or function generator, which is controlled by a personal computer (PC). The switching waveforms are measured by an oscilloscope, and then the data are transmitted back to the PC. The PC is responsible for programming...