Materials for 3D Integration

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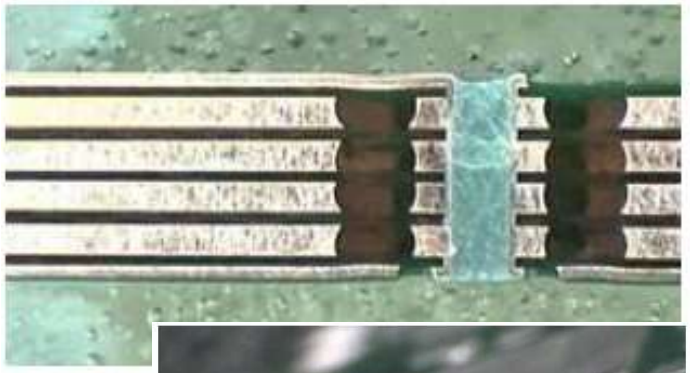
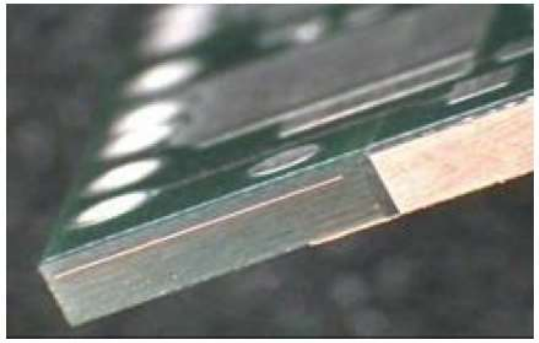
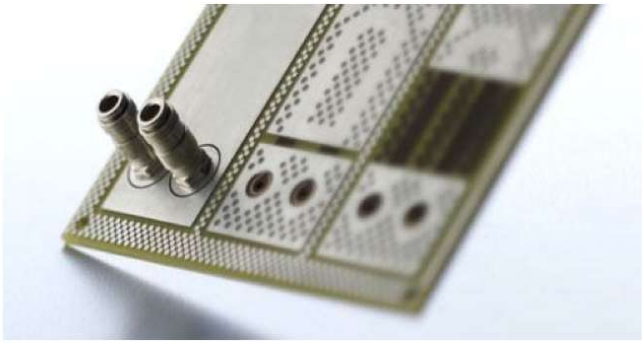
Circuit Board/Substrate Elements of 3D Power Integration

- Some thick copper layers
- Thermal vias
- Cu inlays
- Embedded Cooling



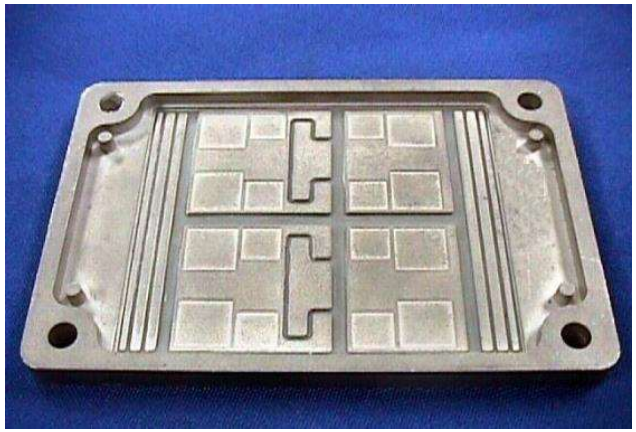




Conductive Layers

MATERIAL	K(x,y) (W/mK)	CTE(x,y) (ppm/K)	DENSITY (g/cm^3)	K/ρ (W/mK)/(g/cm^3)
Diamond/Al	550-600	7.0-7.5	3.1	177-194
Diamond/Cu	550-600	4.0-6.0	-	-
Diamond/SiC	600	1.8	3.3	180
Graphite Flake/Al*	650	4.5-5.0	2.1	310
HOPG*	1500	-1	2.3	650)

* Inplane isotropic - K(z) much lower



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Circuit Board/Substrate Elements of 3D Power Integration

- Embedded Passives
  - Inductors/ Transformers
  - Capacitors
    - Pwr/Gnd decoupling
  - Resistors
    - +/- 20%
  - EMI filters

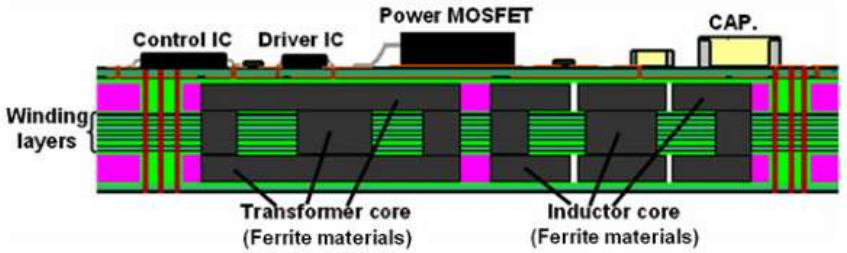


Fig.1 Structure schematic of converter based on embedded passive substrate

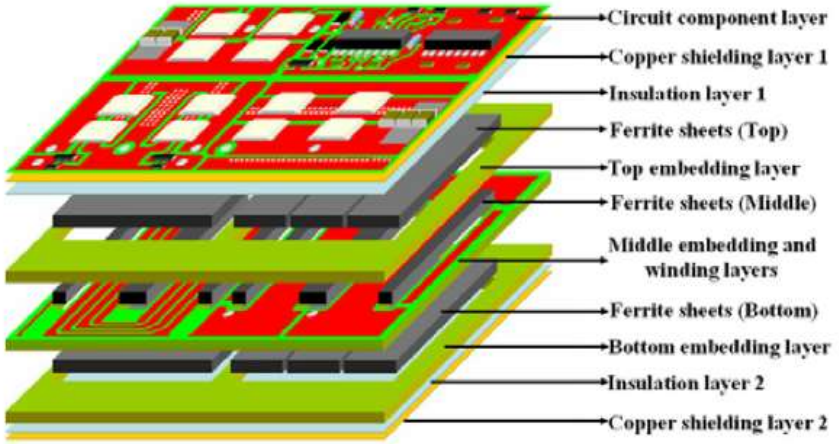
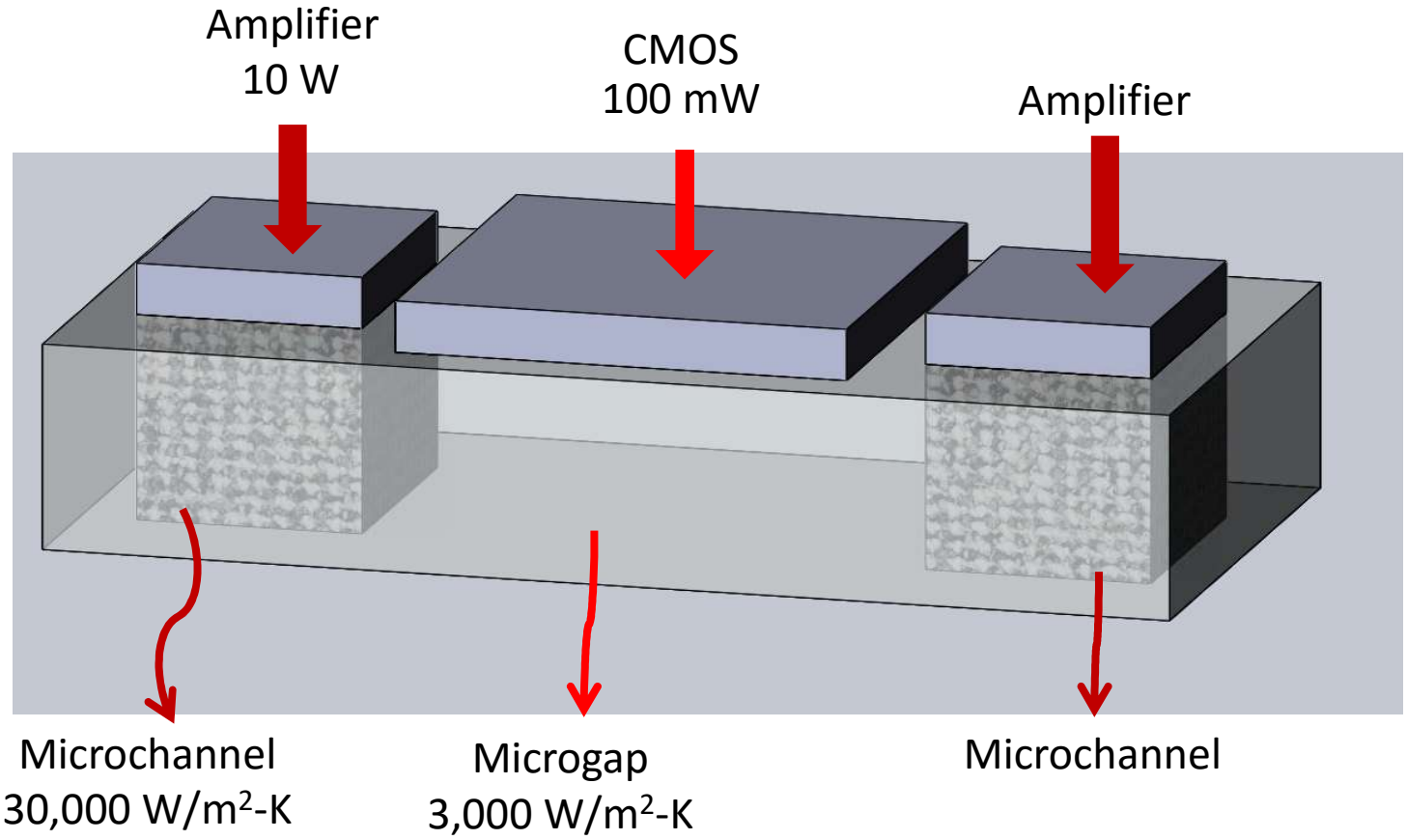


Fig.2 Exploded view of converter based on embedded passive substrate

Images: Zhankun Gong; Qiaoliang Chen; Xu Yang; Bo Yuan; Weiyi Feng; Zhaoan Wang, "Design of high power density DC-DC converter based on embedded passive substrate," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* , vol., no., pp.273,277, 15-19 June 2008

Chiplet on Substrate

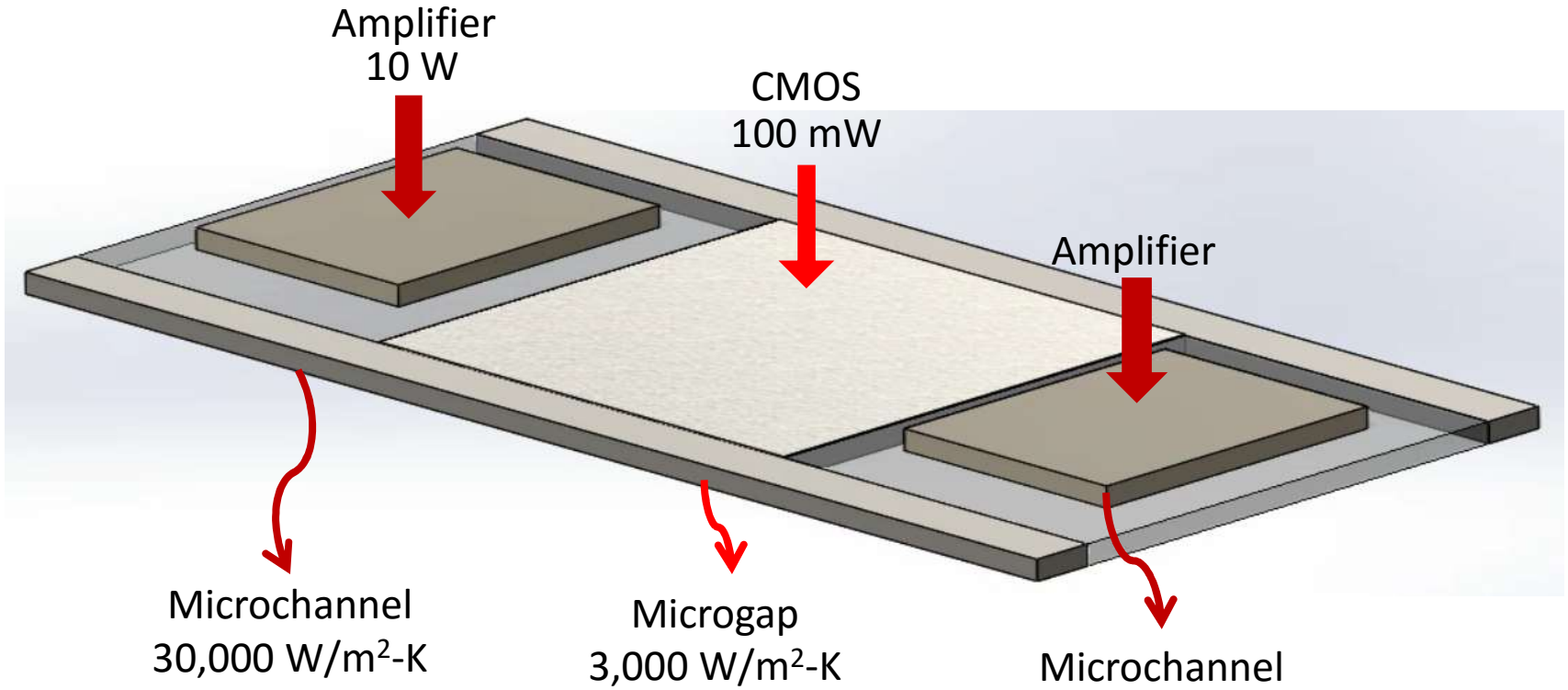
Low and high power dissipating chiplets located on a common low conductivity substrate with TXV and microchannel cooling under higher flux areas.



GOAL: Examine temperature rise of individual chips (e.g. CMOS) from heat generated by power amplifier chip

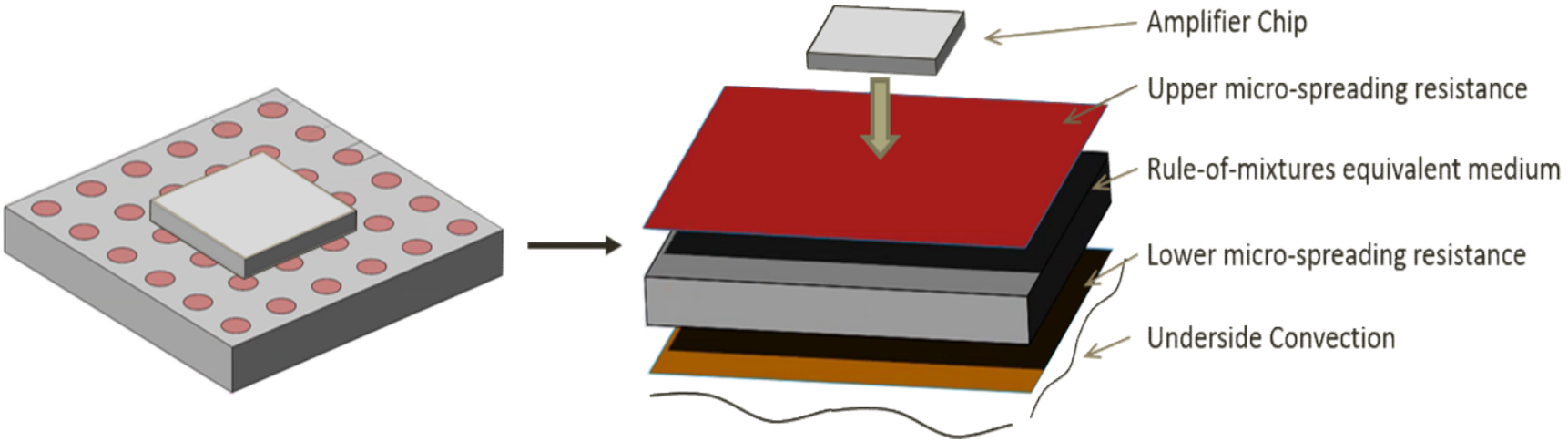
Chiplet on Chip

CMOS device is patterned on base silicon wafer. High power dissipating chiplets are placed on via-enhanced low-k material deposited on base wafer and joined to differential cooling.



Examining incorporating these thermal isolation techniques into DAHI SoC

Modeling Structure



- For the analysis, a simplified, one-component isolation model was used.
- A "hot" chip was attached (with die attach layers, not shown) to a via-enhanced interposer with underside convective cooling.
- The homogenized, equivalent model uses anisotropic interposer properties and introduces upper and lower micro-spreading resistances.
- The interposer is assumed to extend far enough beyond the chip to reach a temperature rise of zero (no edge effects, i.e. infinite extent).

Effect of Film on Temperature

A copper film dramatically reduces the spreading resistance, by smoothing the transition between the convection boundary and the interposer surface. For these system parameters, the optimal film thickness is between 6 and 25 µm.

Interface	T_{avg} [K] 6 µm film	T_{avg} [K] 15 µm film	T_{avg} [K] 25 µm film
Top of Chip	71.75	71.66	71.68
Interposer-Chip	70.67	70.58	70.60
Film-Interposer	66.69	66.74	66.79
Bottom of Film	66.66	66.66	66.66

ΔT_{avg} by layer	ΔT_{avg} Case 3 [K]	ΔT_{avg} [K] 6 µm film	ΔT_{avg} [K] 15 µm film	ΔT_{avg} [K] 25 µm film
SiC	~ 1	1.08	1.08	1.08
Interposer	45	3.98	3.84	3.81
Film	~	0.03	0.08	0.13
Convection	66	66.66	66.66	66.66
Film + Int ΔT	**45**	**4.01**	**3.92**	**3.94**

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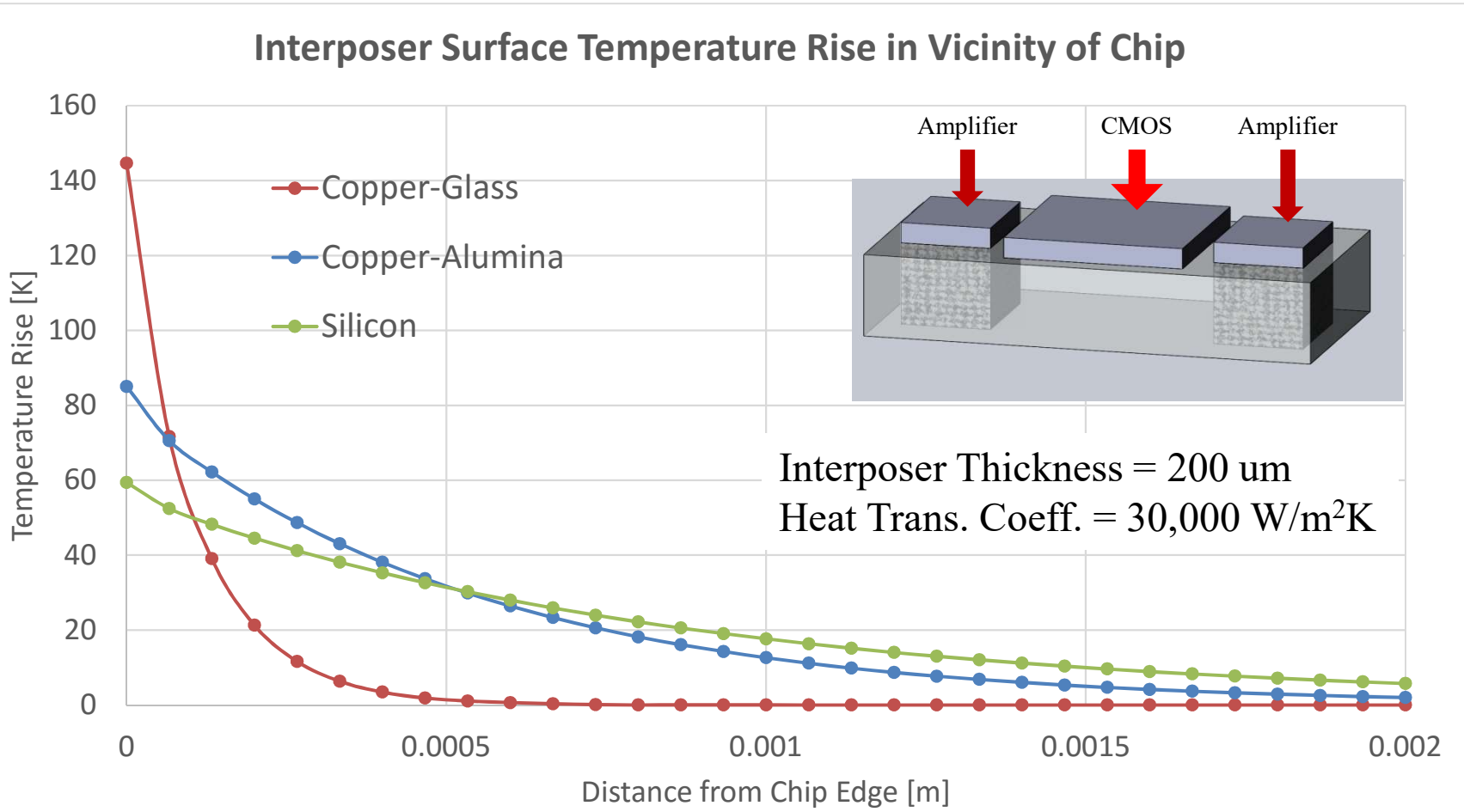
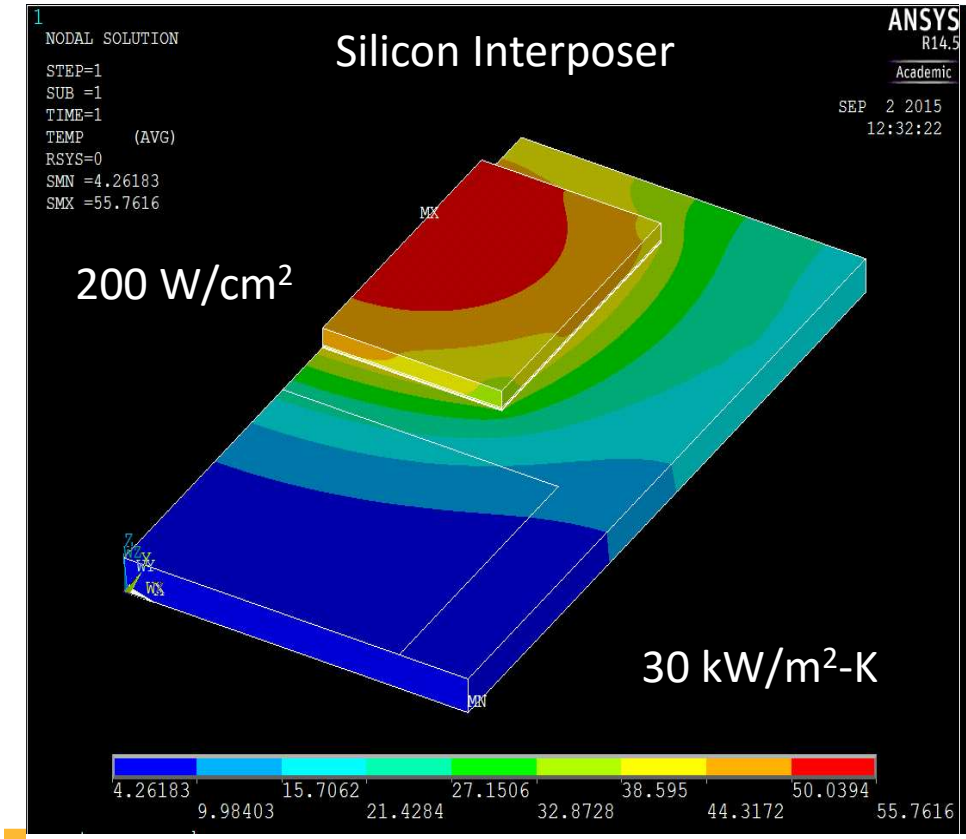
Thermal Isolation



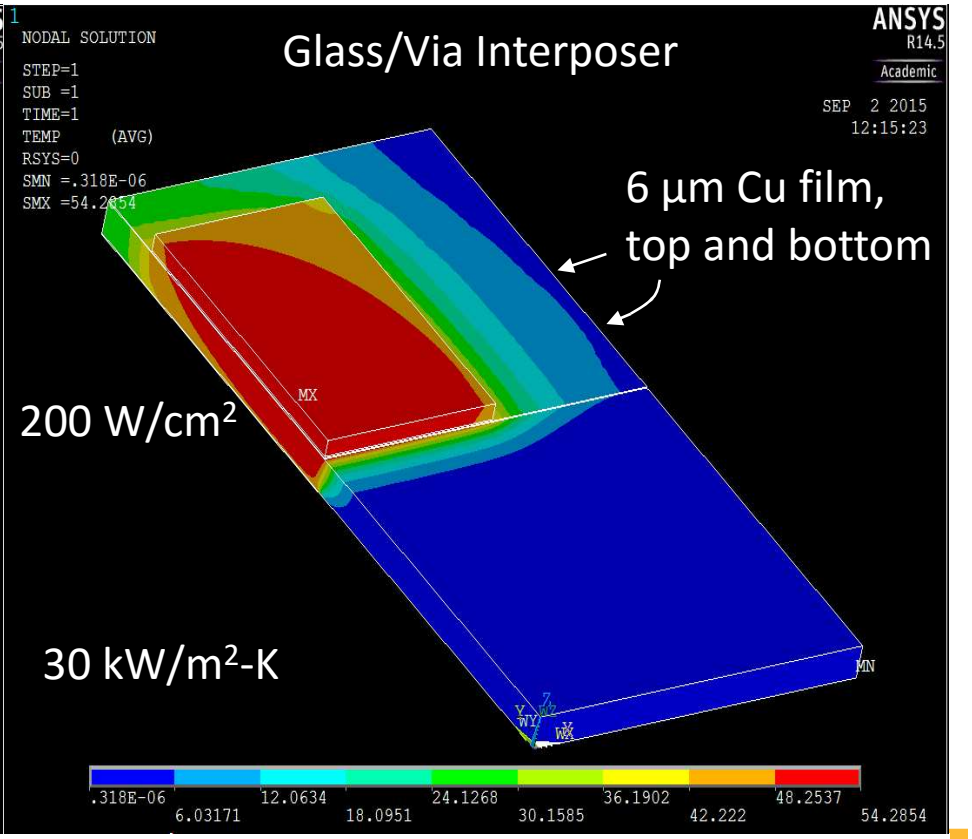
Low and high power dissipating chiplets located on a common low conductivity substrate with TXV and microchannel cooling under higher flux areas.

Heat Spreading on Different Substrates

- The lessons learned from simplified models can be applied to more complex applications
- The thin spreading films that help mitigate micro-spreading resistance can be used to direct heat toward interposer regions that will not host CMOS devices

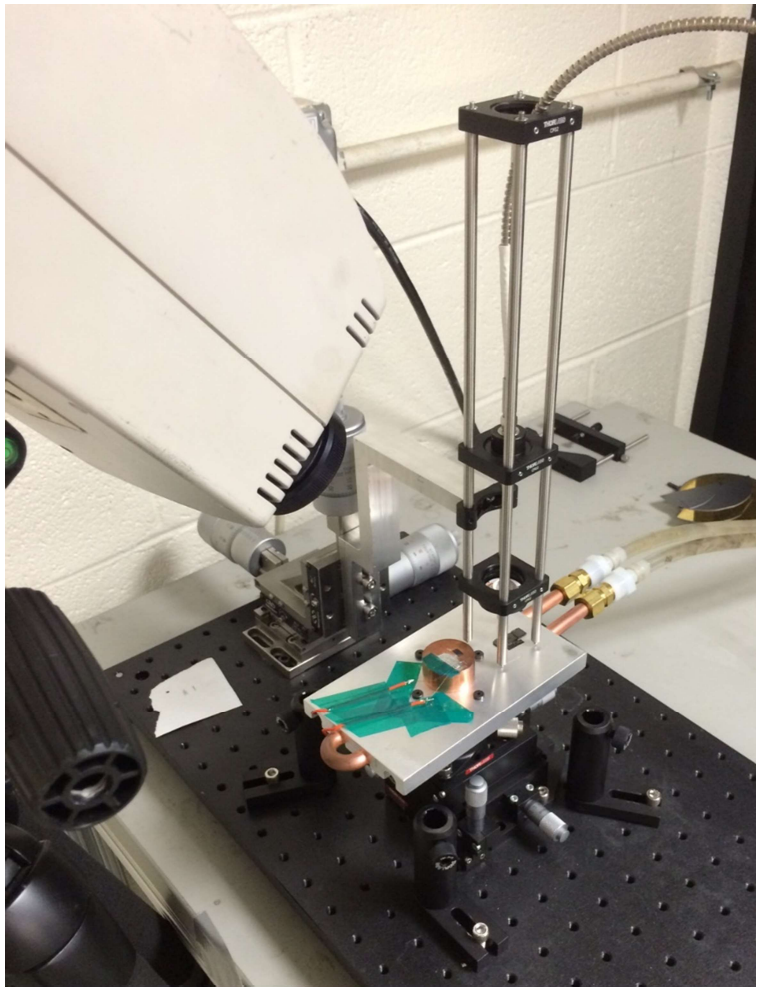


Uniform silicon interposer, with microchannel cooling under entirety



Glass interposer, with vias and a copper spreader film on top and bottom in vicinity of amplifier

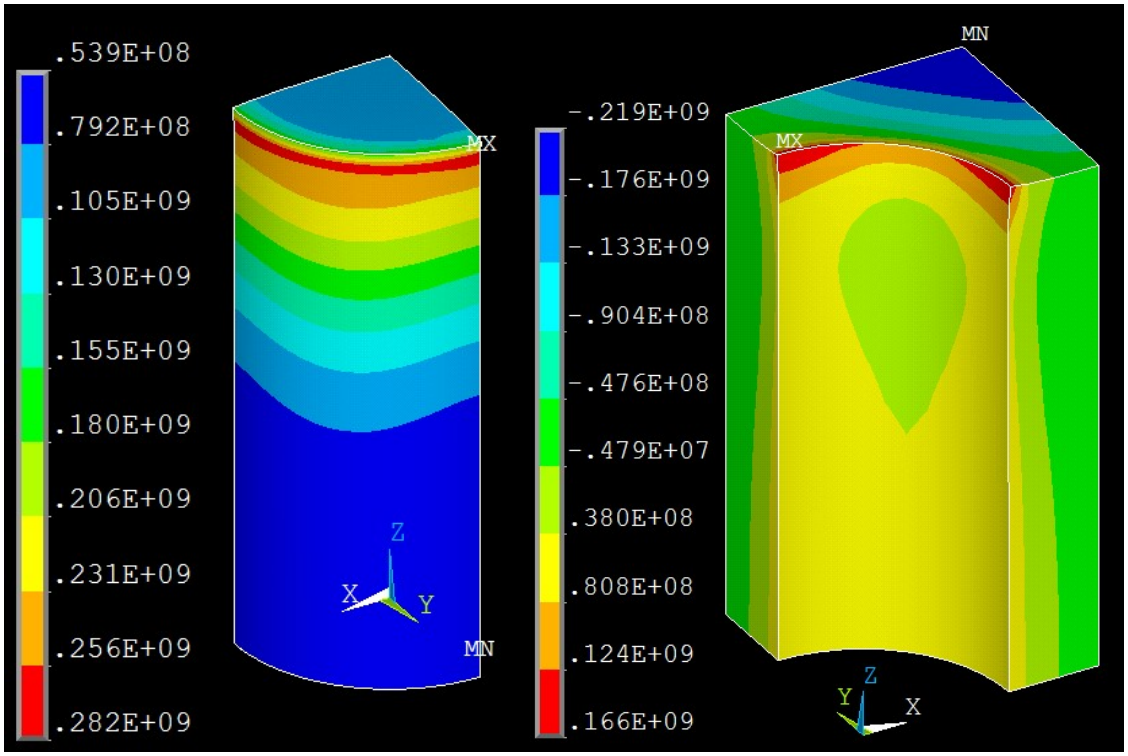
Experimental Validation and Calibration



- A Coherent 100W continuous wattage fiber laser is focused on the surface of test samples
  - Spot size focused to 2 mm diameter
- FLIR Merlin infrared camera is used to monitor surface temperature
- A thin graphite coating provides good laser absorption and IR emissivity
- Samples are adhered to an aluminum cold plate with silver-filled thermal grease
  - Future goal is direct liquid cooling using microgap/microchannel

Structural Reliability Modeling

- Thermal stress modeling is used to identify via array materials and dimensions that will have reliability concerns.
- Possible failure modes are:
  - Fatigue failure of ductile via material (via extrusion)
  - Interfacial delamination between via and substrate
  - Brittle substrate crack growth
- Trade-offs between reliability and thermal performance are being considered.
- For this case, at a hoop stress of 166 MPa in glass with a K_{IC} of 0.7 MPa$\sqrt{m}$, the critical crack size is > 5.6 μm.



Von Mises stress in copper via and hoop stress in glass substrate

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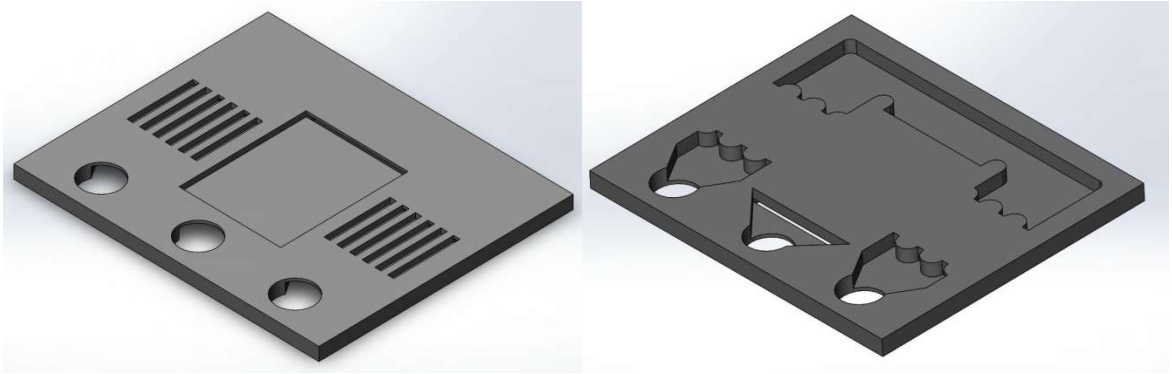
Differential Cooling Analysis

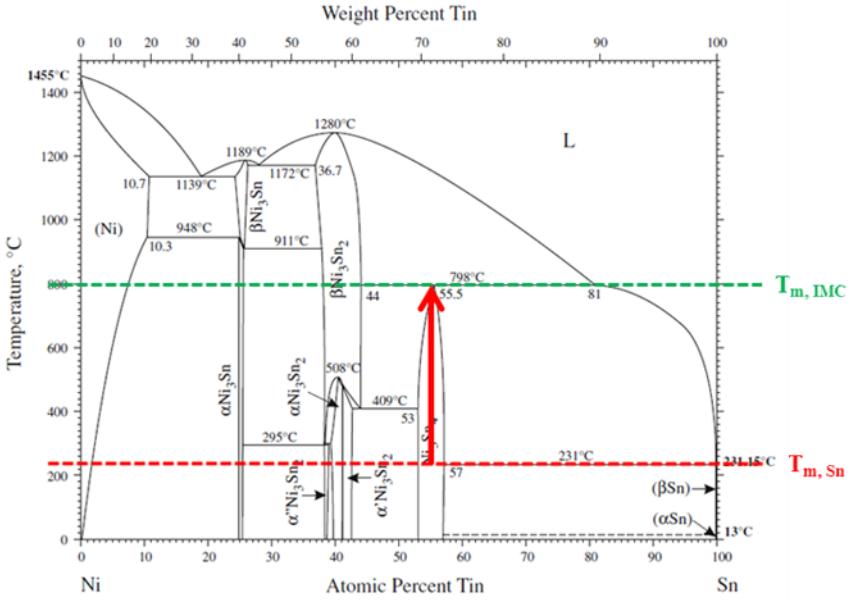
Combining microchannel and microgap coolers can significantly increase COP for the combination as a whole.



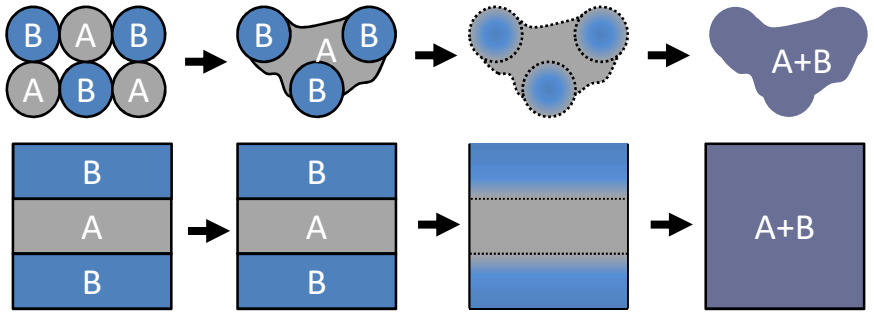
Microchannel Coolers		Microgap Coolers	
h [W/m²-K]	Areal Pump Power [W/cm²]	h [W/m²-K]	Areal Pump Power [W/cm²]
115,000 [9]	0.04	15,400 [11]	0.0011
182,000 [10]	0.1	24,000 [11]	0.133
417,000 [10]	10	37,000 (This Research)	1.0

TLPS Attach Technology

- TLPS (Transient Liquid Phase Sintering) is a liquid-assisted sintering process during which a low melting temperature constituent, *A*, melts, surrounds, and diffuses in a high melting temperature constituent *B*.
- Intermetallics with high melting temperatures are formed by liquid-solid diffusion
- TLPS systems can be processed at low temperatures but are capable of operating at the high melting temperatures of the intermetallic compounds.

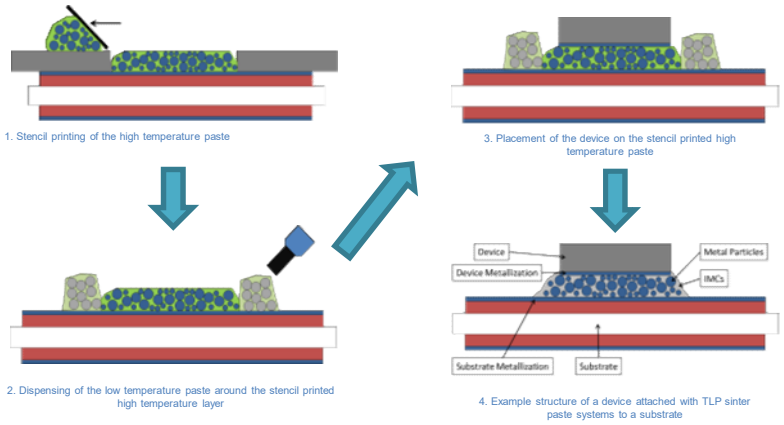


- TLPS joints with flux can be formed from low cost material systems (Cu-Sn, Ni-Sn) without pressure or vacuum. Common metallizations can be joined.

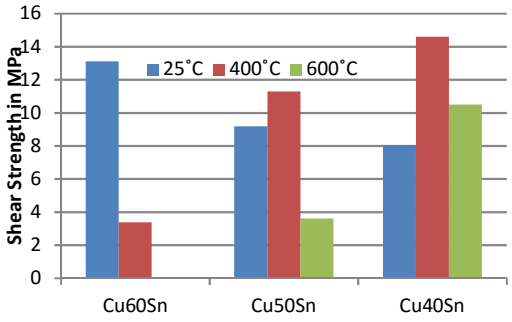


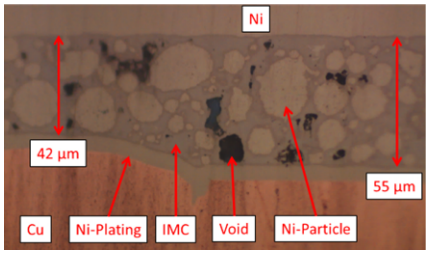
TLPS Research

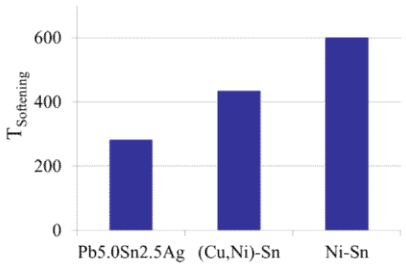
Developed process for creating joints



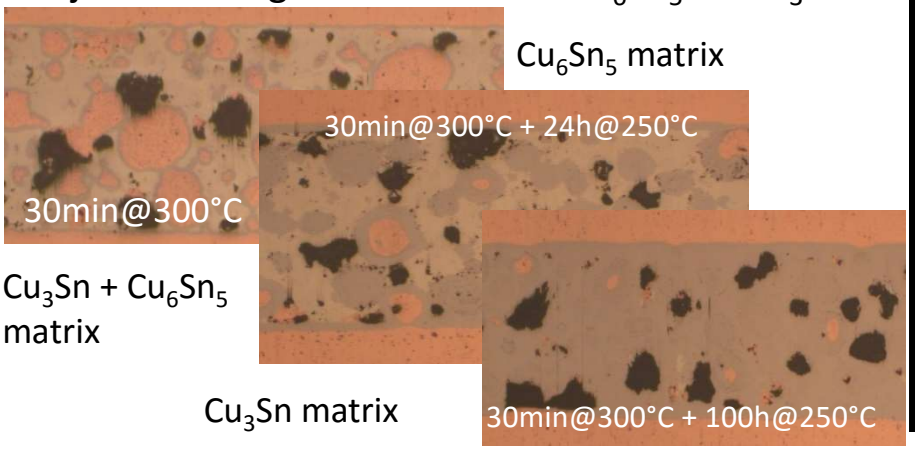
Showed that TLPS joints retain strength > 10 MPa to temperatures > 600°C







Characterized microstructural evolution in joints during use from Cu → Cu_6Sn_5 → Cu_3Sn

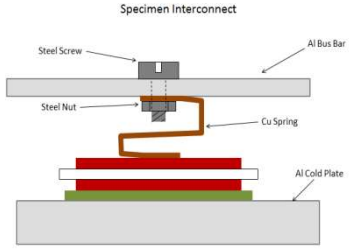


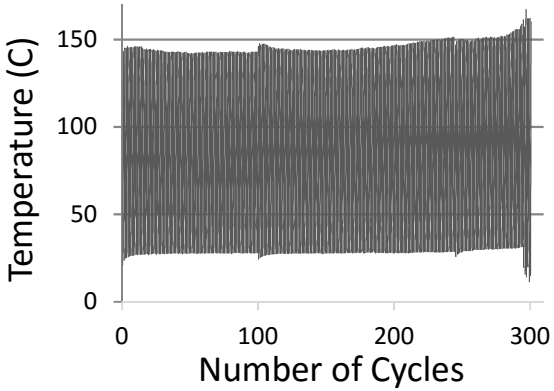
Cu_6Sn_5 matrix

Cu_3Sn + Cu_6Sn_5 matrix

Cu_3Sn matrix

Characterized attach reliability

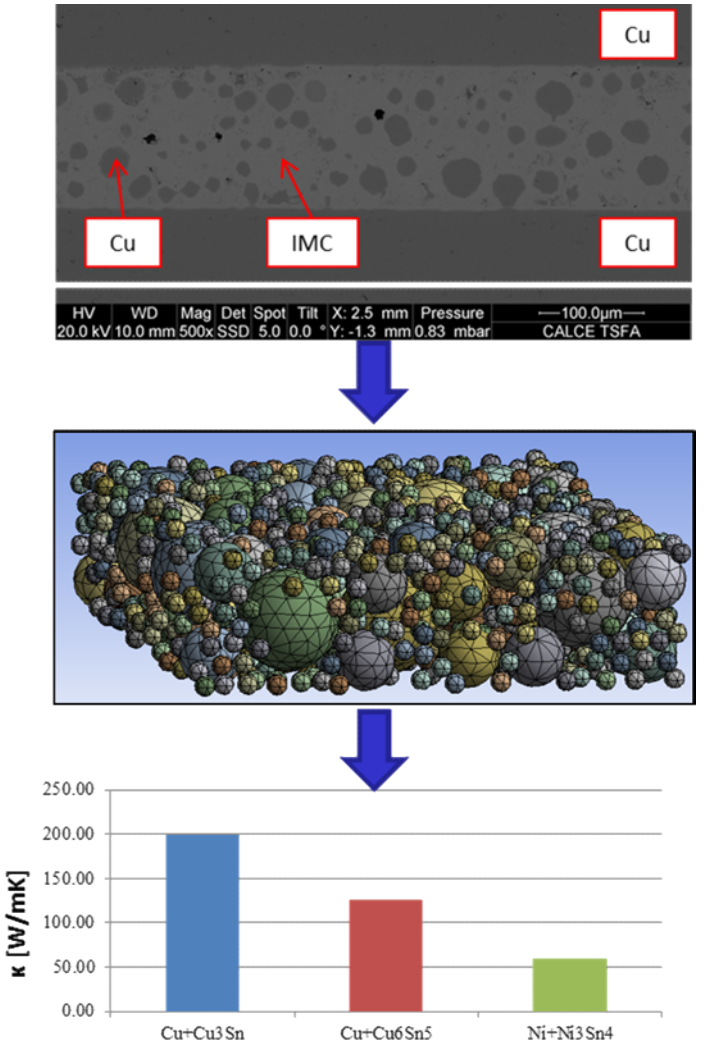




Power Cycling

Simulated Thermal Conductivity
Joint Maximally Filled with 50, 30 and 10 μm Metal Particles

- Joint maximally filled with metal particles with radii of 50, 30, and 10μm.
- Remaining space is filled with intermetallic compounds.
- (Cu_3Sn+Cu), (Cu_6Sn_5+Cu), and (Ni_3Sn_4+Ni) have thermal conductivities of 200 W/mK, 125 W/mK, and 60 W/mK respectively.



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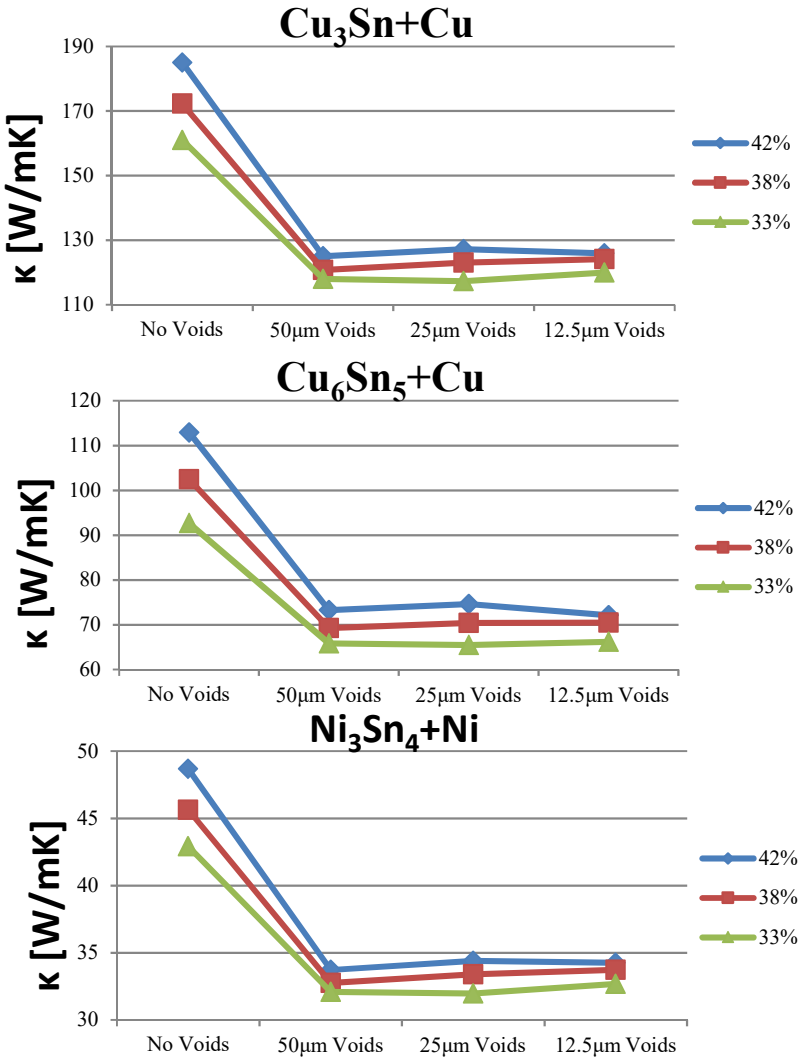
Simulated Thermal Conductivity
Mixed Particle Sizes, Variation of Metal Loading, Partially Voided

- One type of metal particle was replaced with voided regions.
- On average the thermal conductivity of the (Cu_3Sn+Cu), (Cu_6Sn_5+Cu), and (Ni_3Sn_4+Ni) systems were reduced by 29%, 32%, and 27%, respectively.
- The highest reduction for the (Cu_3Sn+Cu) systems is 32 % for the 42% condition with <u>50µm</u> voids.
- For the (Ni_3Sn_4+Ni) system it occurs under the same condition with a reduction of 31%.
- In contrast, for the (Cu_6Sn_5+Cu) system the highest reduction of 36% occurs for the 42% condition with <u>10µm</u> voids



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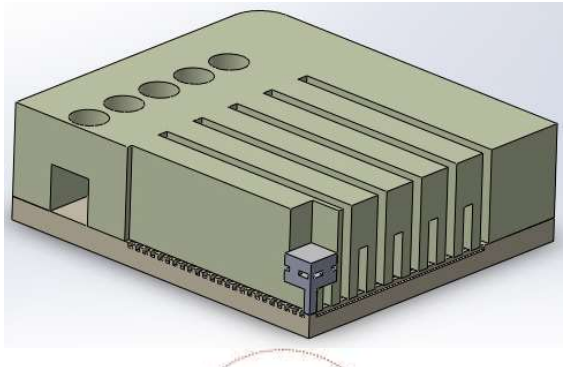
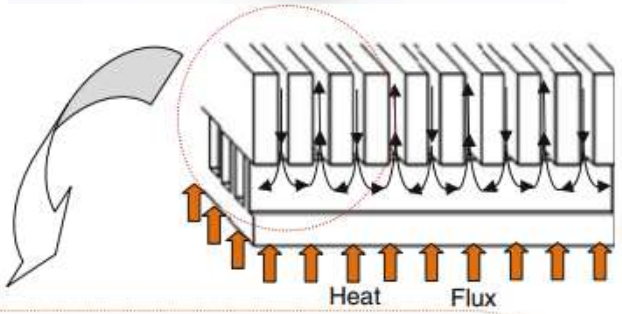
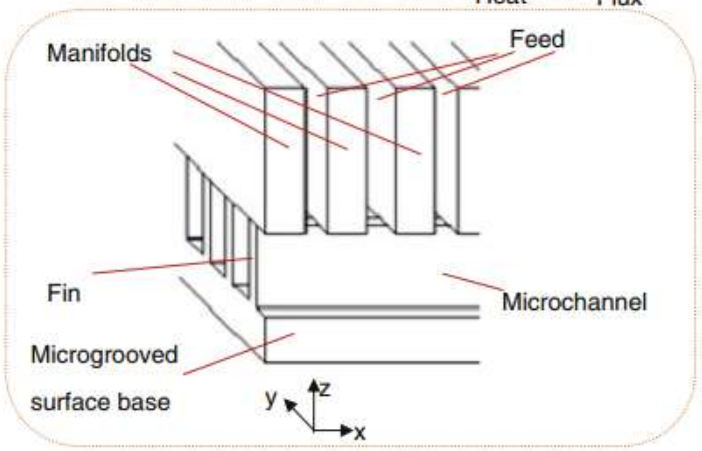
3D Integrated Cooling

- Manifold-Microchannel coolers and Thermoelectric devices can be embedded directly into the substrate or chip to provide localized heat removal at high volumetric rates from the backside of active ICs and power devices.
- Issues include
  - Fluid flow (no dry spots)
  - Heat transfer = f(fin width, fin length, fin pitch)
  - Interconnection
  - Hot spot cooling
  - Reliability
    - Structural Integrity
    - Erosion/Corrosion
    - Clogging

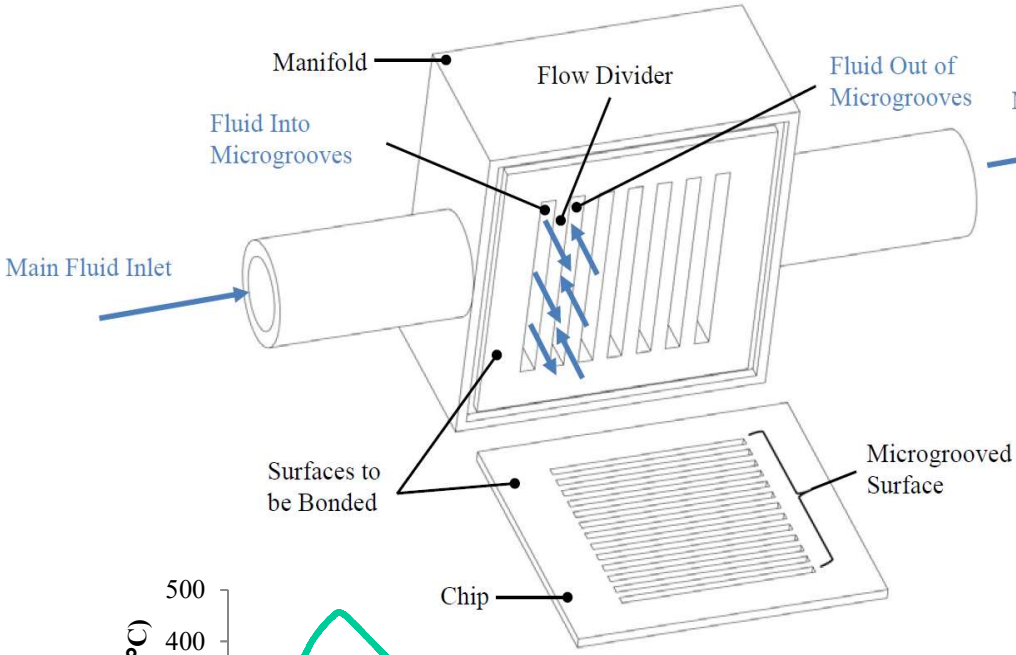


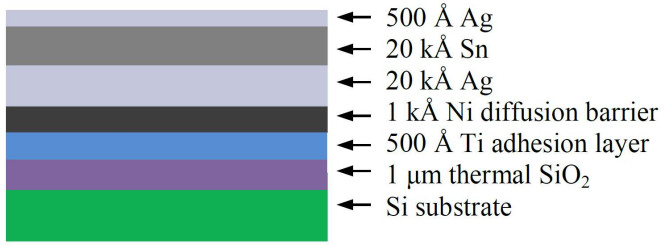


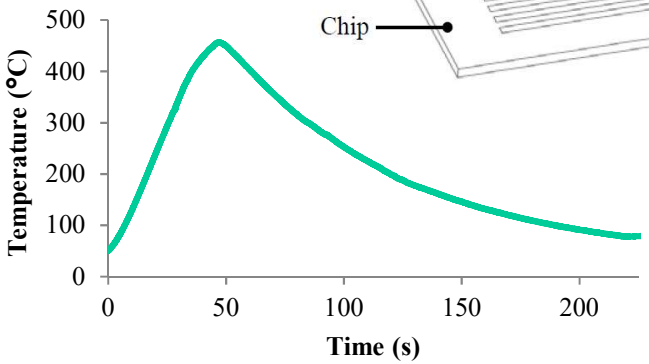


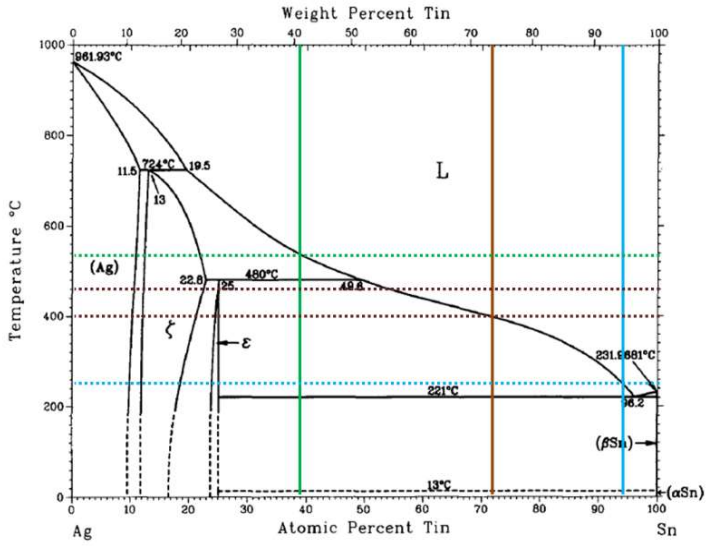
Attaching the Manifold to the Microchannels

Attachment is done by a layered Ag-Sn TLPS Joint deposited on the tops of the fins









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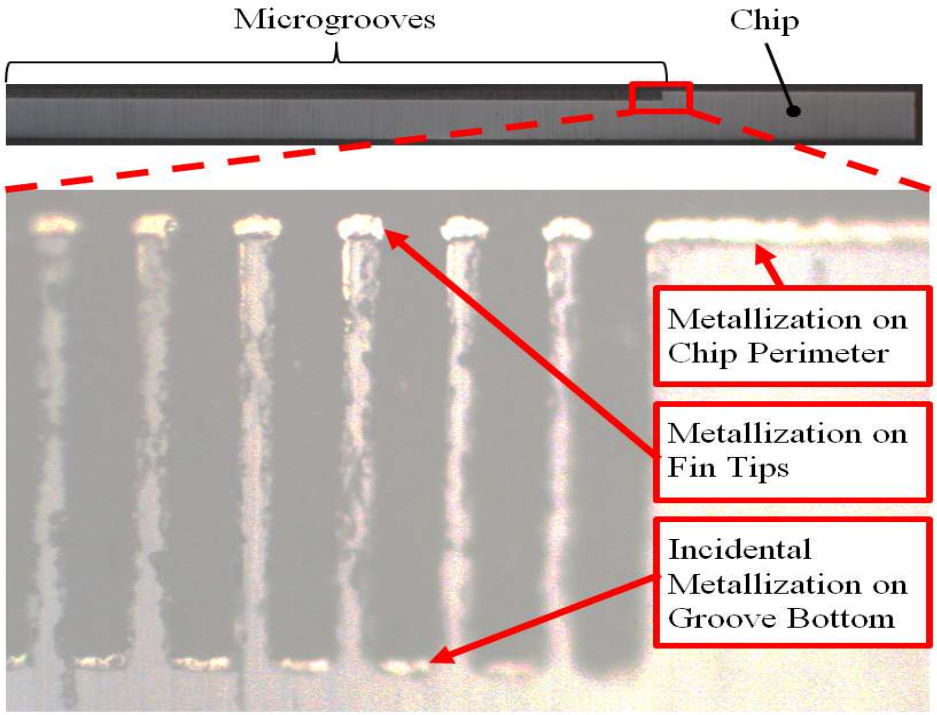
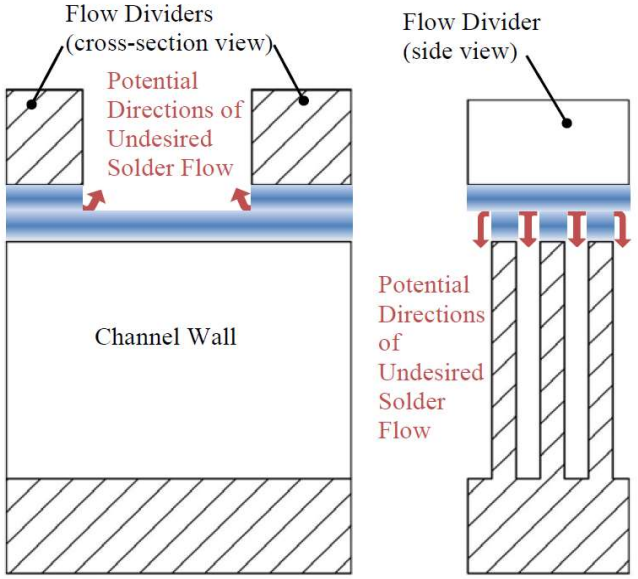
Visualization of the Attach Material

Focusing on placing the joining metallization only on the fin tips. Can see failure occurs at manifold to chip interface on the right.





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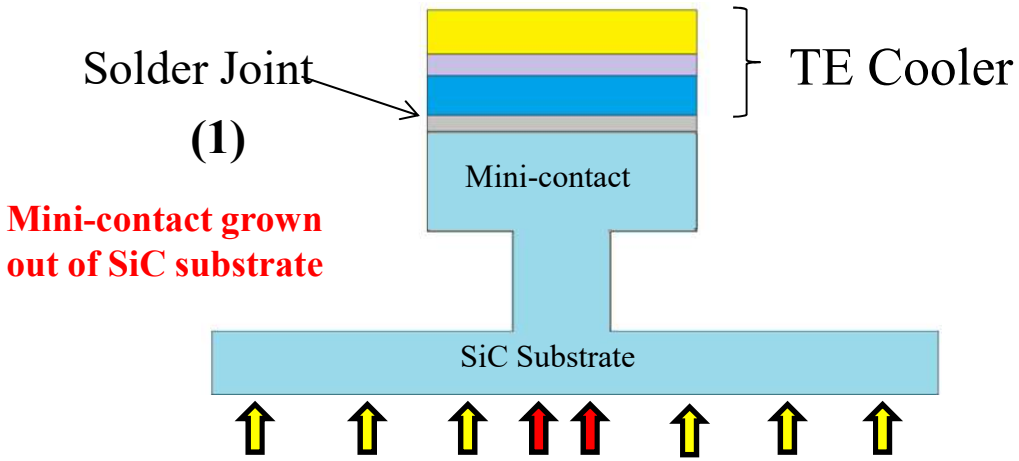
Reliable Integration of Mini-contact

Integrated SiC Mini-contact (1)



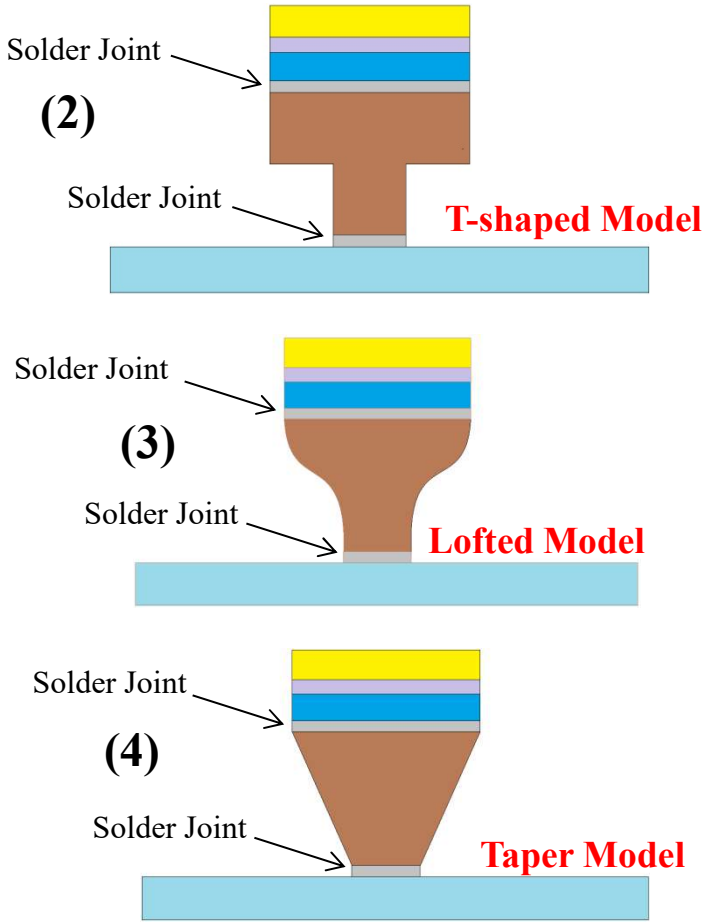
Solder Joint = 20 μm (assumed)

5 – 10 μm = Intermetallic formation

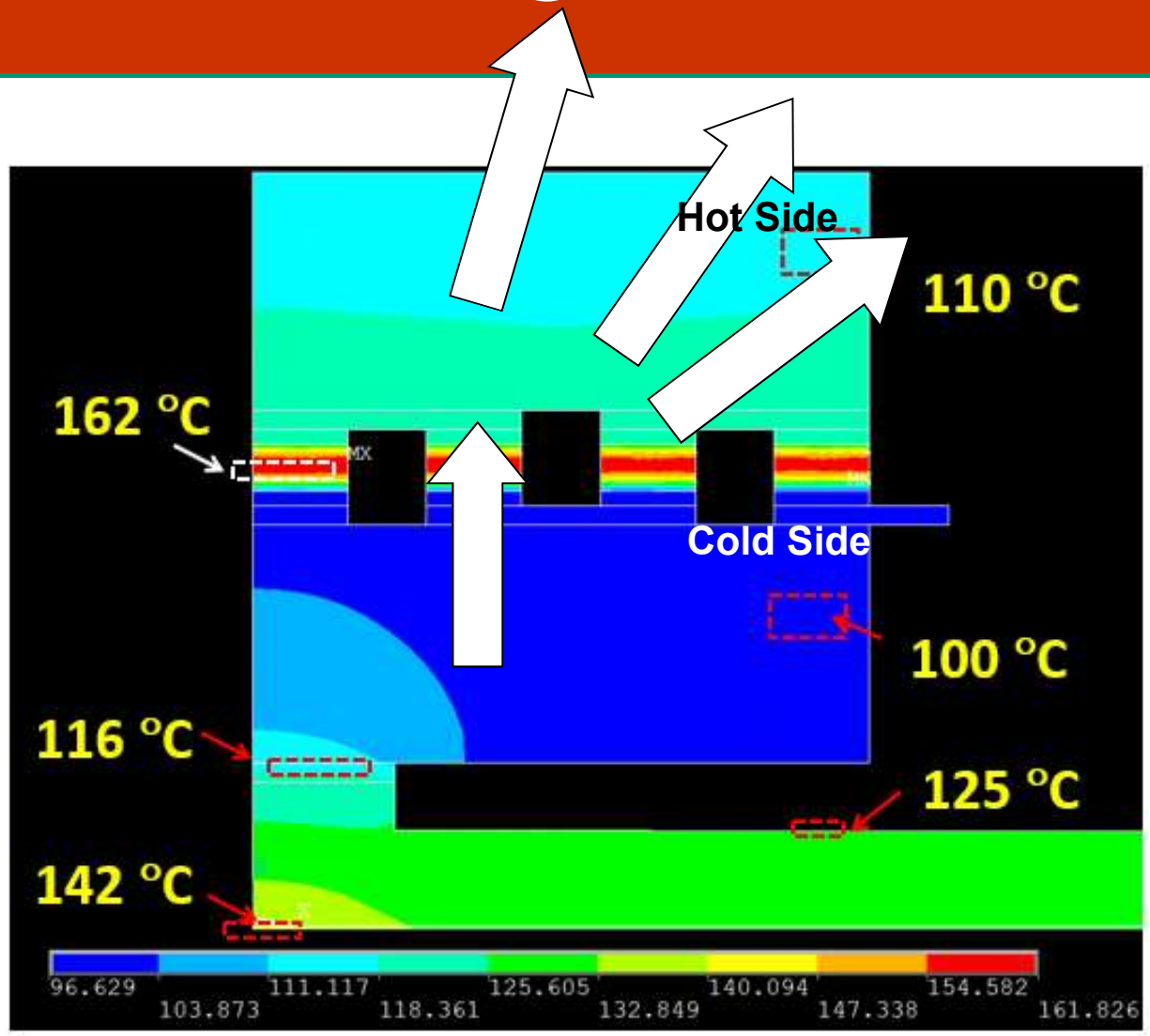
10 – 15 μm = Solder joint

SAC305 good for 100 °C - 150 °C

Discrete Mini-contact: Copper, Diamond



Heat Transfer Through the Thermoelectric



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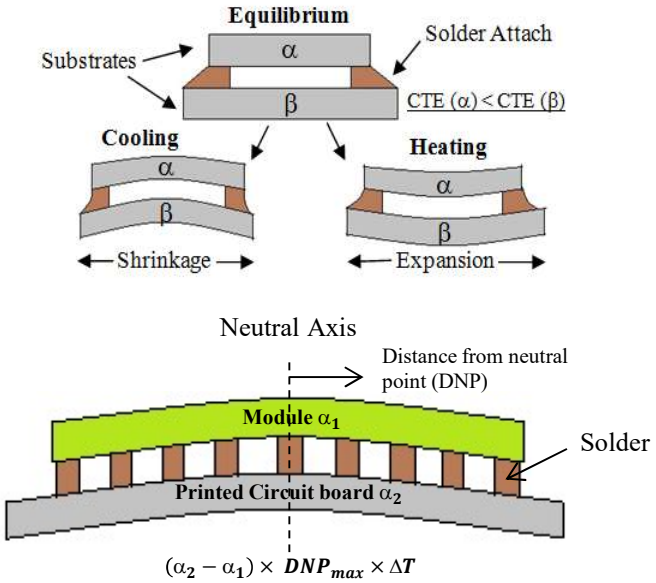
Engelmaier's Failure Model

Lead free solder - CALCE



Local C.T.E. Mismatch
Global C.T.E. Mismatch

$$N_f\,(50\%) = \frac{1}{2}\left[\frac{0.480}{\Delta D}\right]^m$$

$$\frac{1}{m} = c_0 + c_1 \bar{T}_{SJ} + ln\left(1 + \frac{t_0}{t_D}\right)$$

$$\frac{1}{m} = 0.390 + 9.3 * 10^{-4}\,\bar{T}_{SJ} - 1.92 * 10^{-2}\,ln\left(1 + \frac{100}{t_D}\right)$$

ΔD - Plastic strain component

t_D - Dwell time, $\bar{T}_{SJ}$ - Average solder temp.

C_0, C_1, C_2, t_0 - constants (0.39, 9.3e-4, -1.92e-2, 100)

Engelmaier's Failure Model gives good approximation to Solder Joint Reliability

[4] P. Chauhan, M. Osterman, S.W.R. Lee and M. Pecht. "Critical Review of Engelmaier Model for Solder Joint Creep Fatigue Reliability," in Proc. IEEE Transactions on Components and Packaging Technology, Sep. 2009, pp. 693-700
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[6] "Weibull Distribution." Internet: http://reliawiki.org/index.php/The_Weibull_Distribution
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TE Cooler Integration with Mini-contact Solder Joint Reliability (MTTF in Cycles)

Shape	Materials	Solder Dwell Time		
		596 mins.	20 mins.	1 min.
T-shaped	Int. SiC	Avg. Temp.= 71 °C, Pl. Strain= 3e-4		
	MTTF	66,088	165,260	1,181,292
	Copper	Avg.Temp.= 72 °C, Pl. Strain=7.6e-4		
	MTTF	26,079	60,638	369,478
	Diamond	Avg. Temp.=101 °C, Pl. Strain=5e-3		
	MTTF	5,920	11,496	46,295
Lofted	Copper	Avg. Temp. = 61°C, Pl. Strain = 4e-3		
	MTTF	21,187	48,160	278,693
	Diamond	Avg. Temp.= 65 °C, Pl. Strain= 5e-3		
	MTTF	10,281	21,939	110,485
Taper	Copper	Avg. Temp.= 62 °C, Pl. Strain = 4e-3		
	MTTF	23,282	53,194	310,877
	Diamond	Avg. Temp.= 66 °C, Pl. Strain = 5e-3		
	MTTF	10,474	22,369	112,828

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Mini-contact Integration with SiC chip
Solder Joint Reliability (MTTF in Cycles)

Shape	Materials	Solder Dwell Time		
		596 mins.	20 mins.	1 min.
T-shaped	Int. SiC	-	-	-
	Copper	Avg. Temp. = 72 °C, Pl. Strain = 7.6e-4		
	MTTF	662,174	1,905,917	18,045,632
	Diamond	Avg. Temp. = 69 °C, Pl. Strain = 4.9e-3		
	MTTF	11,883	25,502	129,664
Lofted	Copper	Avg. Temp. = 71 °C, Pl. Strain = 7.7e-4		
	MTTF	661,809	1,908,229	18,150,450
	Diamond	Avg. Temp. = 70 °C, Pl. Strain = 4.5e-3		
	MTTF	13,758	29,780	154,058
Taper	Copper	Avg. Temp. = 71 °C, Pl. Strain = 5.8e-4		
	MTTF	1,236,818	3,737,994	39,305,584
	Diamond	Avg. Temp. = 70 °C, Pl. Strain = 4.4e-3		
	MTTF	14,328	31,111	162,016

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Conclusions

- Embedded technology is everywhere and reducing in size
- One important example is heterogeneous integration including anisotropic or differential cooling
- Moving to thermally anisotropic substrate decreases the safe distance between the power dissipating and the temperature sensitive chips by 5 X.
- TLPS joints can be used to seal 3D integrated coolers
- TEC can be added to 3D integrated cooler by using a mini-contact. The best is a SiC minicontact followed by copper discrete and lastly, diamond mini-contact at both chip level and cooler integration level packaging.
- Maximum strain shedding will be achieved for a tapered mini-contact structure.
- Manufacturing of power electronics package with complex contact shapes (lofted and taper), and ability to integrate combined cooling phenomena will be an important factor for consideration in future design.