Challenges to Improving the Accuracy of High Frequency (120MHz) Test Systems

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Integrated Magnetics for Power Supply on Chip

MAGIC
Making Magnetics Disappear into ICs
Summary of presentation

- Why large signal testing?

- Large signal testing methodology - Transformers & Coupled Inductors
  - Measurement circuitry & Equipment
  - Determine current lag
  - Measurement with dc bias - Single & Dual phases

- Validation of test methodology using On-Silicon coupled inductors

- Summary
Why Large Signal testing?

- Integrated magnetic components including inductors, transformer are of increased interest for realising Power Supply on Chip/in Package modules.
- Research focus has been restricted to design and manufacturing of these components.
- Researchers traditionally focus on small signal testing techniques include VNAs & Impedance Analysers for measuring performance of inductors.
- These techniques can only provide limited information on the device performance.
- Need to apply large signals to accurately measure the performance of devices, magnetic materials.
- Further, this information is necessary to develop an accurate loss model for magnetic materials & copper.

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Magnetic Core losses

- Magnetic core losses can be broadly classified

**Hysteresis Loss**
- Impede domain wall motion
- Loss manifests as Coercive field

**Eddy Current Loss**
- Eddy current resist change in applied magnetic field
- Skin depth, thickness at which the current density drops to $1/e$
- Eddy current loss depends on conductivity & permeability of material
- Eddy current loss (thickness less than one skin depth)

**Anomalous Loss**
- Inconsistencies in domain wall motion during magnetization reversal
- Variations in localized flux densities
- Model for estimating anomalous loss proposed by Bertotti (Book - Hysteresis in Magnetism)

\[ P_{excess} = 8 \sqrt{d_w} \sqrt{\frac{G_V}{\rho}} (B \cdot f)^{\frac{3}{2}} \]

- Small Signal test

\[ P_h = 4 \cdot f \cdot B_{ac}^2 \cdot \frac{H_c}{B_{sat}} \]

\[ P_e = \frac{\omega^2 B_{sat}^2 \sigma a^2}{24} \]
Electroplated Ni$_{45}$Fe$_{55}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturation, $B_{sat}$</td>
<td>1.6 T</td>
</tr>
<tr>
<td>Coercivity, $H_c$</td>
<td>80 A/m</td>
</tr>
<tr>
<td>Resistivity, $\rho$</td>
<td>45 $\mu\Omega$ cm</td>
</tr>
<tr>
<td>Anisotropy, $H_k$</td>
<td>800 A/m</td>
</tr>
</tbody>
</table>

Test conditions - Frequency - 100 kHz; Bacpeak - 100 mT; thickness - 3 $\mu$m

- Classical eddy current loss = 32.4 kW/m$^3$; 1.1% of total loss, measured by small signal testing
- Hysteresis loss = 1333 kW/m$^3$; 45% of total loss
- Anomalous loss = 1624 kW/m$^3$; 53.9% of total loss

Test prototype

![Ni$_{45}$Fe$_{55}$ - 1 $\mu$m thick](image)
Large signal test circuit & set-up

Test Circuit

Test Circuit on PCB

Measurement set-up
Generation of the excitation (ac)

- **ac signal**
  - A 50 Ω output resistance RF-amplifier model 25A250A from Applied Research
  - Controlled by a signal generator model Agilent E8257D
  - SMA connector
  - Series-connected to a decoupling bank capacitor composed of 2 SMD 100nF/25V devices
dc signal

- Two DENMA T2-10480 dc power supplies
- Series-connected to an inductance SMD 1812 3.3 µH from Wurth Elektronics
- Series-connected to a 10 Ω power resistor to limit the total current
Sources of Error in the measurement circuit

» Noise
  » Proper routing of the board: ground plane, small loops
  » 4-wire measurement
  » Minimize loops for the connectors of the probes

» Error in amplitude
  » Low tolerance components are used
  » Impedance measured directly from the voltage and current waveforms, so the main source of error are the probes → compensation of the attenuation of the Pearson 2877 current monitors

» Delay between the signals
  » Voltage and current probes have their own characteristic propagation delay → compensation of the time-skew
Compensation test for current probe delay

To compensate the attenuation and delay of the probes, an additional test was performed.

The voltage across and the current through a capacitor were measured in order to estimate these parameters.

\[ |Z| = \sqrt{R^2 + \left(\frac{1}{2\pi f_{test} C}\right)^2} \]

\[ |Z| = \text{Att} \frac{|V_1|}{|I_1|} \]

\[ \text{Att} = \frac{|I_1| \sqrt{R^2 + \left(\frac{1}{2\pi f_{test} C}\right)^2}}{|V_1|} \]

\[ \angle Z = \angle V_1 - (\angle I_1 + \angle \text{delay}) \]

\[ \angle \text{delay} = \angle V_1 - \angle I_1 - \tan^{-1} \left( \frac{1}{2\pi f_{test} C R} \right) \]
A first test was carried out:
- SMA connector for the voltage probe
- 4-wire measurement
- Ground plane

New test using lower impedance probes:
- New connectors for the new probes
- Minimum current loop of the voltage probes
- No ground plane

### Comparison of voltage probes

<table>
<thead>
<tr>
<th>Voltage probe</th>
<th>Frequency (MHz)</th>
<th>Idc (A)</th>
<th>Iac (mA)</th>
<th>Magnetizing inductance (nH)</th>
<th>Core resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>11 pF</td>
<td>40</td>
<td>0</td>
<td>24</td>
<td>14.64</td>
<td>1223</td>
</tr>
<tr>
<td>1 pF</td>
<td>40</td>
<td>0</td>
<td>20</td>
<td>14.96</td>
<td>609</td>
</tr>
<tr>
<td>11 pF</td>
<td>80</td>
<td>0</td>
<td>25</td>
<td>16.72</td>
<td>987</td>
</tr>
<tr>
<td>1 pF</td>
<td>80</td>
<td>0</td>
<td>50</td>
<td>16.63</td>
<td>1171</td>
</tr>
</tbody>
</table>

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The current monitor is only suitable for ac current and saturates at moderate values of dc bias.

To avoid this saturation, the dc current has been compensated.
Validation using on-Si coupled inductor

- Two coupled equal coils
  - Self-inductance 47 nH
  - Coupling factor 0.4

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core thickness</td>
<td>1.6 µm</td>
</tr>
<tr>
<td>Core length</td>
<td>1.78 mm</td>
</tr>
<tr>
<td>Copper width</td>
<td>50.62 µm</td>
</tr>
<tr>
<td>Copper thickness</td>
<td>15 µm</td>
</tr>
<tr>
<td>DCR</td>
<td>0.3425 Ω</td>
</tr>
<tr>
<td>Device footprint</td>
<td>2 mm²</td>
</tr>
</tbody>
</table>

L11 - Total inductance of one phase
L12 - Core inductance
R11 - Total resistance of one phase
R12 - Core resistance

Small signal test*

*Small signal bias test

Ampere lab

I_{sat} = 650 mA
- This measurement is consistent with the small-signal measurements
- Core losses increase with the square of frequency (as Eddy currents)
- Consistent with theory for single lamination NiFe core (low anomalous, hysteresis losses)
Dual dc, single ac test

Test conditions:
- Frequency: 100 MHz, 120 MHz
- AC current peak: 100 mA
- DC current: 0-1.5 A

![Diagram of circuit with labels: i_{ac1}, I_{dc1}, v_{ac1}, V_{dc1}, i_1, v_2, I_{dc2}]

![Graph showing L1, L2 vs. dc current (A) and BH curves based on 1st harmonic calculations. L12-120MHz, L11-120MHz, L12-100MHz, L11-100MHz, 100MHz, 100mA AC pk]
Dual dc, single ac test

Test conditions:
- Frequency: 100 MHz, 120 MHz
- AC current peak: 100 mA
- DC current: 0 - 1.5 A
• Large signal measurement critical to minimizing the development cycle
• Provide accurate loss information for the inductor before a full circuit test
• PCB design and tool set-up critical for precise measurement
• Highlighted the challenges with measurement errors at high frequencies
• Explained the tooling, equipment required for improved precision
• Demonstrated the workings of the test set-up using on-silicon coupled inductors
Lab Ampere, INSA, Lyon - Florian Neveu, Dr. Christian Martin, Prof. Bruno Allard

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