

Part 2.

# Hysteresis Loss Model

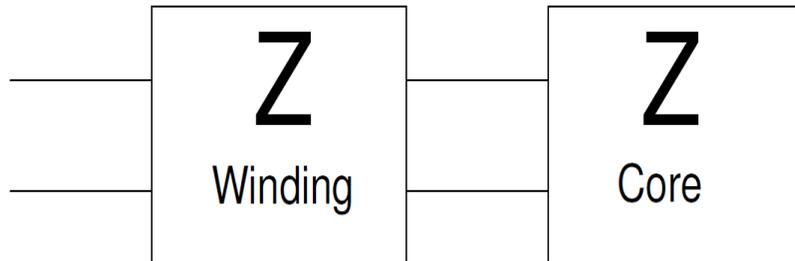
Edward Herbert

# Core loss modeling

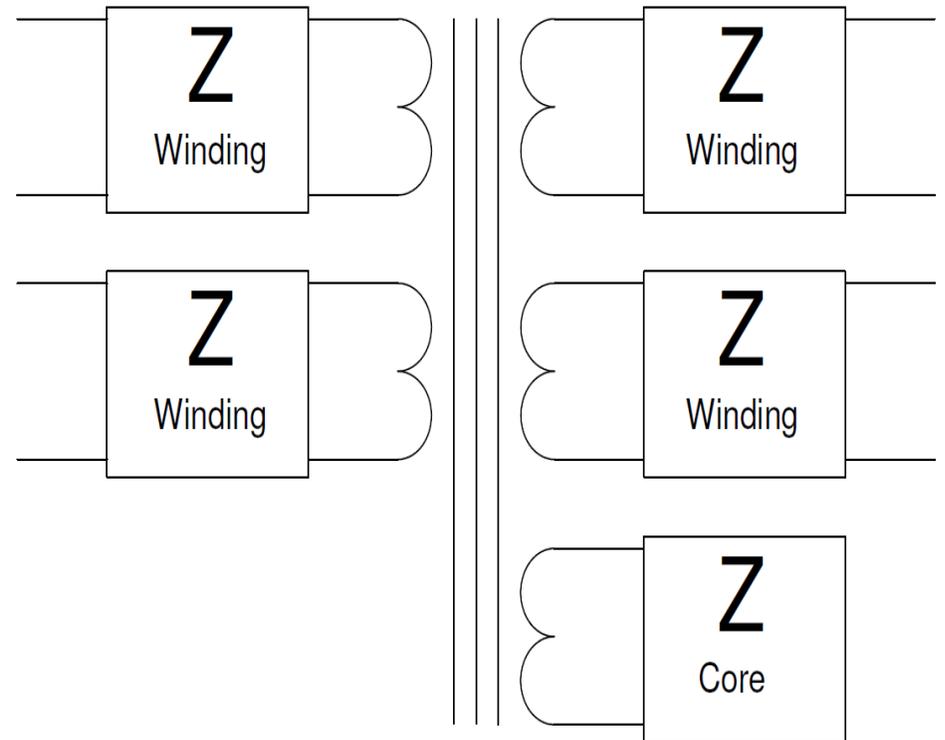
We will explore whether core loss and reactance can be modeled as an impedance. If they can,



an inductor can be modeled as series impedances,  $Z_w$  and  $Z_c$ .

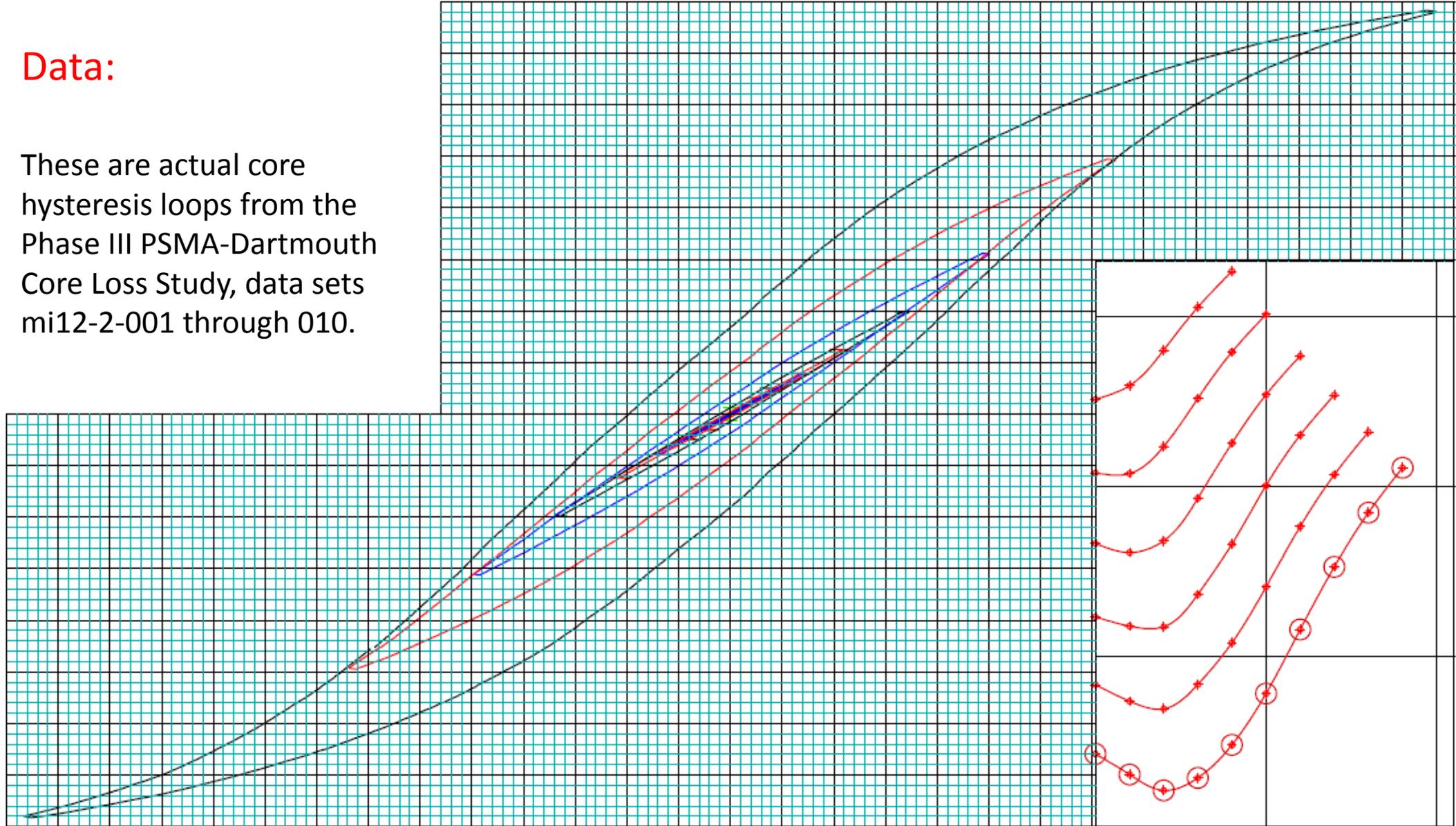


Also,  
a transformer can be modeled as an ideal transformer with an extra single turn winding for the core loss.



## Data:

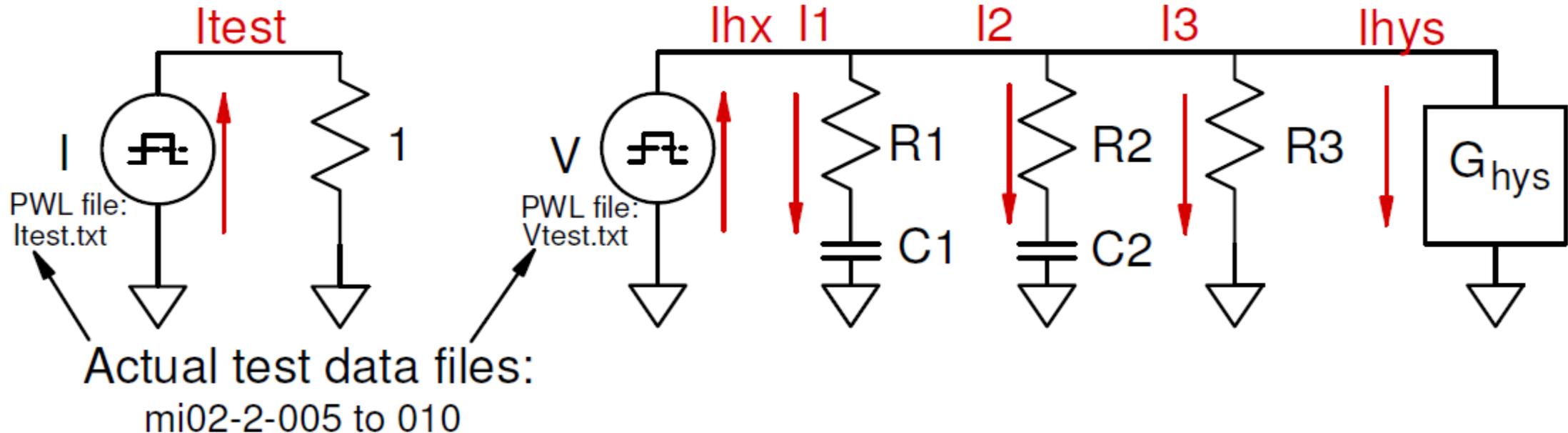
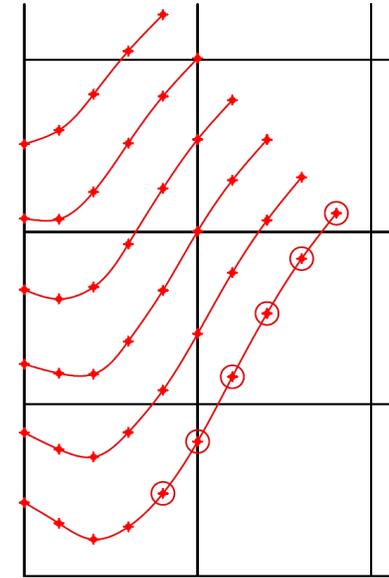
These are actual core hysteresis loops from the Phase III PSMA-Dartmouth Core Loss Study, data sets mi12-2-001 through 010.



# Synthesizing the hysteresis admittance model, $G_{hys}$

The admittance model,  $G_{hys}$ , takes the place of the inductor  $L$  in the previous model. The other components are the same.

The algorithm for  $G_{hys}$  is populated with 207 points from the actual data from six data sets, mi12-2-005 to 010, as indicated by the circles on the small graph. In this way, good accuracy is assured. Doubtless, more samples would improve the algorithm.



# SPICE criteria

The model is LTspice

Once the model is established, it is **NOT** modified for different runs, **except** the initial condition of inductor (current at  $t=0$ ) is set and also the initial flux (v-s at  $t=0$ ). In some cases, the initial condition of capacitors (voltage at  $t=0$ ) is set.

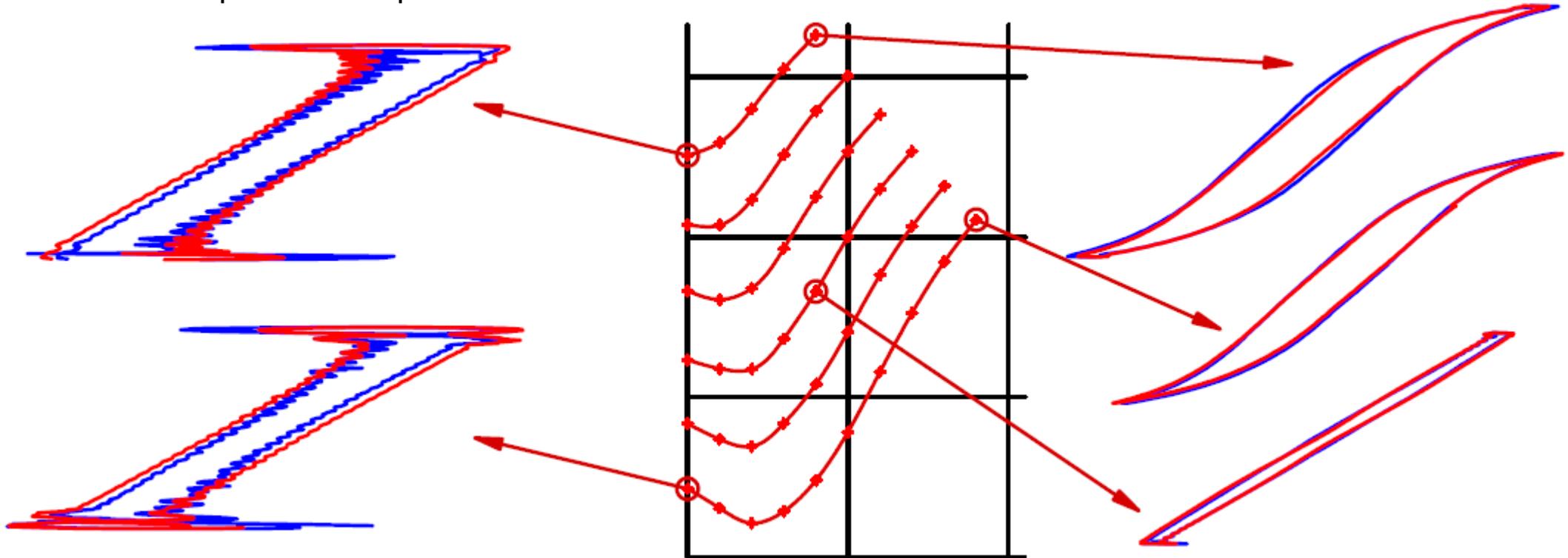
There are **no** changes to component values or the algorithm between runs.

No component nor the algorithm has a voltage coefficient. This was unexpected.

A voltage dependence for the components or the algorithm would be permissible, as voltage can be determined instantaneously and applied to a coefficient, as long as the coefficient factor is not changed from run to run. This may be a desirable future refinement.

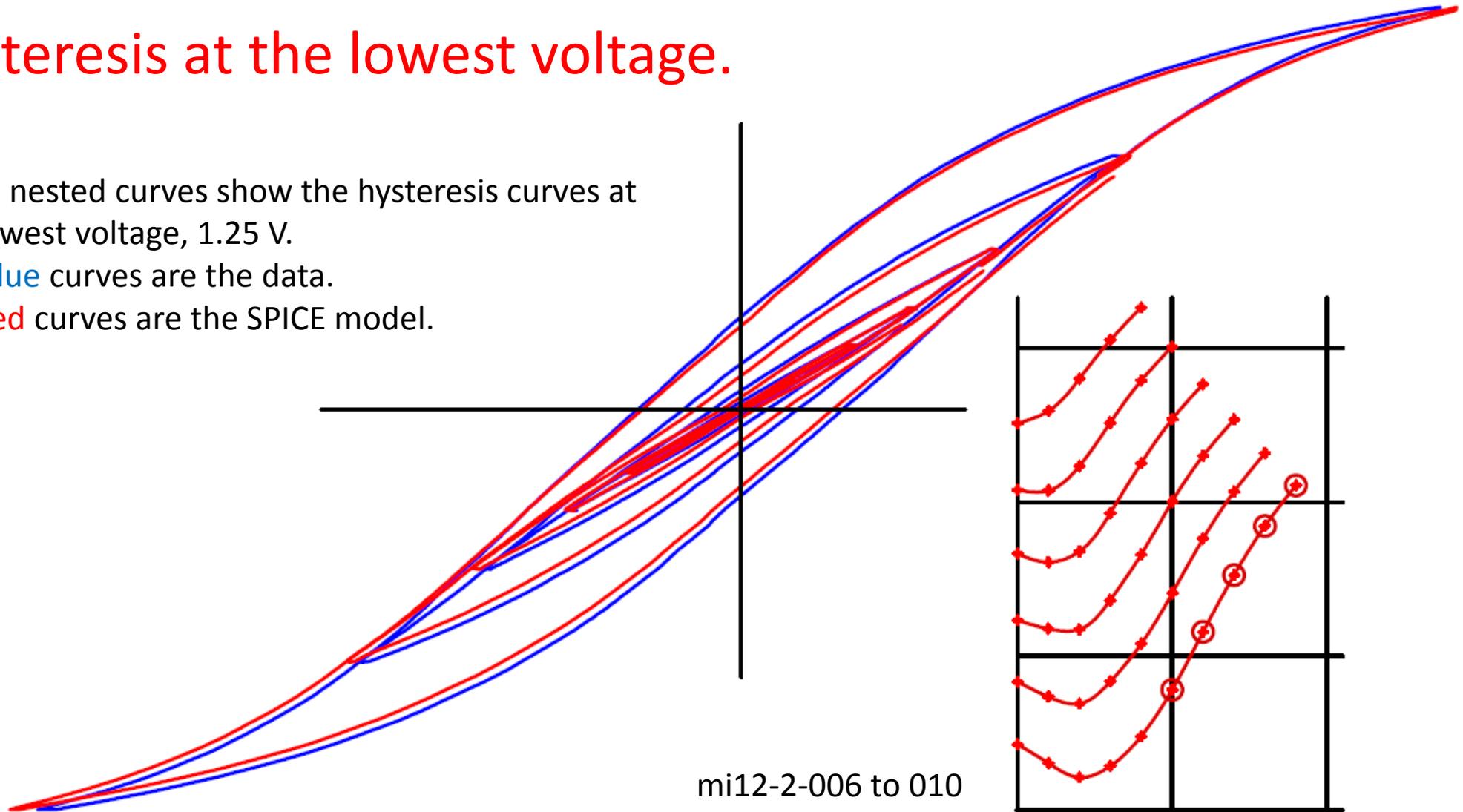
# The fit is good over the entire range of data

The blue curves are the data from the PSMA-Dartmouth Core Loss Studies.  
The red curves are the SPICE model results when applying the voltage from the data.  
The scales vary widely in the different curves, but the aspect ratio is fixed.  
It is the shape that is important.



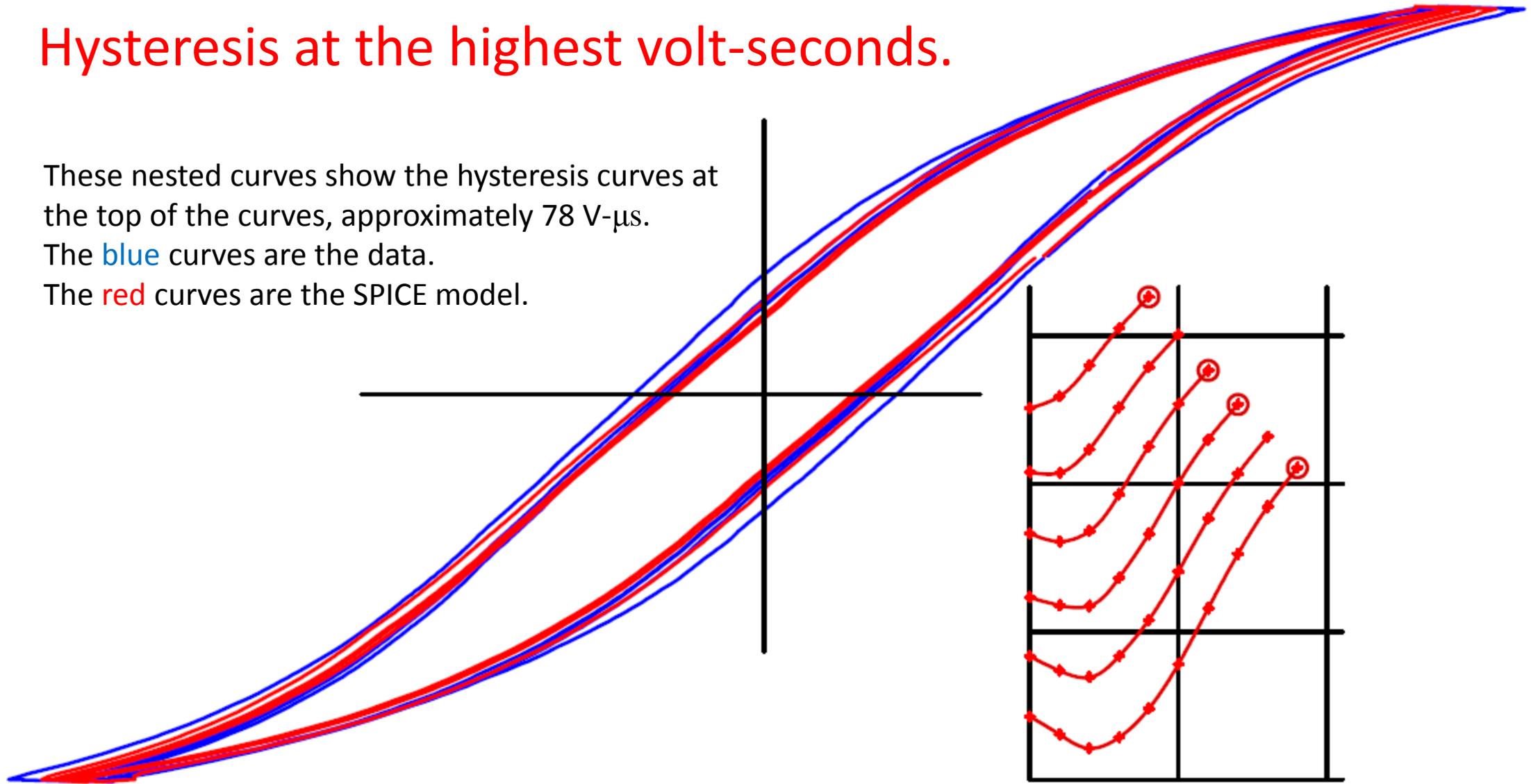
# Hysteresis at the lowest voltage.

These nested curves show the hysteresis curves at the lowest voltage, 1.25 V.  
The blue curves are the data.  
The red curves are the SPICE model.



# Hysteresis at the highest volt-seconds.

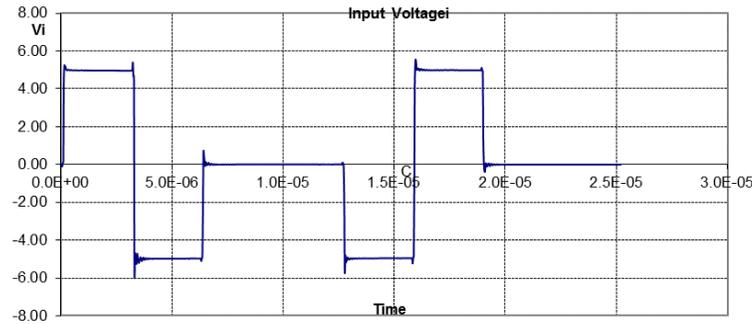
These nested curves show the hysteresis curves at the top of the curves, approximately 78 V- $\mu$ s.  
The blue curves are the data.  
The red curves are the SPICE model.



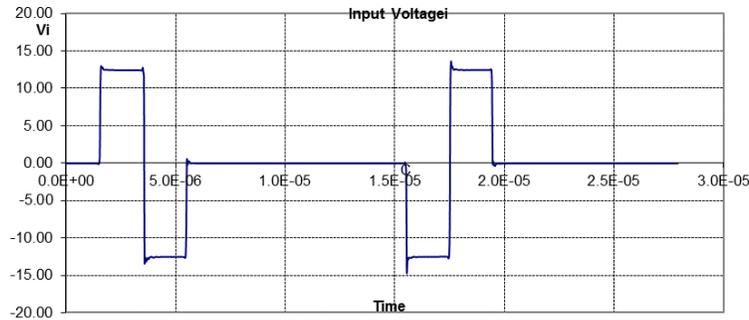
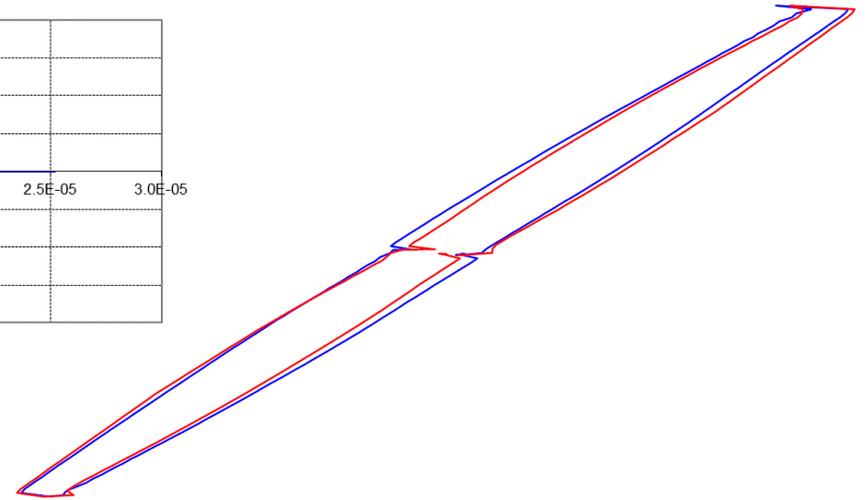
# Other wave forms

The SPICE model fits the data fairly well for the “Hippo” waveform.

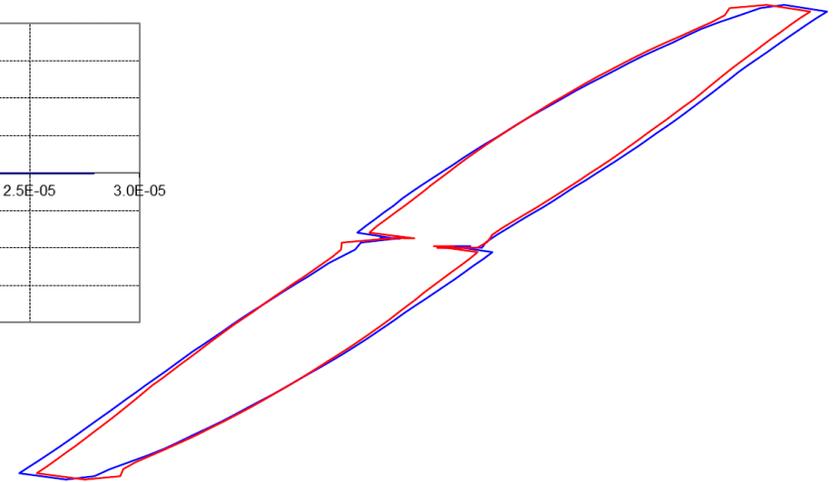
Note the tuck in the hysteresis curve near zero.



mi12-2-132



mi12-2-150

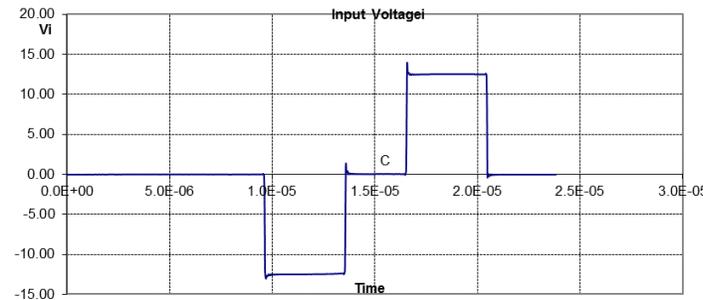


## “Skewed” wave form (DC bias)

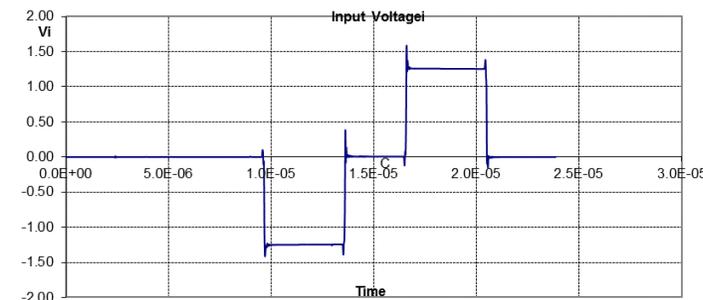
No data from the PSMA-Dartmouth core loss study purposefully introduced a dc bias.

However, because a dc blocking capacitor was used, there was a dc bias in the “Skewed” wave form, where the off-times are unequal. The capacitor forces equal amp-seconds (coulombs) as well as equal volt-seconds, so the operating point moved accordingly.

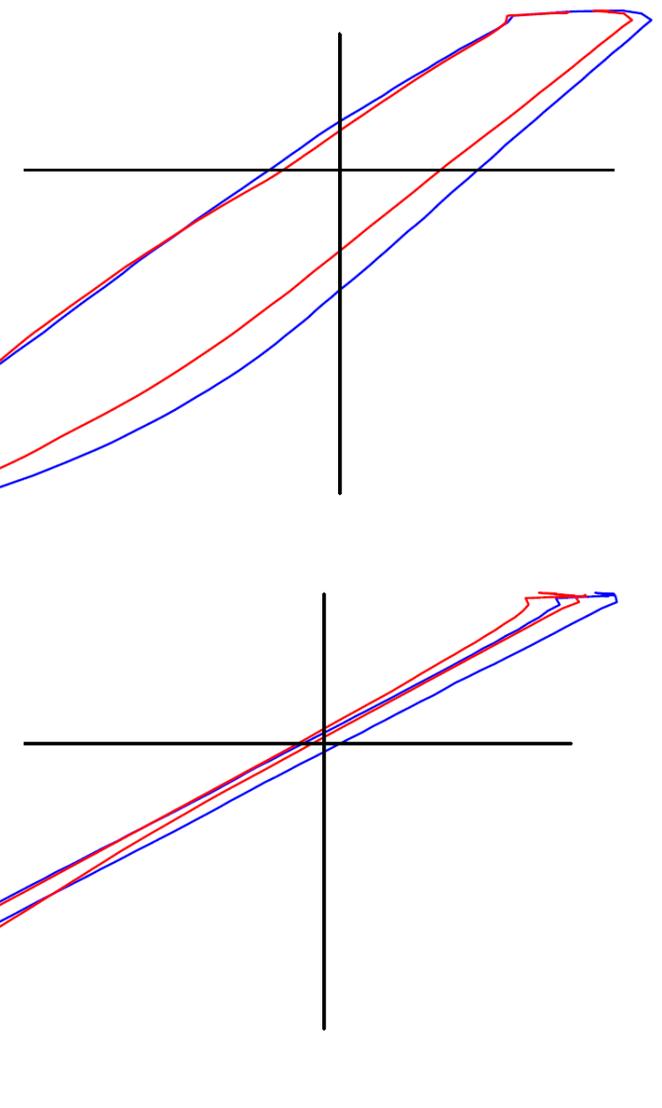
Although it was not planned, it looks as if the SPICE model may accommodate dc bias. More data points are needed.



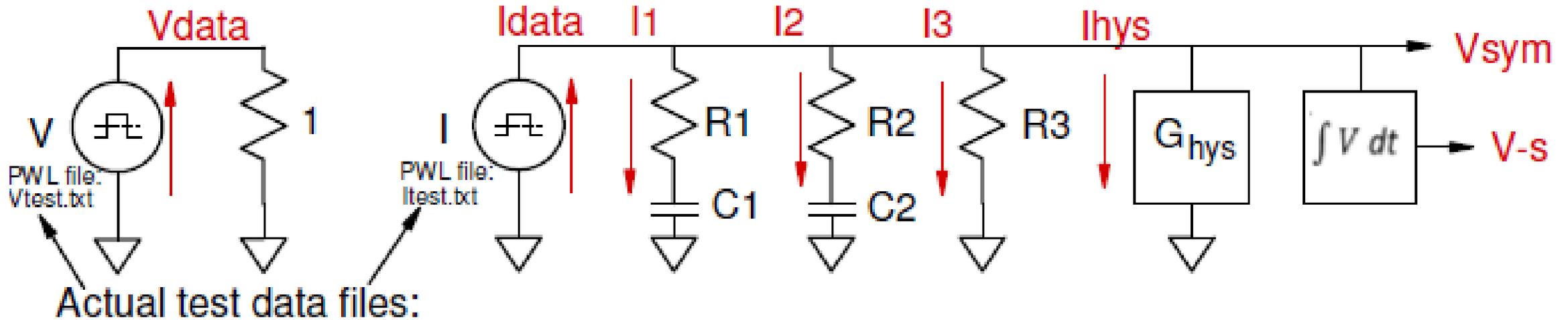
mi12-2-060



mi12-2-050



# Current-driven simulation



Because the core is modeled as an admittance, it can be driven by a current.

The voltage drop across the core model is the simulated voltage,  $V_{sym}$ , and it can be integrated to give a simulated  $V-s$  as the Y-axis of the hysteresis curves. The X-axis is the driving current.

There are no data that are current driven, so the hysteresis loops following are superimposed on the voltage driven hysteresis loop for the same conditions of voltage, current and time.

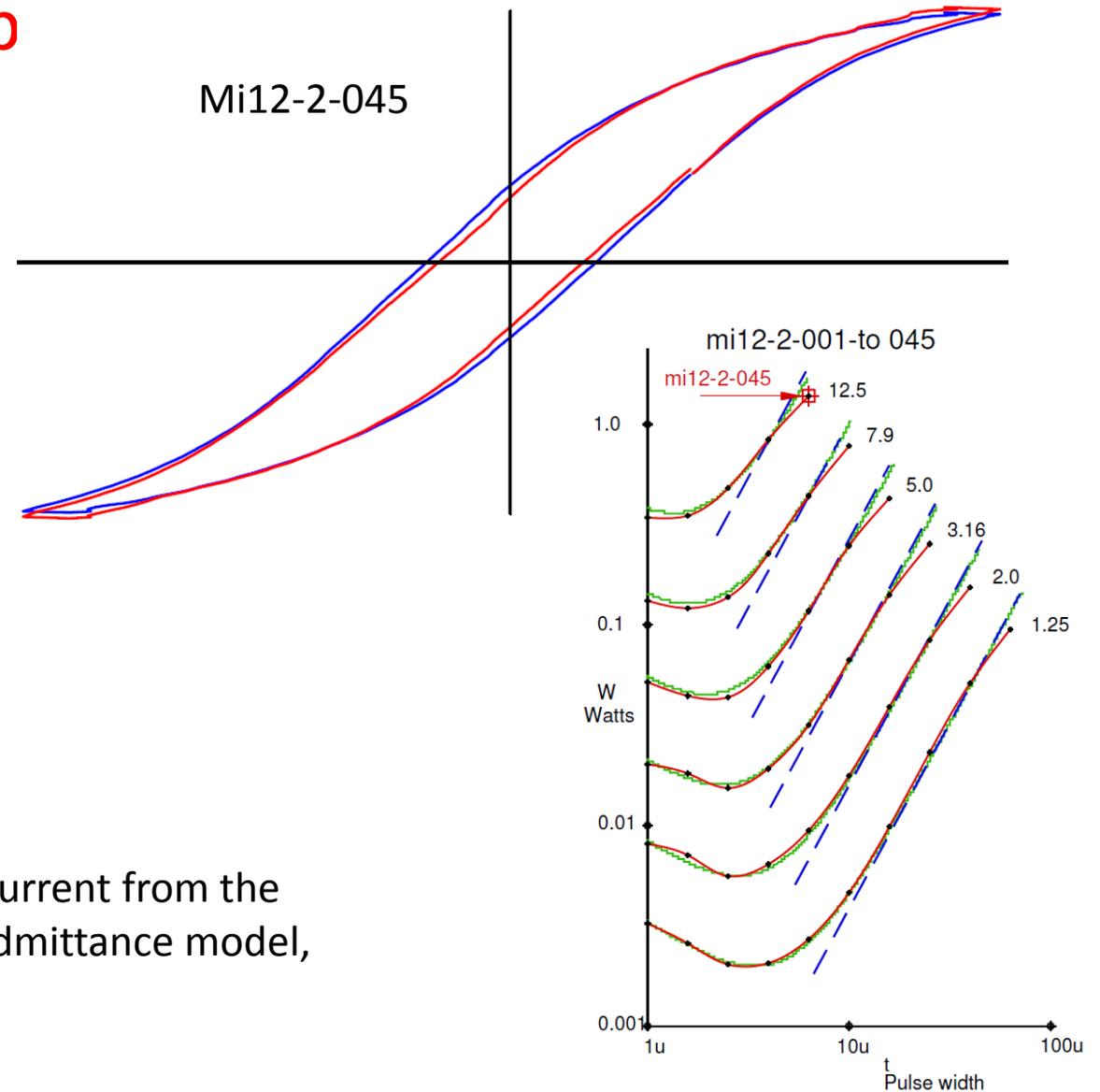
# Current driven hysteresis loop

There are no current driven data from the PSMA-Dartmouth core loss studies.

For these tests, the measured current data was fed into a current source in the LTspice model as a PWL text file, and it was applied to the admittance model. The resulting voltage was then integrated to produce volt-seconds, V-s, for the Y-axis for the model, the **red** curves.

The **blue** curves are the corresponding voltage driven hysteresis loop from the data.

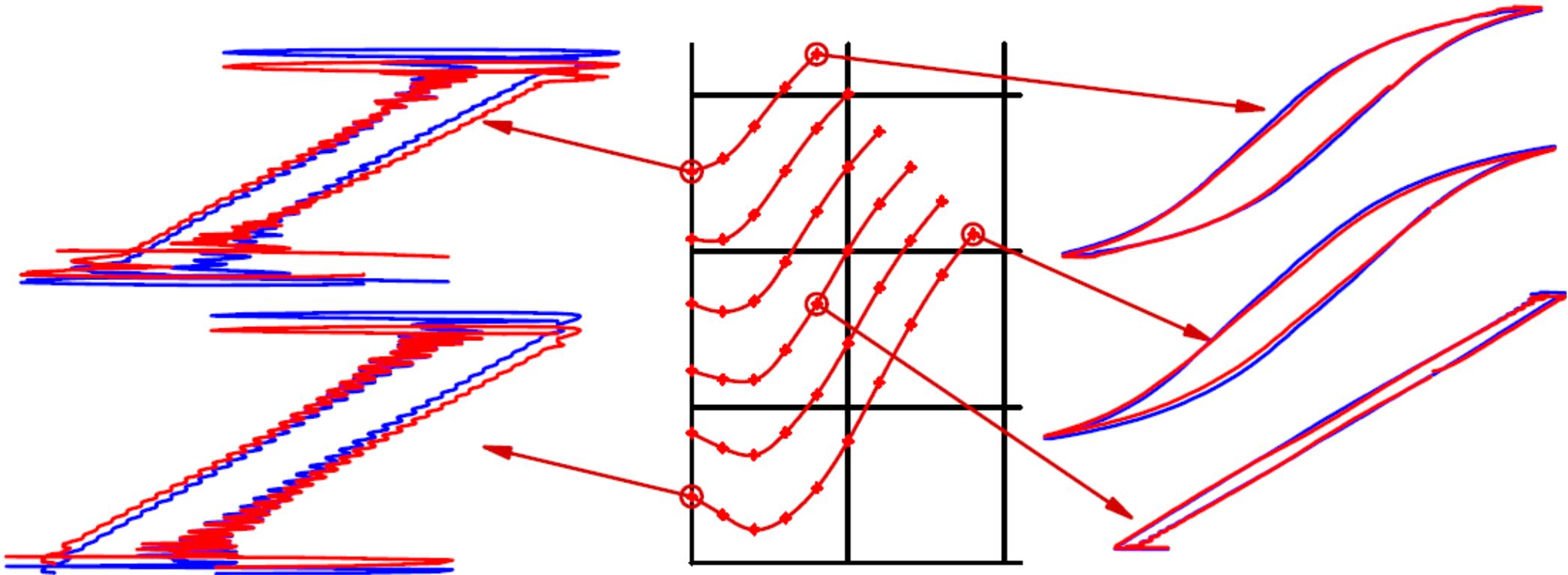
The x-axis is the current. Because the measured current from the voltage driven data is the applied current to the admittance model, the X parameters are the same for both curves.



# Current driven admittance model

## Hysteresis loops

The curve fit is reasonably good over the range of available data.  
The scale varies a lot, but the aspect ratio is fixed.



Thank you.

Questions?

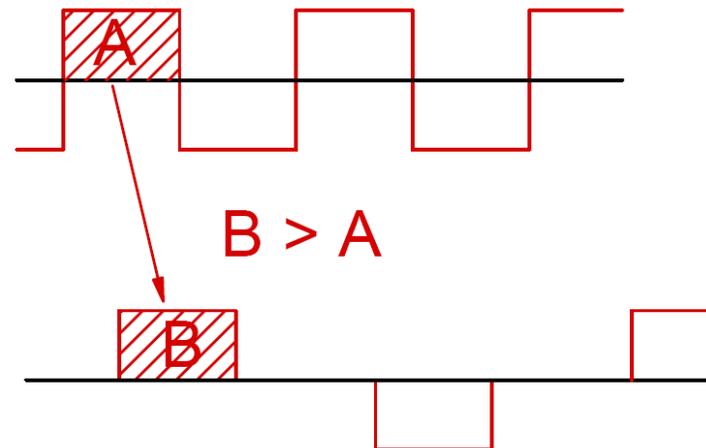
# Addendum

There will not be time to present these slides at the workshop.

However, the information may interest those who preview the slides before the workshop, or who review the slides in the archive.

## Off-time phenomenon

In Phase I of the PSMA-Dartmouth core loss studies, it was discovered that the loss per cycle increased under some circumstances if off-time was inserted into the excitation wave-form.

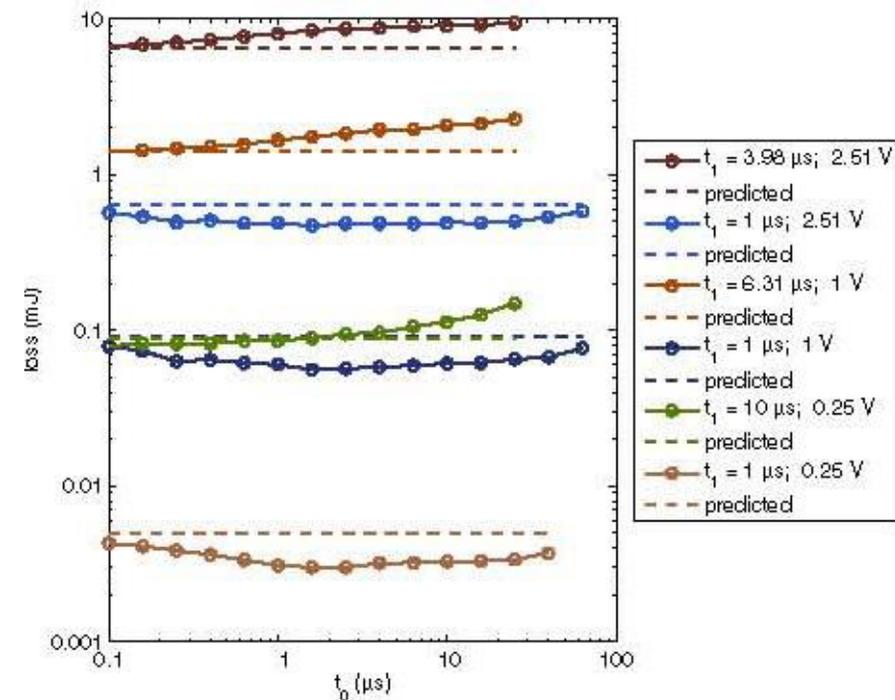


# Off-time phenomenon

Core Loss Project,  
Phase I, Dartmouth

## Anomalous result:

In the ferrite core, losses per cycle increase significantly if off-time is added between the pulses of a square-wave. The loss increases with longer off-time.



(a) Varying period

# Off-time phenomenon on Herbert curve

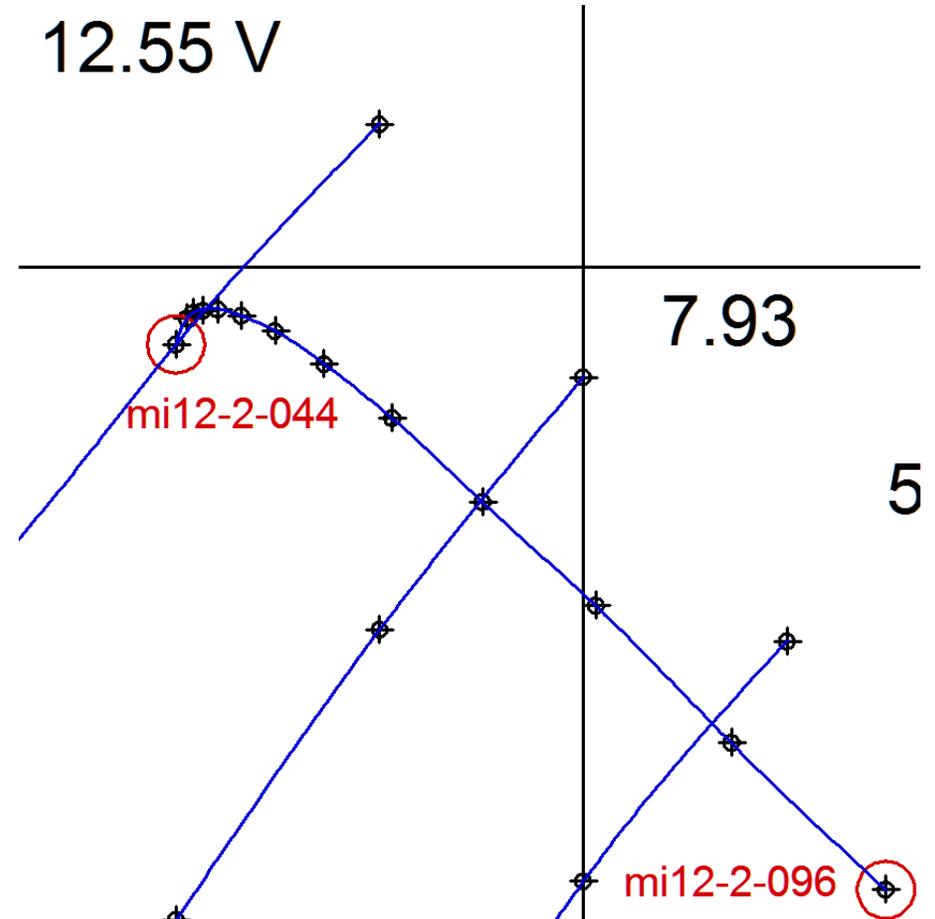
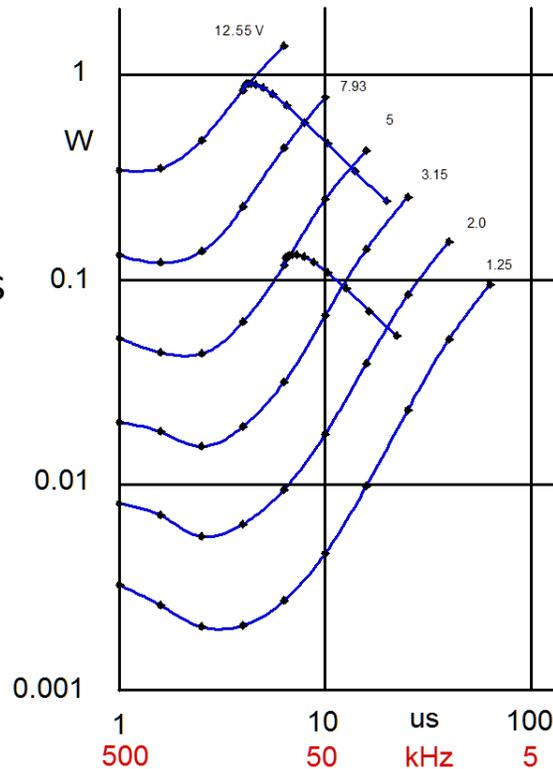
To determine reduced duty-ratio losses on the Herbert curve, find the square-wave with the same excitation and pulse width.

On the X-axis, find the pulse width including the off-time (one half of the period).

Move up to the low duty-ratio curve, then across to find the power in watts.

For this core and winding, the core loss increases initially before decreasing with lower duty-ratio.

The energy loss per cycle is increasing asymptotically.



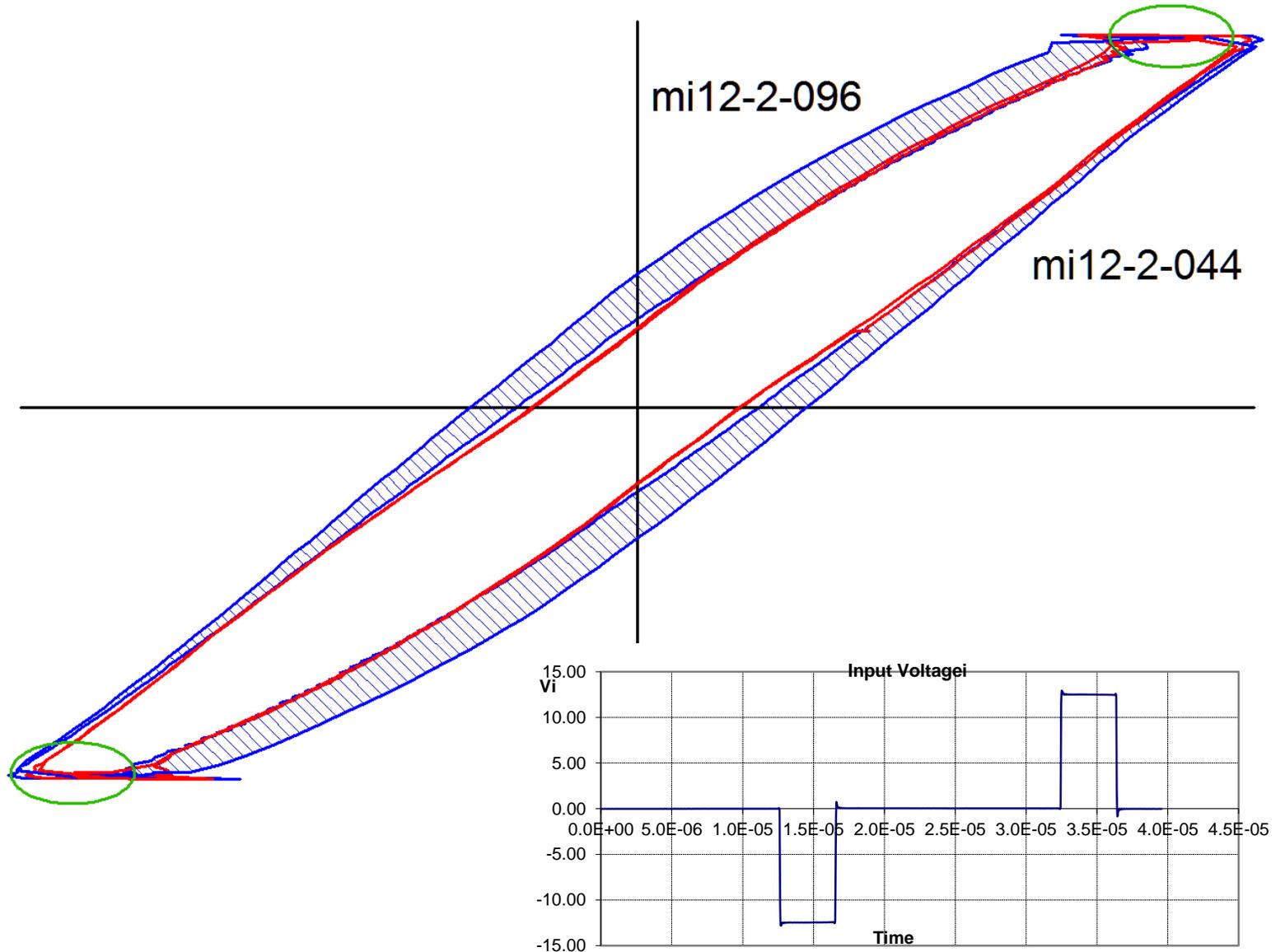
# SPICE model error

The hysteresis loop is useful for synthesizing the SPICE model, but it is useless during the off-time, as the V-s (Y axis) does not change.

The off time occurs within the green ovals.

The SPICE model shows the same loss as an excitation with the same pulse width and voltage but without off-time.

The actual hysteresis loop for mi12-2-096 shows significantly higher loss.



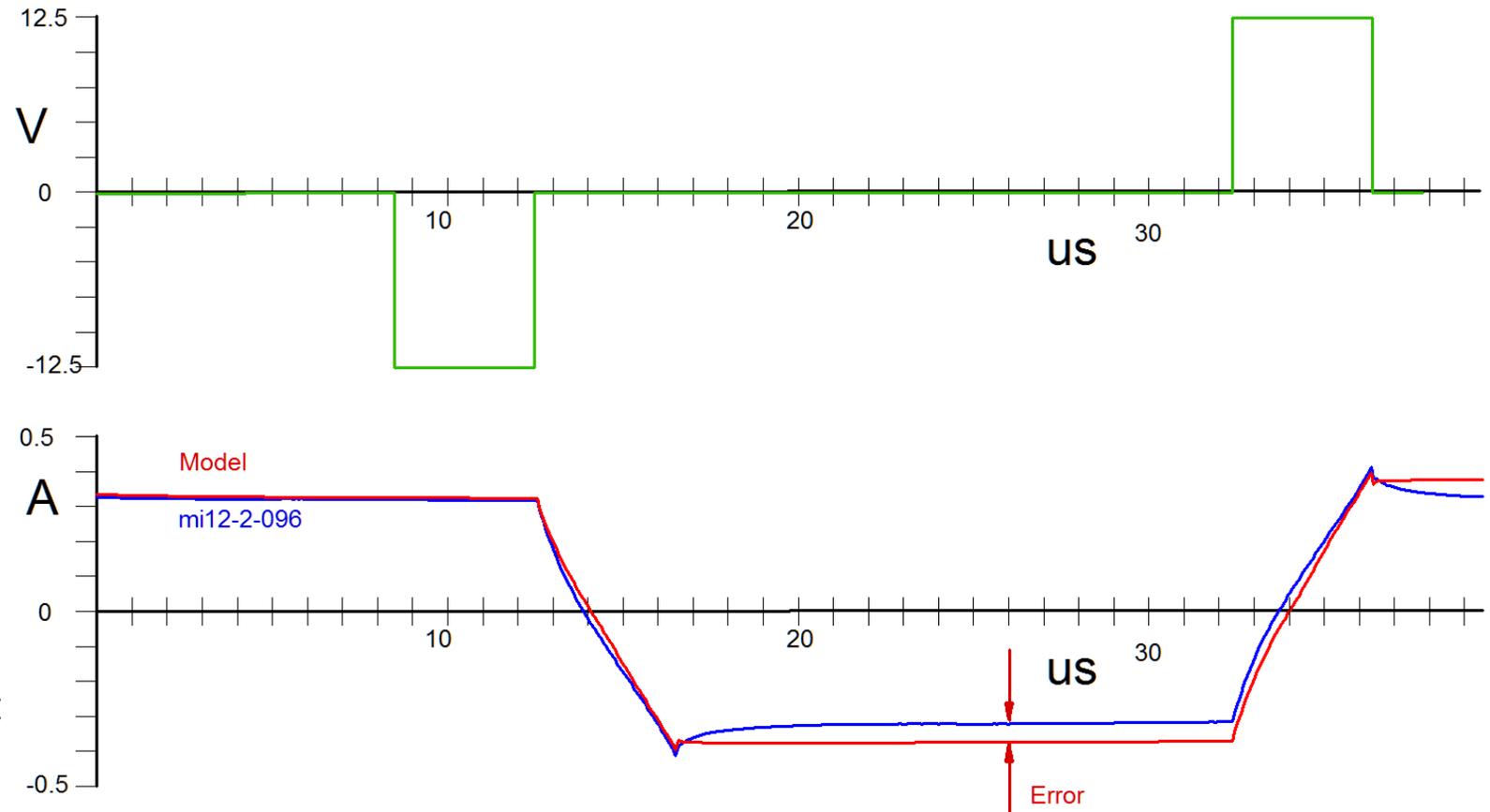
# Off-time losses

To see the error, it is necessary to look at the actual current and compare it to the current produced by the SPICE model.

It can be seen that the current in the SPICE model does not change during the off-time, whereas the actual current changes significantly.

The real core loses significant energy during the off-time, which has to be made up during the next on-time.

This function has to be added to the SPICE model.



# Hysteresis loop of an R-L circuit

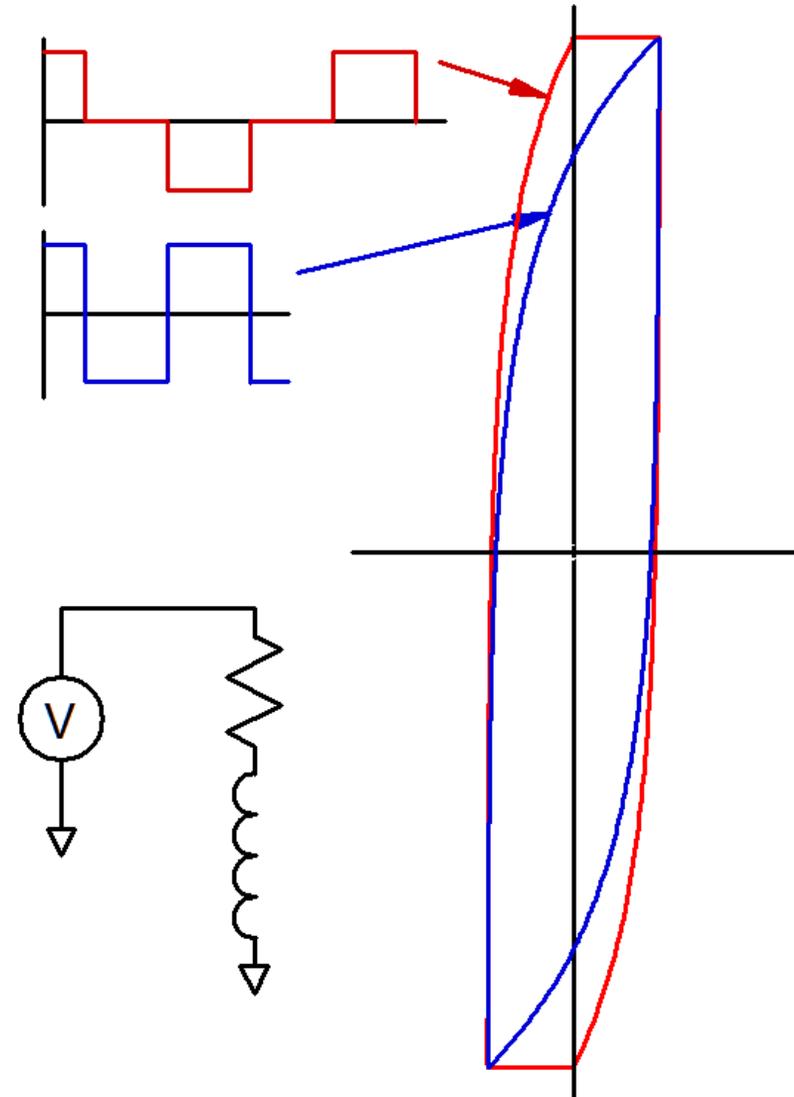
Earlier, we looked at the hysteresis loops of an inductor, a resistor and R-C circuits with different time constants, all with square-wave excitation.

If we look at the hysteresis loop of a resistor in series with an inductor, we see the **blue** curve on the right.

If we then look at the hysteresis loop of the same R-L with reduced duty-ratio, we see the **red** curve.

The loss is significantly higher.

This very likely is the underlying cause of the off-time phenomenon losses. Very likely, it can be quantified.

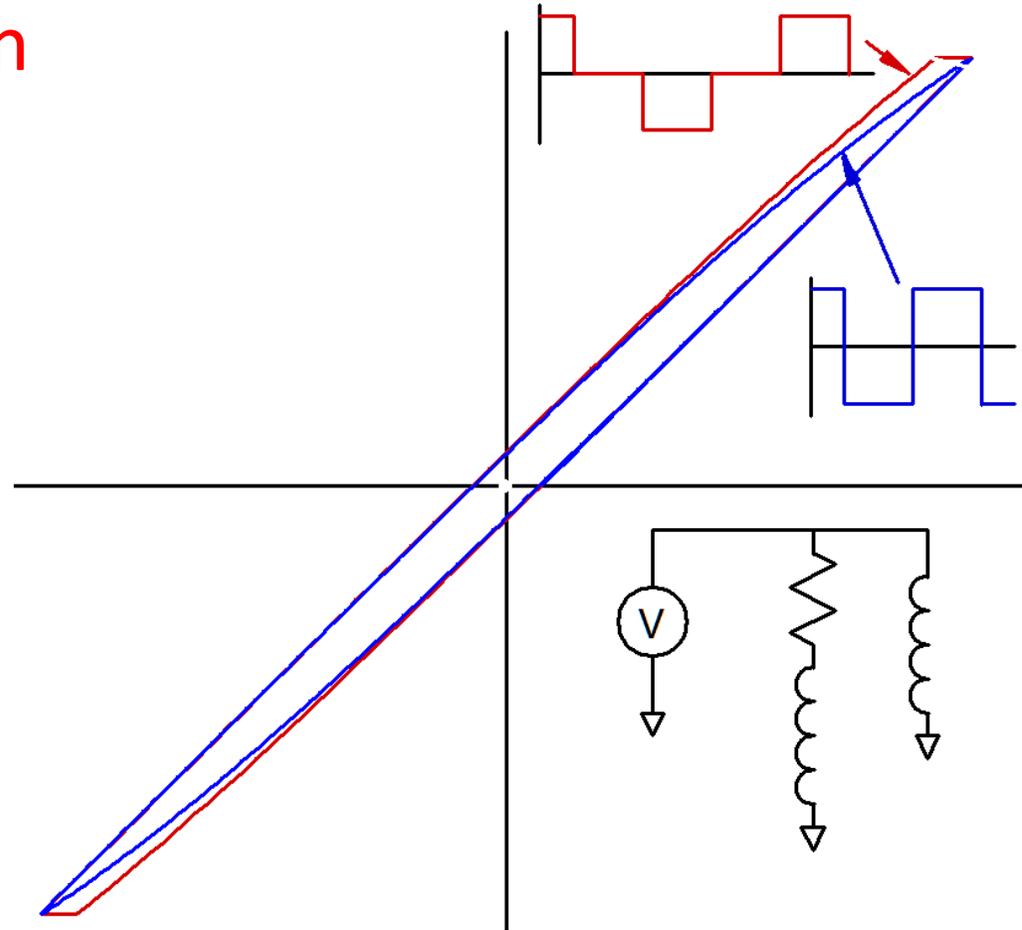


## Hysteresis loop of an R-L in parallel with a larger L

If a resistor and inductor in series are placed in parallel with the inductor in a SPICE model, their combined hysteresis loop is as shown on the right.

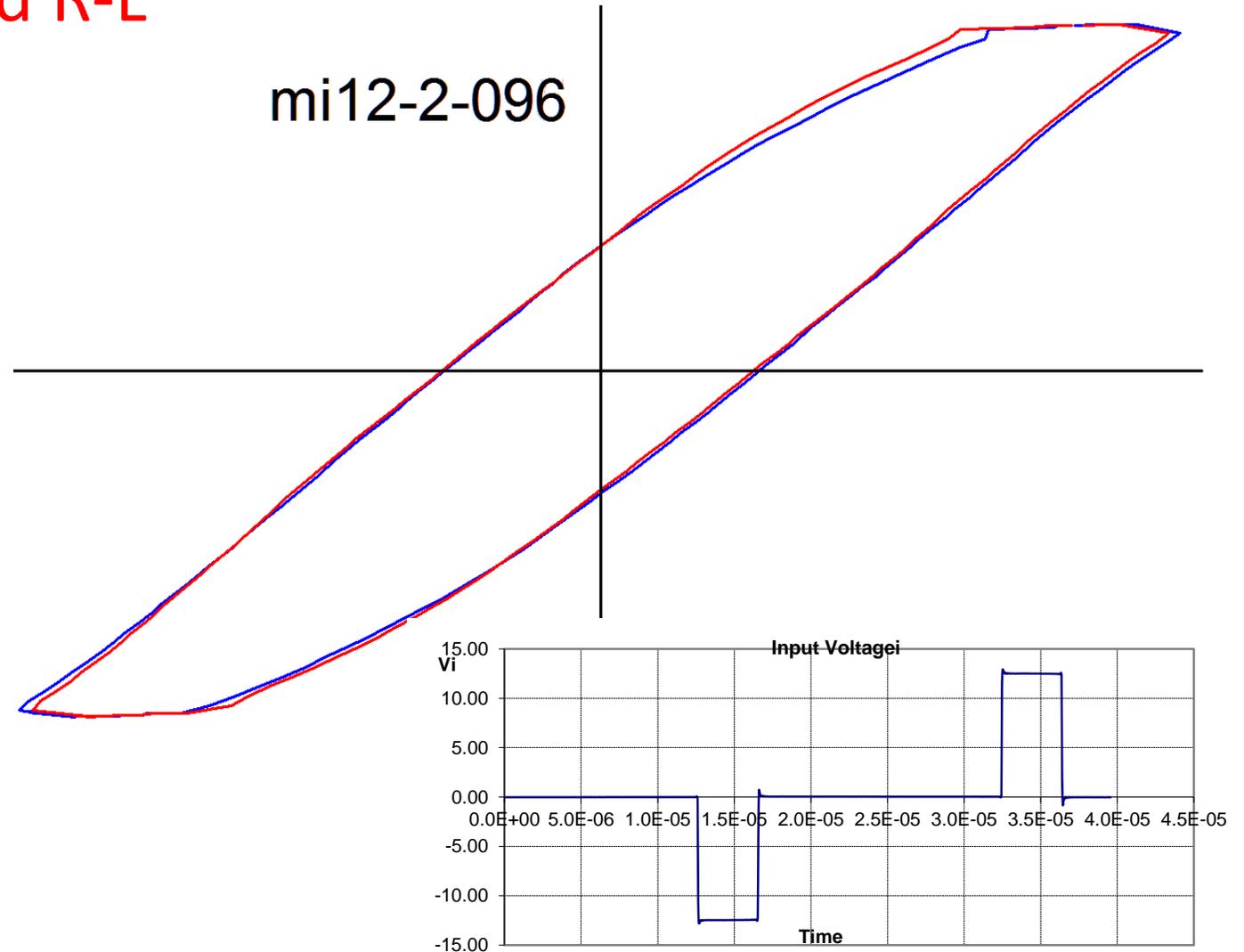
The blue curve is for a square wave, and the red curve is with reduced duty-ratio.

The losses become significantly higher as off-time is introduced into the waveform.



# SPICE model with added R-L

If a resistor in series with an inductor are added to the SPICE model, trial and error can find values that produce a good fit to the data.



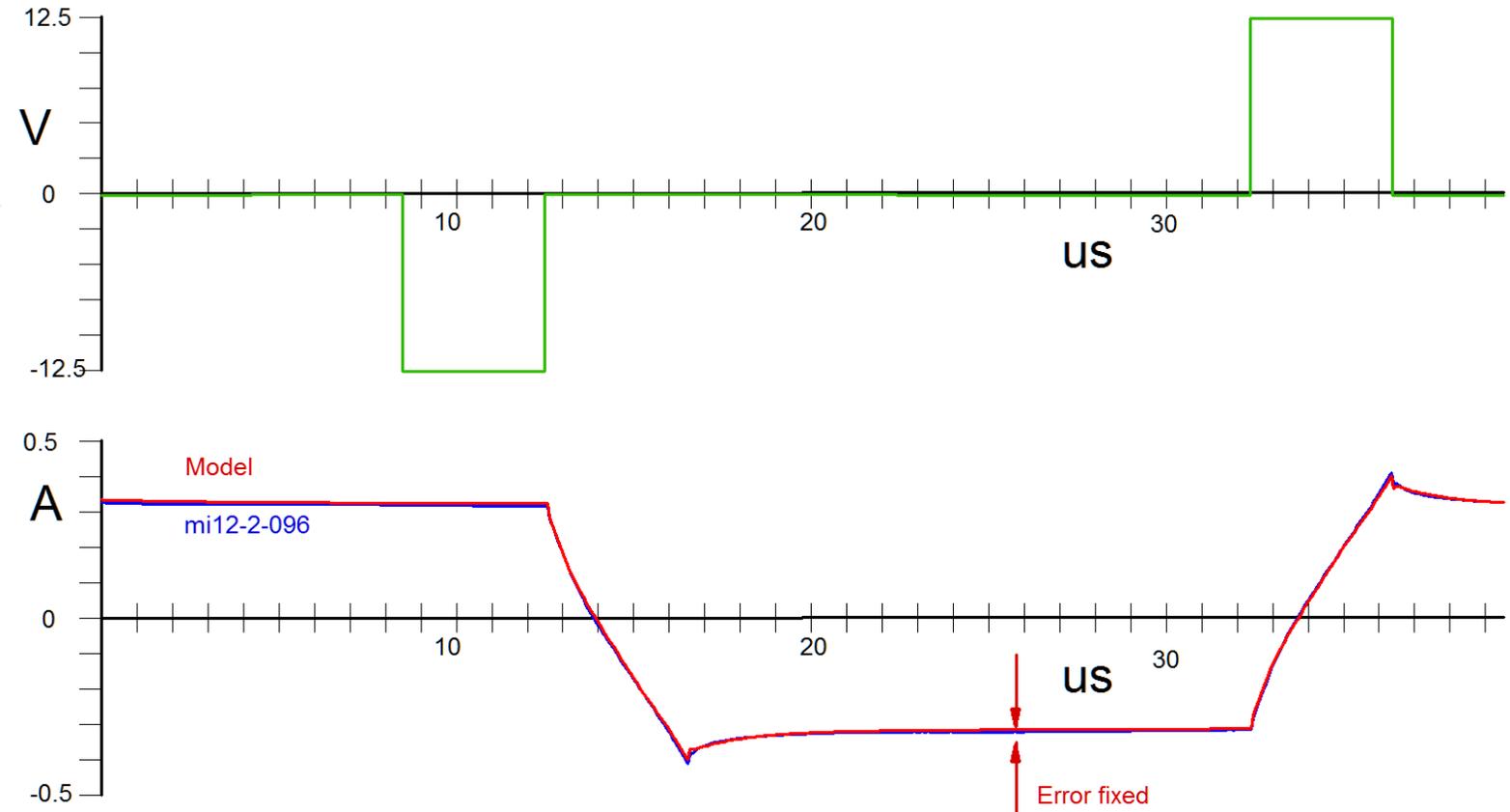
# Correction applied

The Spice model now tracks the test current quite well.

Adding a function to a SPICE model is like playing Whac-A-Mole. Once something is added, all of the components in the model and the algorithms have to be reevaluated.

With so little data with low duty-ratio, I did not try to do this.

However, I am optimistic that it can be done.



# Off-time with R-C

There are no data for the off-time phenomenon with a series circuit of a resistor and a capacitor, but a SPICE model suggests that this circuit has lower losses with lower duty-ratio.

This further complicates updating the SPICE model to include low duty-ratio waveforms.

## Conclusion

There are way too little data to begin integrating off-time into a SPICE model at this time.

Once data are available, I am optimistic that it can be done.

