A High Power Density Three-Phase Inverter Adopting Double-End Sourced Power Module Structure

CHPPE Center for High Performance Power Electronics

Presented by : Fang Luo

The Ohio State University

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3D-PEIM
3D Power Electronics Integration and Manufacturing

The Ohio State University

Outline

- Introduction
- DOUBLE-END SOURCED (DES) Layout
- Performance Evaluation
- Three-Phase Inverter Design

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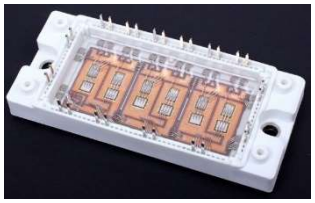
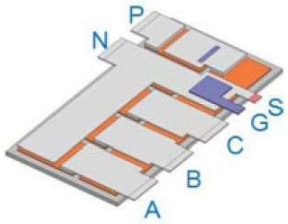
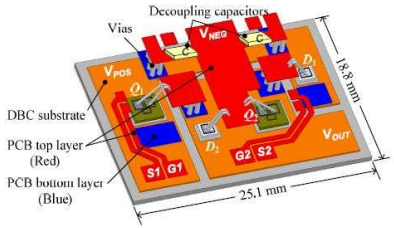
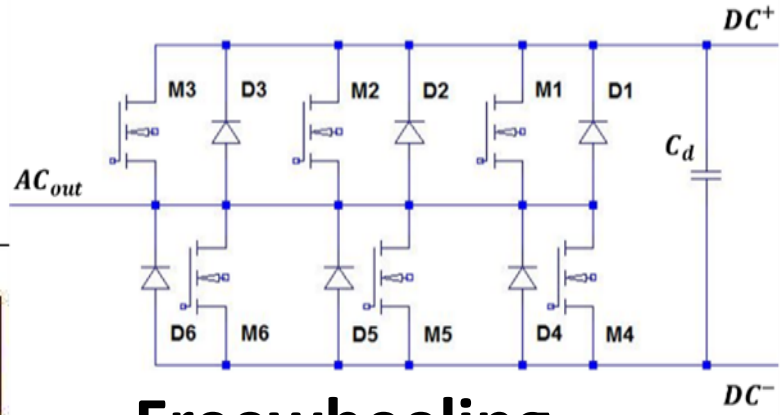
		Pros	Cons
Wire-bonded	 Courtesy of Cree	➢ High maturity ➢ Low cost	➢ Large stray inductance
Planar	 Courtesy of Virginia Tech	➢ Reduced inductance ➢ Double-side cooling	➢ High Complexity ➢ Double-side solder-able device
Hybrid	 Courtesy of Virginia Tech	➢ Medium fabrication difficulty ➢ Medium inductance	➢ Low maturity ➢ Relatively new

Conventional Layout



Freewheeling Diode

DC^+

AC_{out}

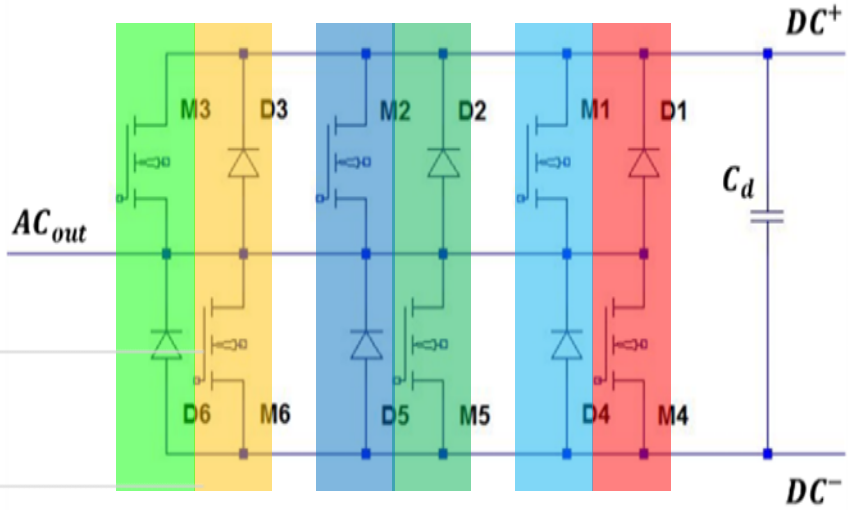
C_d

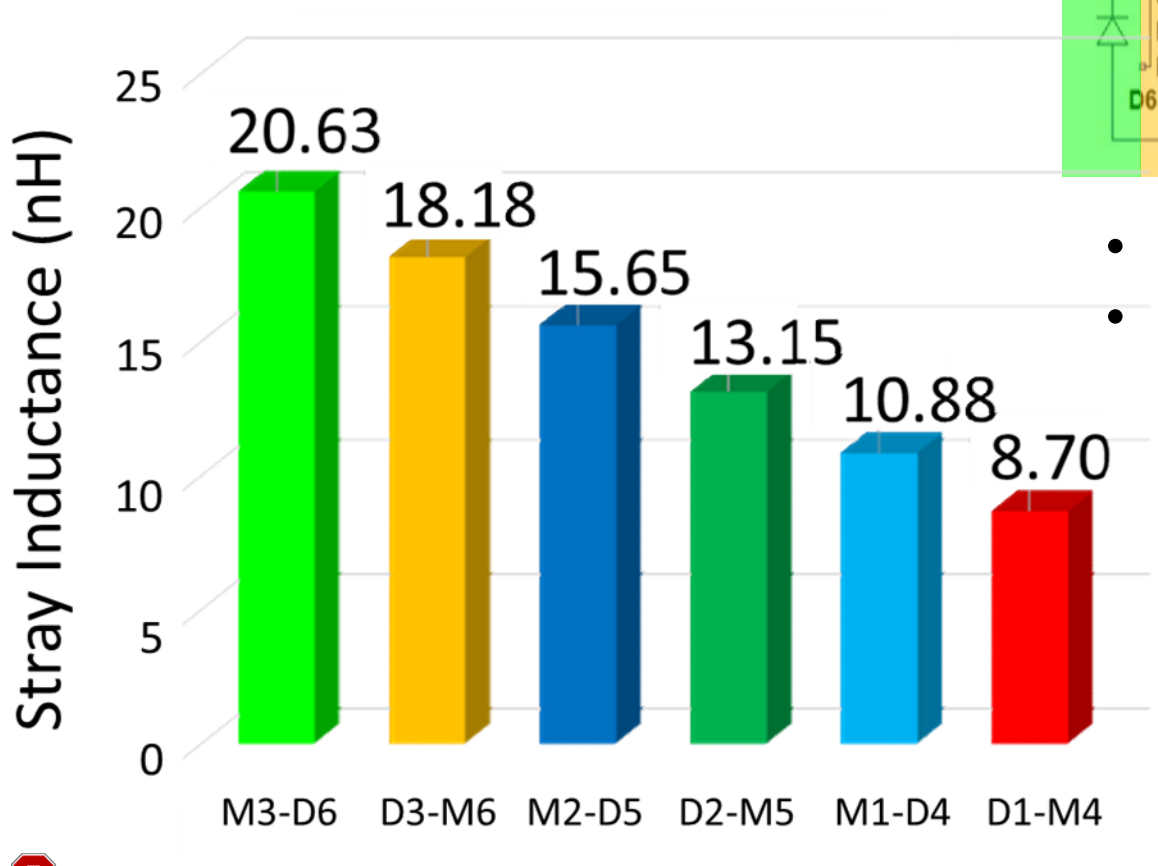
DC^-

MOSFET

Gate & Kelvin Source

Power-Loop Inductance





- Large stray inductance
- Unbalanced power loops

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- **DOUBLE-END SOURCED (DES) Layout**
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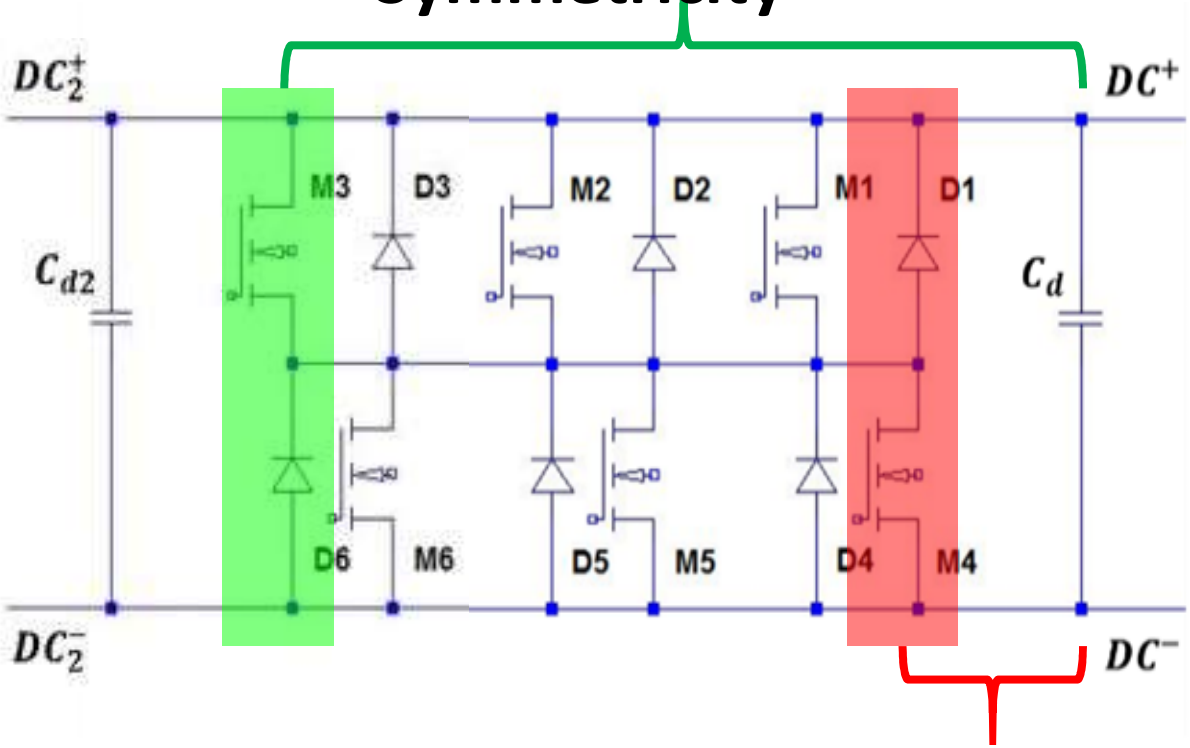
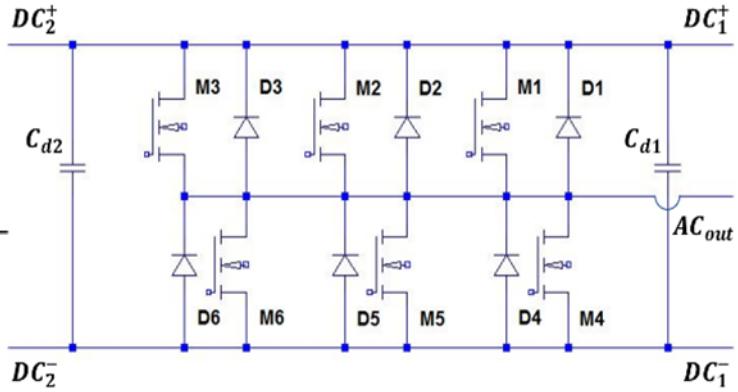
Long Distance → Large Inductance

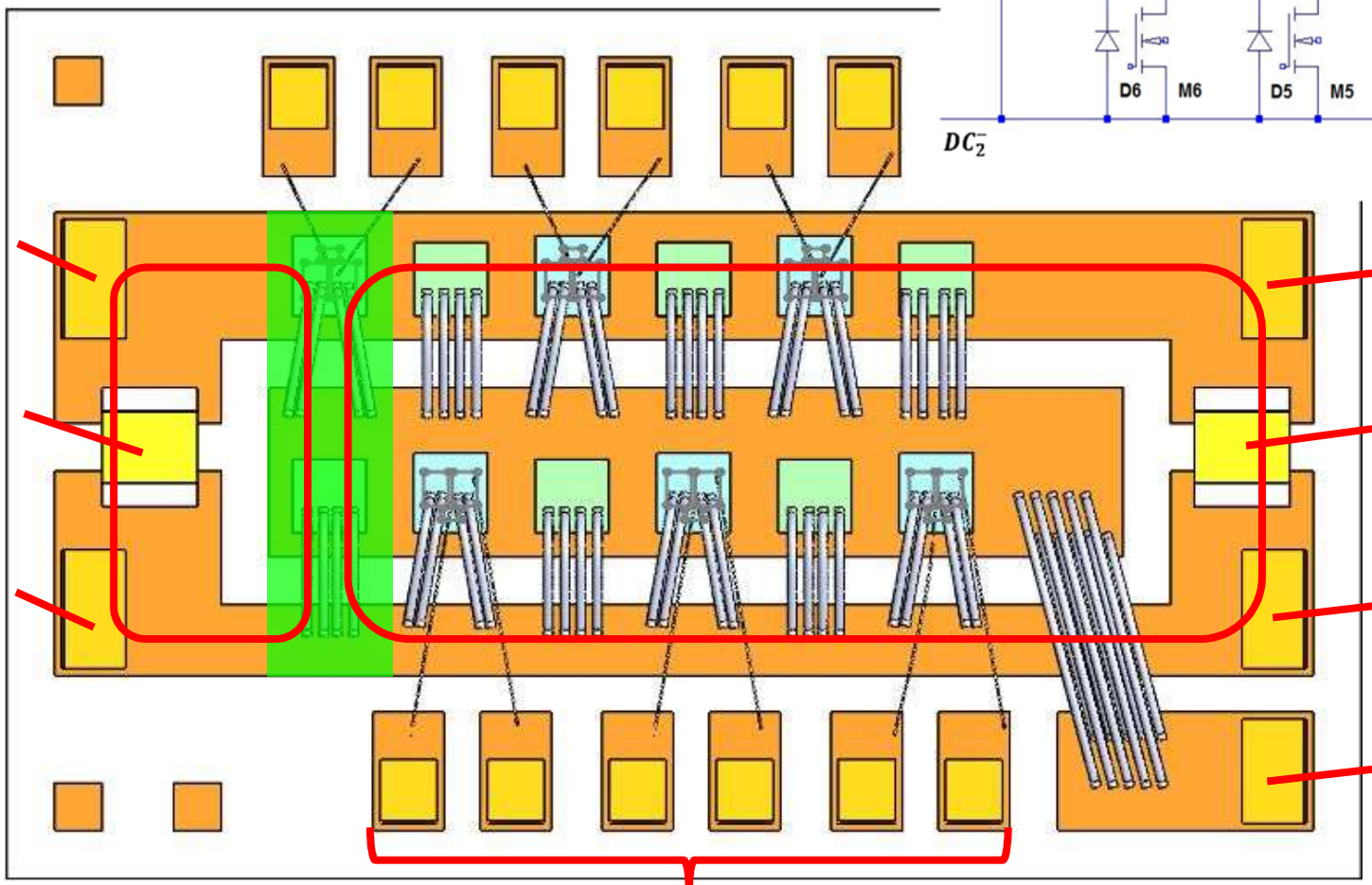
Symmetricity



Short Distance → Small Inductance

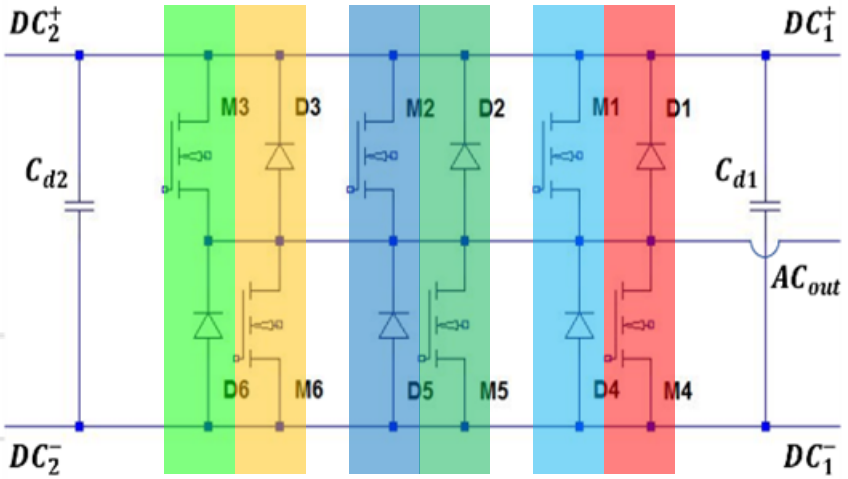
DES Layout

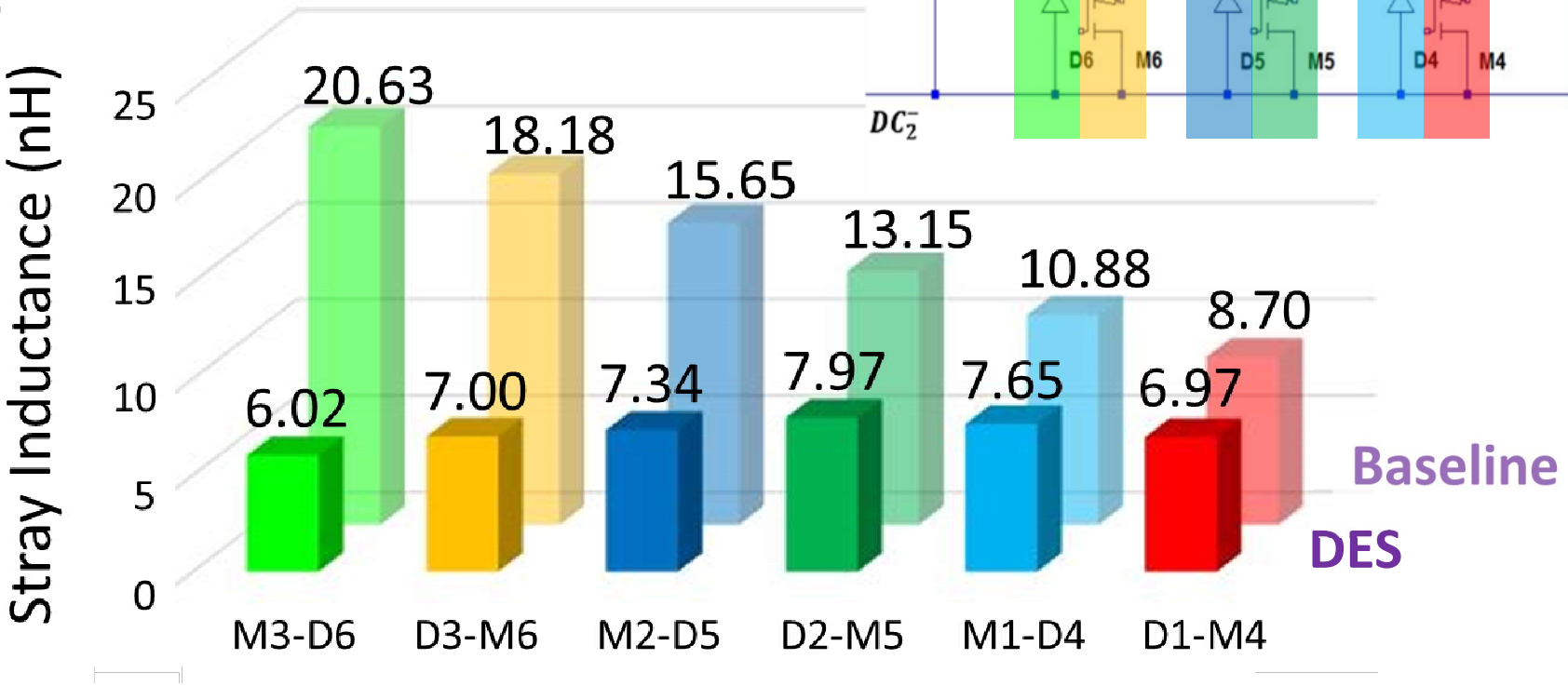

DC_2^+
DC_1^+
M3
D3
M2
D2
M1
D1
C_{d2}
C_{d1}
AC_{out}
D6
M6
D5
M5
D4
M4
DC_2^-
DC_1^-


DC_2^+
C_{d1}
DC_2^-
DC_1^+
C_{d1}
DC_1^-
AC_{out}
Gate & Kelvin Source

Power-Loop Inductance

- Reduced stray inductance
- Balanced power loops





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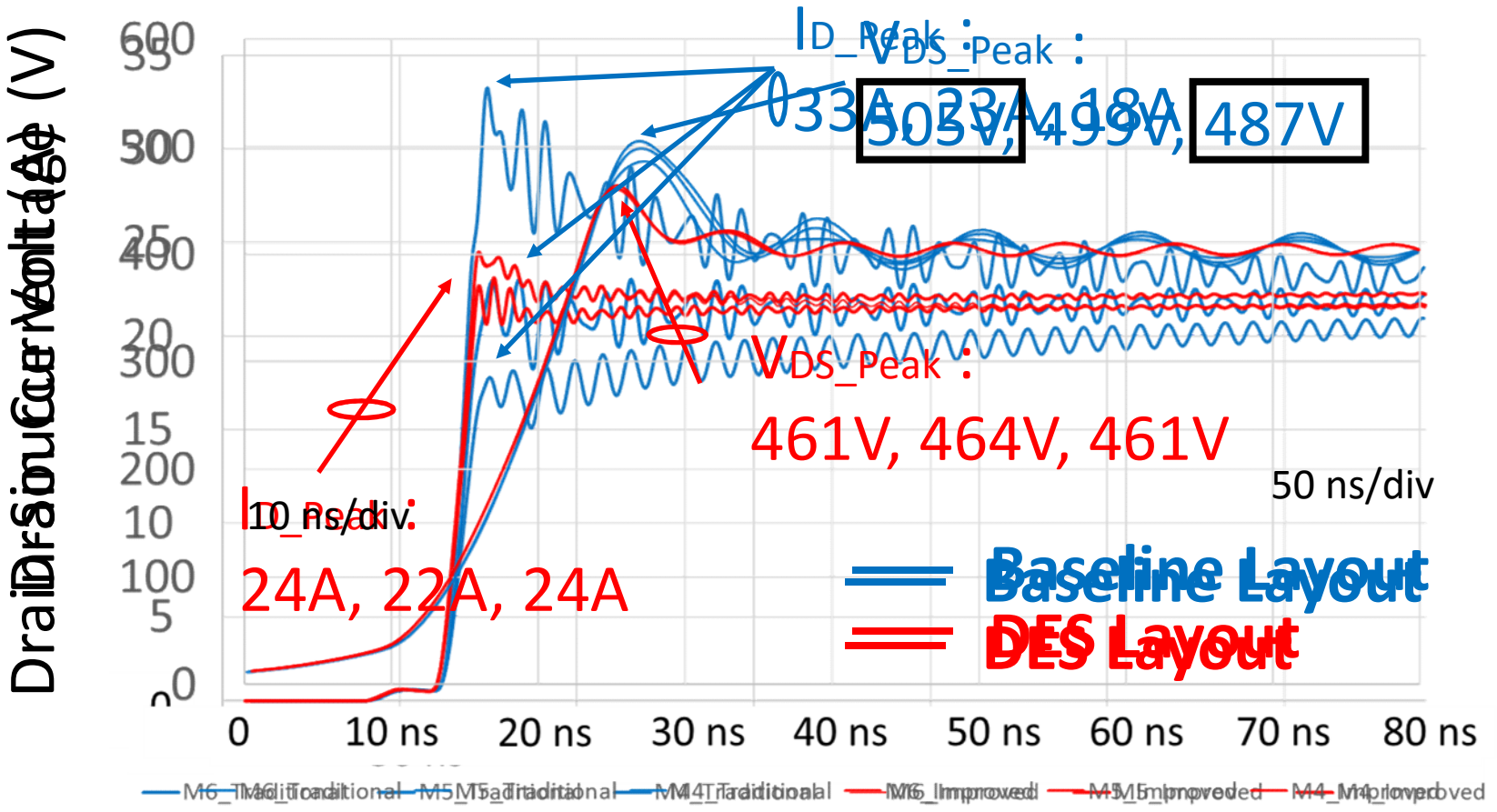
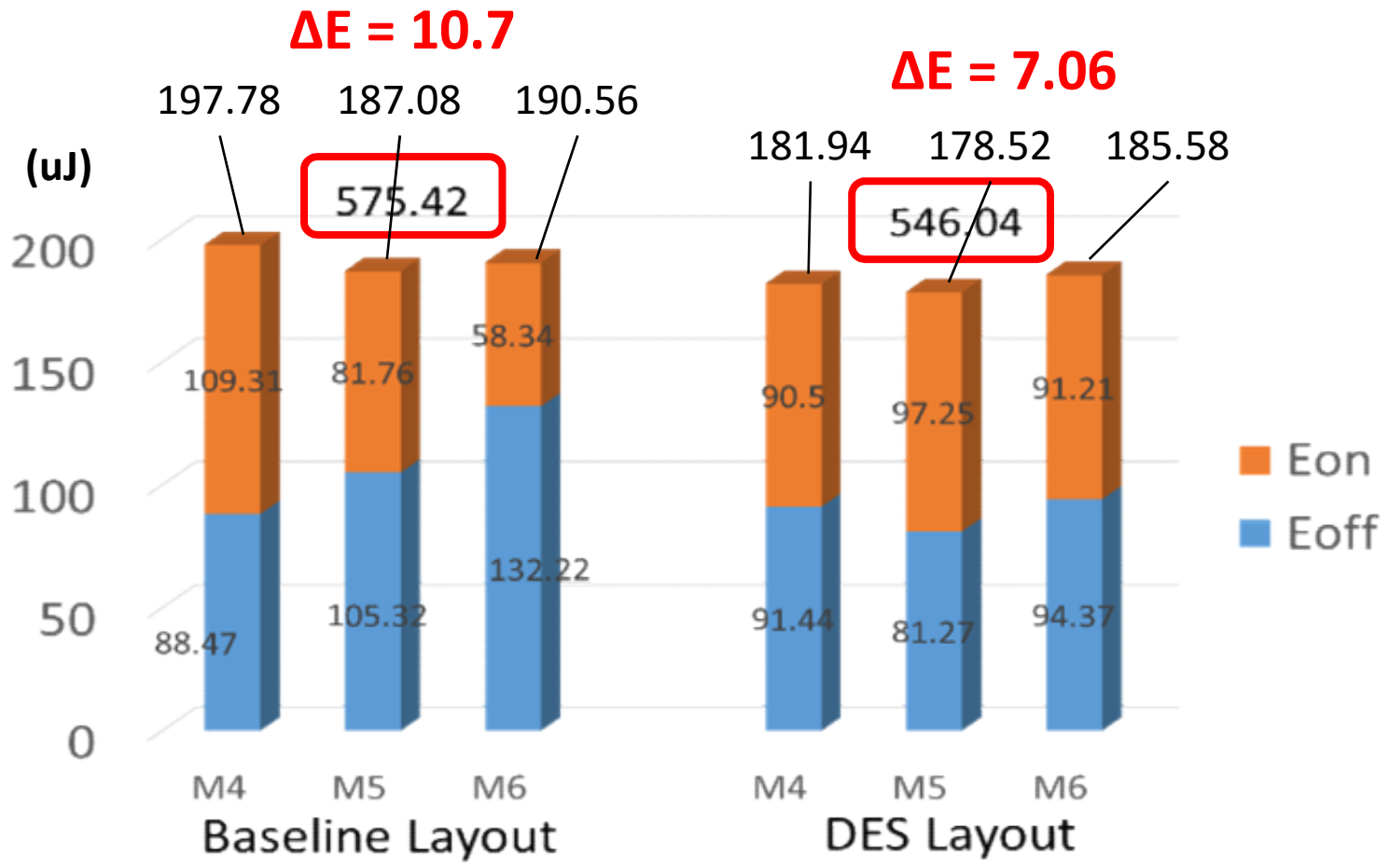
- Three-Phase Inverter Design

Simulated Turn-off Waveform (400V/60A)

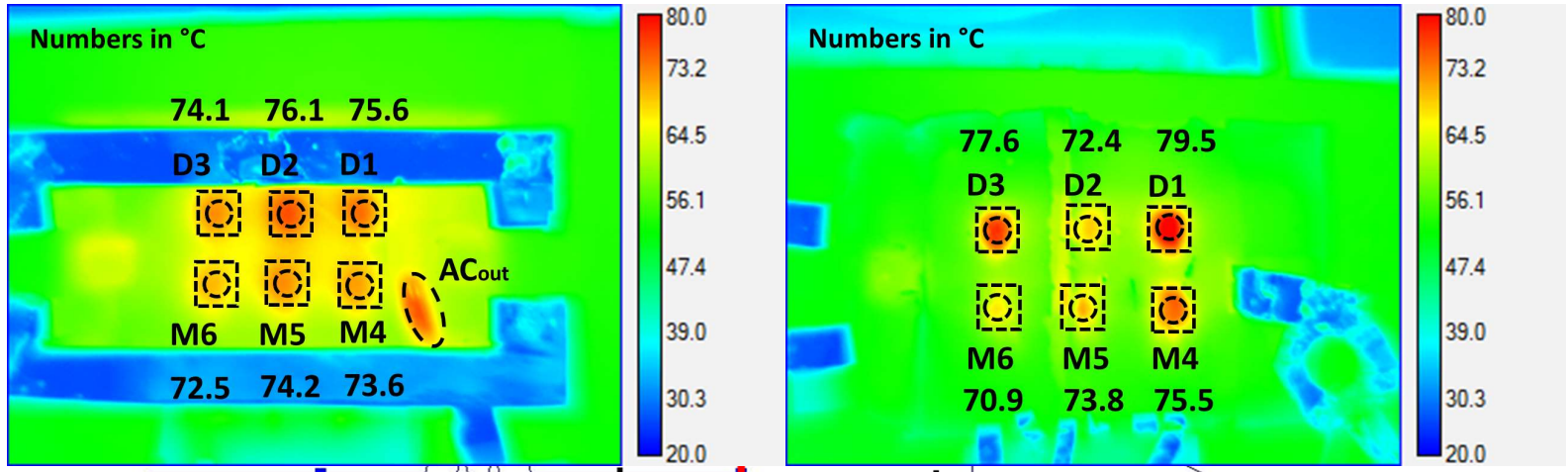


Switching Loss



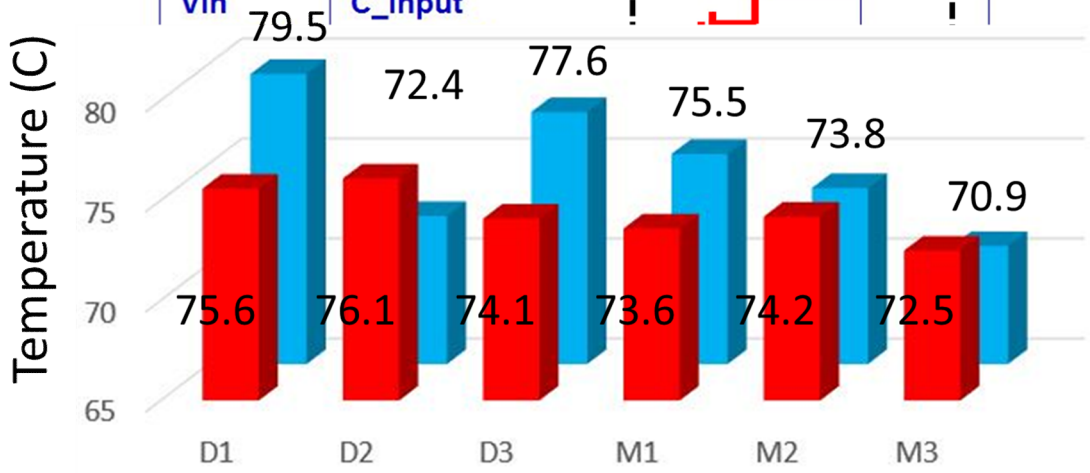
- **Total: 5.1% Lower**
- **Difference Reduced**

Continuous Power Test



DES Layout

Baseline Layout



Baseline

T_max = 79.5 °C

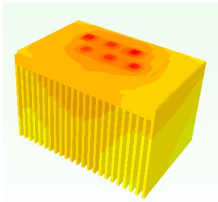
ΔT = 8.6 °C

DES

T_max = 76.1 °C

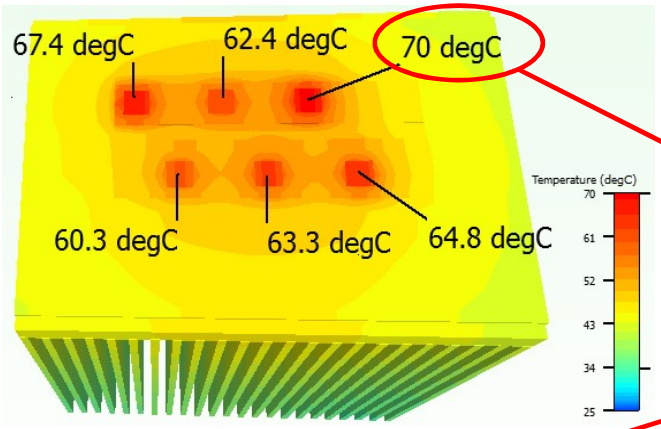
Δ T = 3.6 °C

Comparison of heatsinks

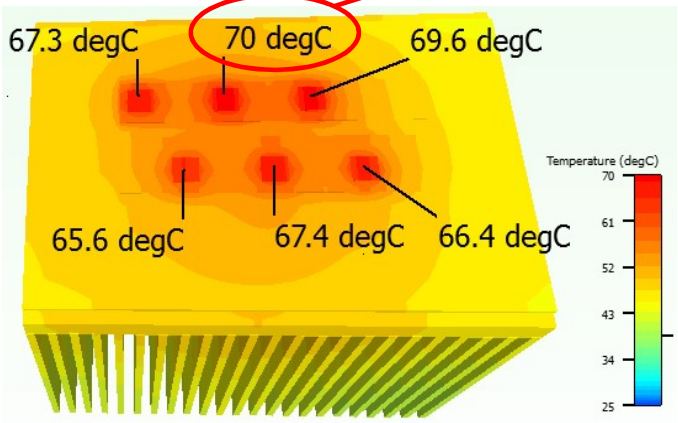


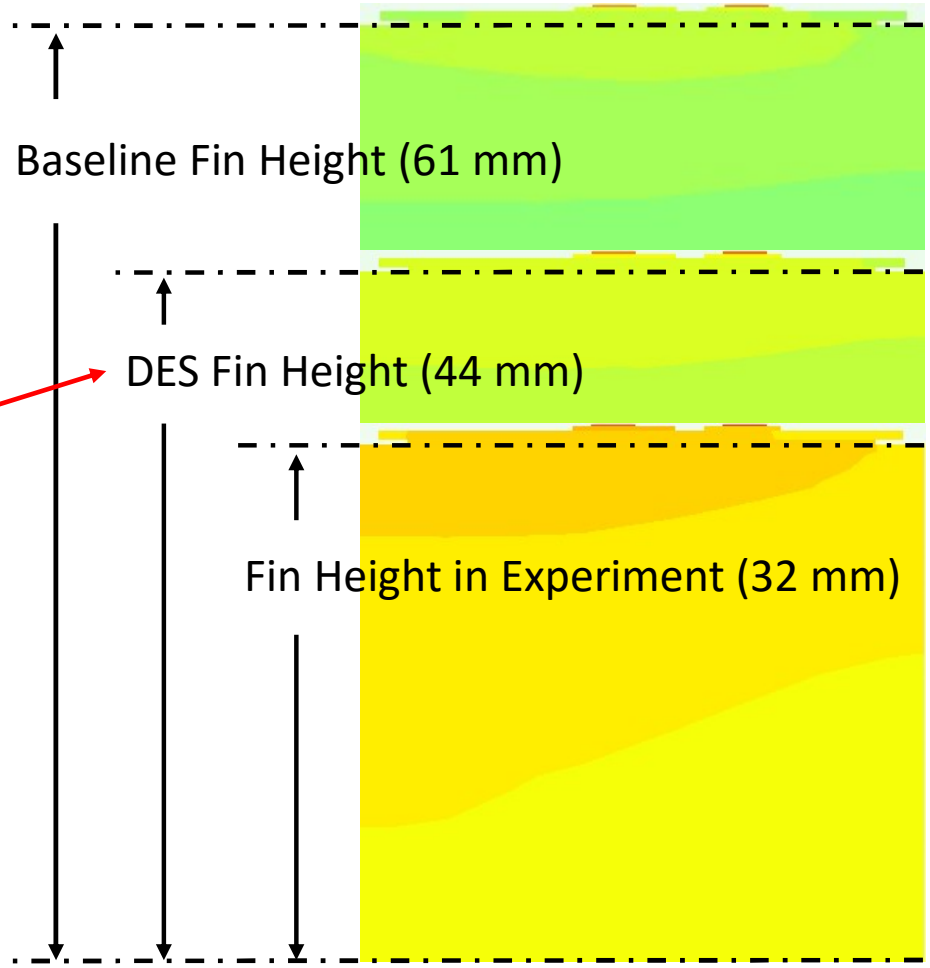
Side View

Baseline Design



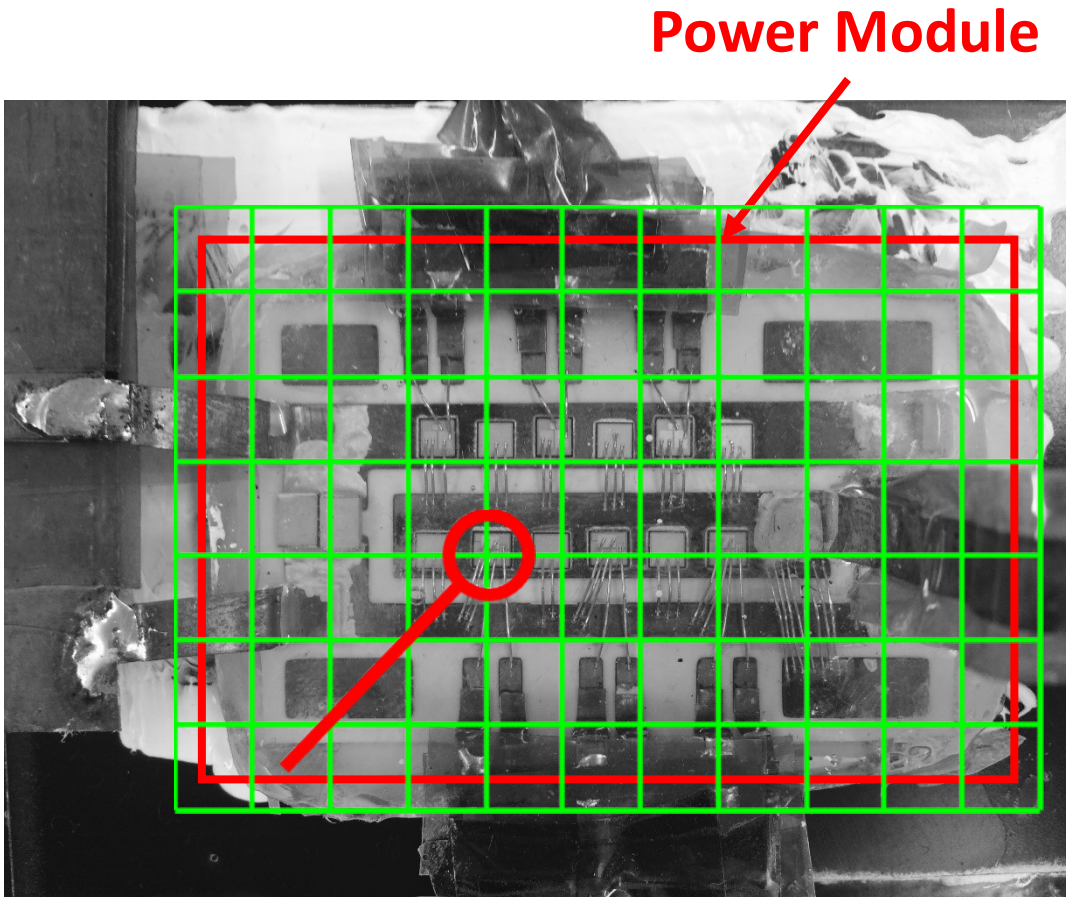
DES Design



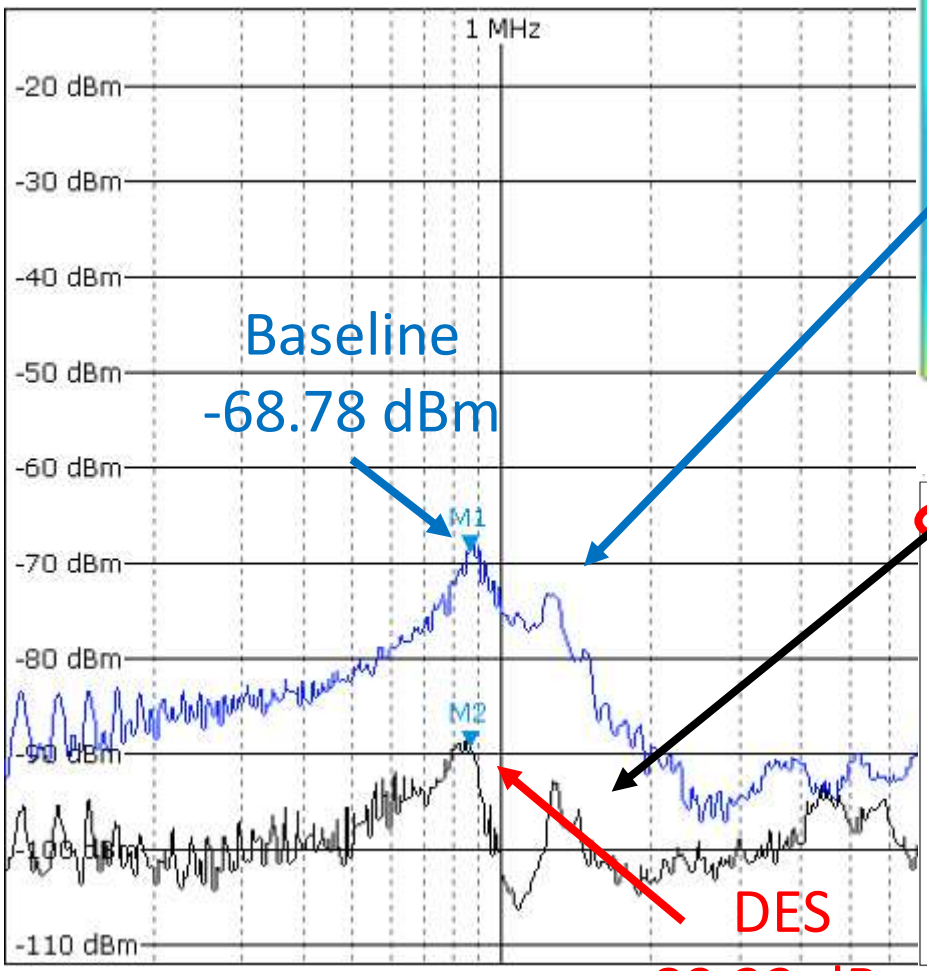


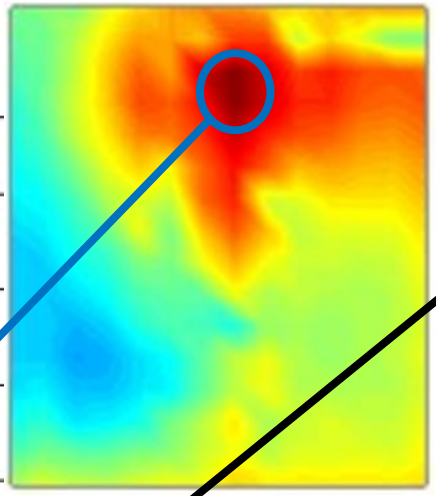
To restrain the hot point within 70 degrees:

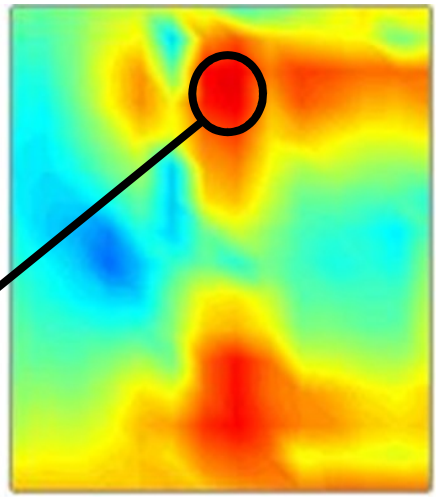
Near Field Radiation



Near Field Radiation

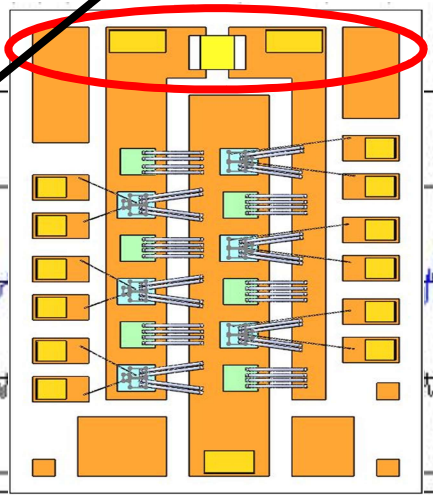


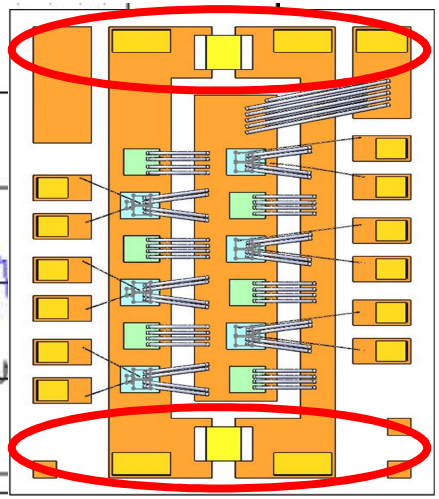




Baseline Layout

DES Layout





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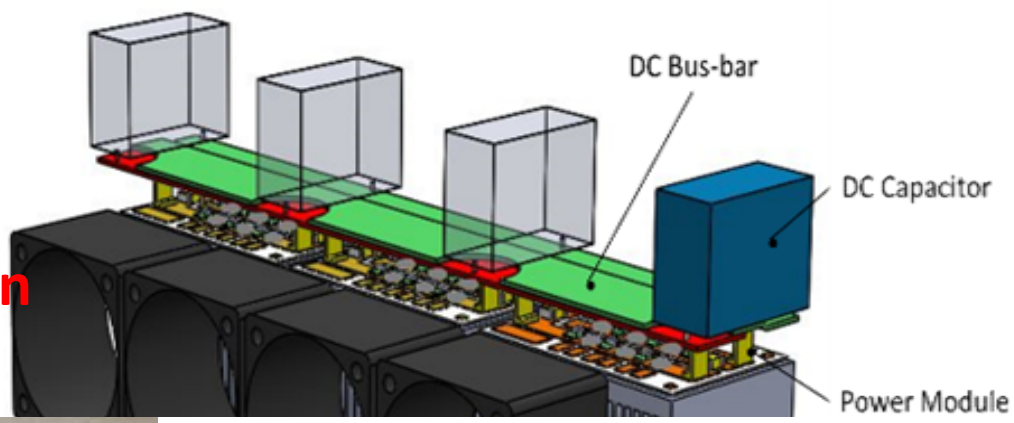
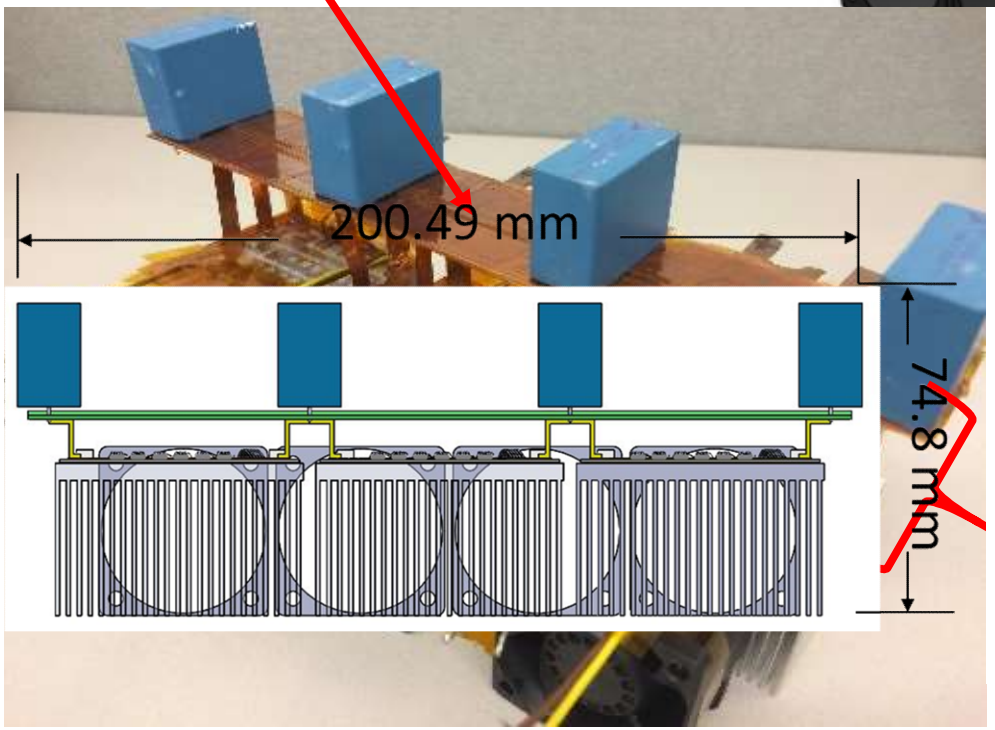
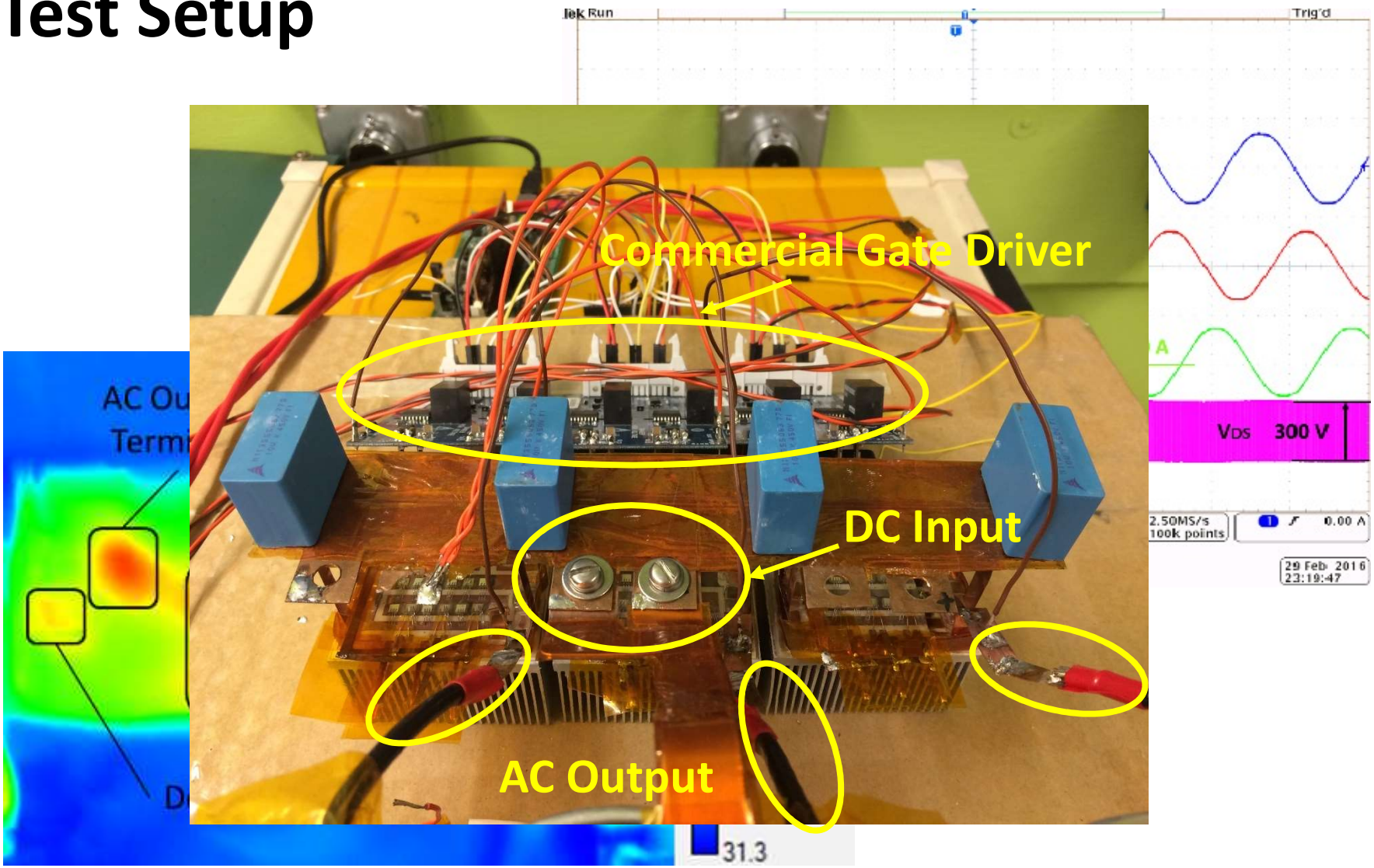
Vertical integrated DC link design



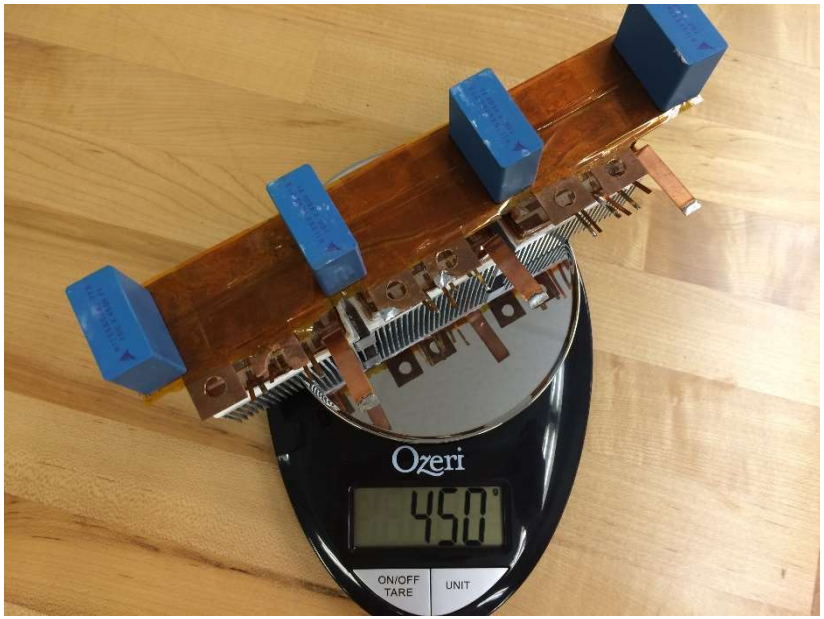


[1] www.passivedevice.com

Test Setup


Tek Run
Trig'd
Commercial Gate Driver
DC Input
AC Output
VDS 300 V
2.50MS/s
100k points
0.00 A
29 Feb 2016
23:19:47
31.3

Power Density Estimation



Gate Driver Boards

Weight: 450 + 132 + 129 = ***711 gram***

Calculated Power Density: ***21.97 kVA/kg***

Power Modules, DC Bus-bar, DC Capacitors, Heatsinks

Cooling Fans

*Based on 300 V/60 A, designed for 800 V/60 A

Summary of DES Module Design

- ❑ Reduced stray inductances/Balanced power-loops
- ❑ Improved the switching performance of the module
- ❑ Reduced dynamic loss-imbalance among paralleled chips
- ❑ Increased power density
- ❑ Reduced near field EMI emission

- ➢ Challenges in converter level layout
- ➢ Challenges in gate-drive design and layout

Questions?

Thanks to the Ohio State University Institute for Materials Research