ipdia

The 3D Silicon Leader

High performing wire bondable vertical Silicon Capacitors for RF power modules

3D PEIM 2016 Raleigh

Catherine Bunel

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- Reliability
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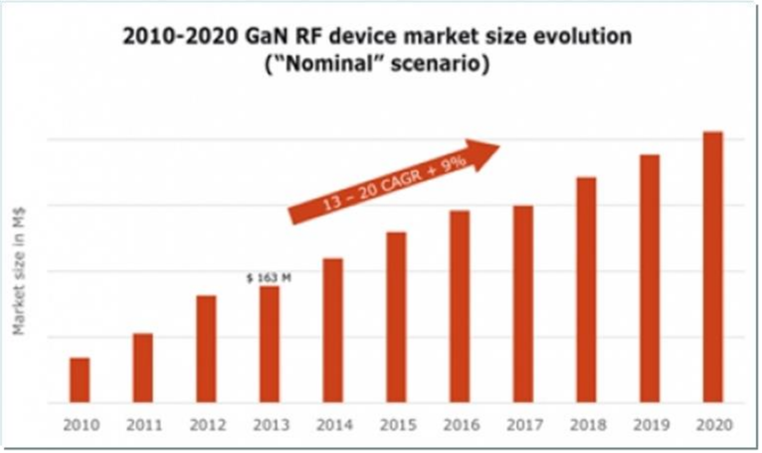
Who are we?

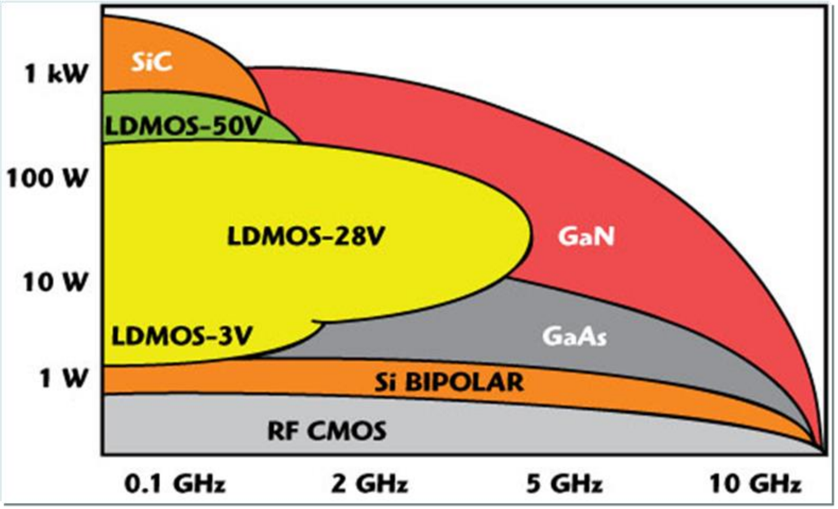
- Independent European High Tech Company
- Specialized in leading edge Integrated Passive Devices, world leader in 3D Silicon capacitors
- Operating own 10 000 m² Silicon wafer facility
- 25% of financial resources allocated to R&D
- 25% of sales in EU, 25% US, 50% Asia
- Technology adopted by 3 of the top 5 leaders in medical electronics as well as by key players in the semiconductor area and Hi-Rel industry

Introduction

- The need for high-power and high frequency transistors is increasing.
- GaN has progressed significantly over the last years
- GaN device portfolio is covering a wide range of applications.
- LDMOS performance is continuously pushed to its limits.



www.semiconductor-today.com



www. microwave journal.com

Requirements for RF products :

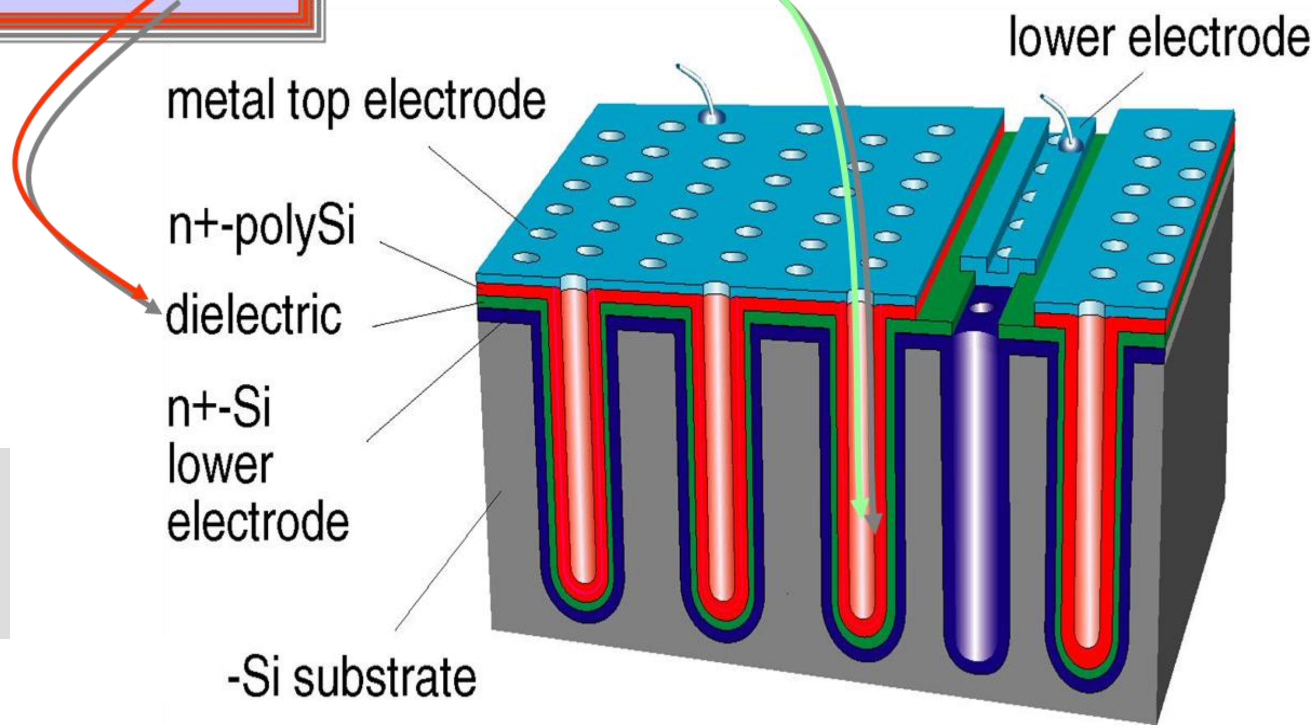
- High efficiency
- High bandwidth and linearity
- High polarization voltage
- Low cost
- High reliability
- Smaller footprint

Value proposition of the 3D Si capacitors :

- Proper decoupling of the power supply :quick, smooth response to the large current demands of the output circuit .
- Low parasitic loss.
- High capacitance density with high voltage
- Small footprint and low profile
- High performance and power efficiency by using larger capacitor value in a small package
- Cost saving due to the package size reduction.

3D Capacitor Technology

$$C = \frac{\varepsilon_0 \varepsilon_S \cdot S}{e}$$



Capacitance

1.3nF/m² up to 900 nF/mm²

BV 450V down to 6v

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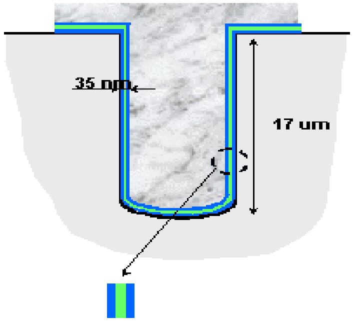
3D Capacitor Technology

Architecture

1.3nF/mm² up to 6nF/mm²

VBD = 450V down to 150V

A.R. ~ 1:20

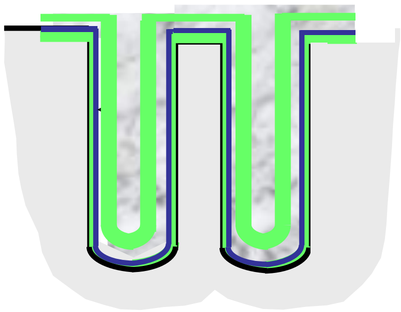


ONO (Oxide – Nitride – Oxide)

20nF/mm² up to 900nF/mm²

VBD min = 100V down to 6V

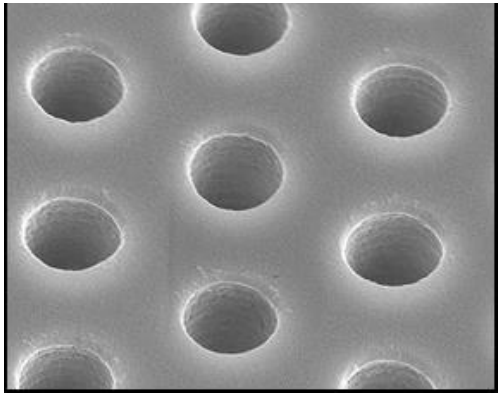
A.R. ~ 1:60



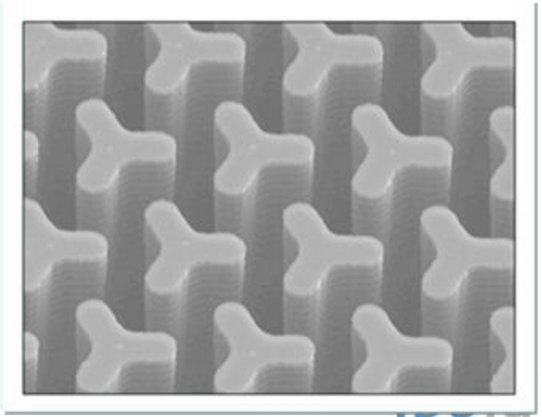
Nitride Double stack

Design

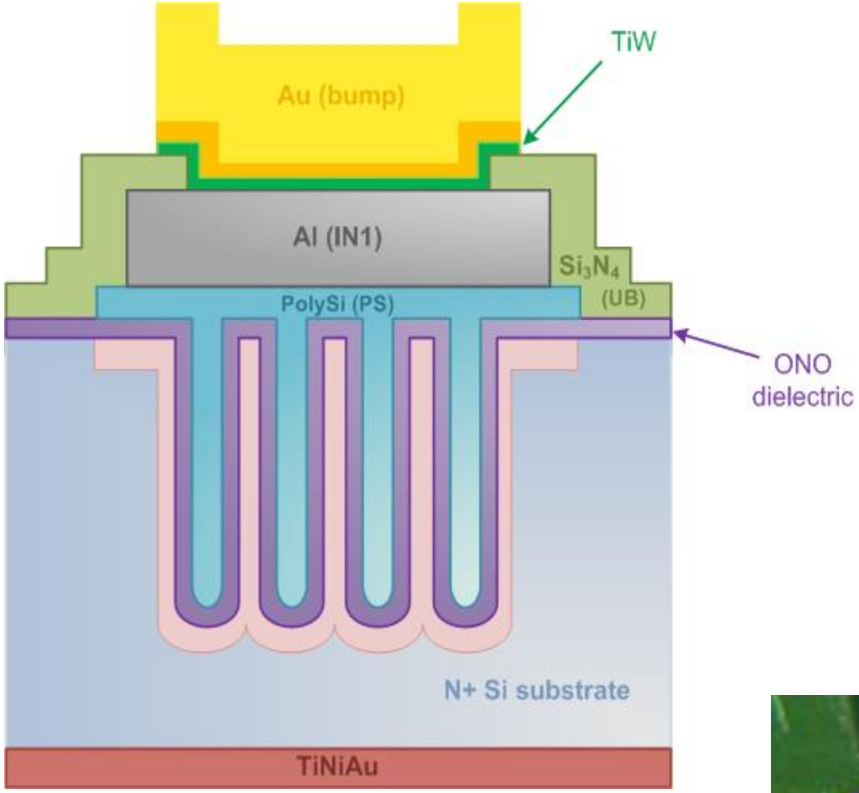
Pores

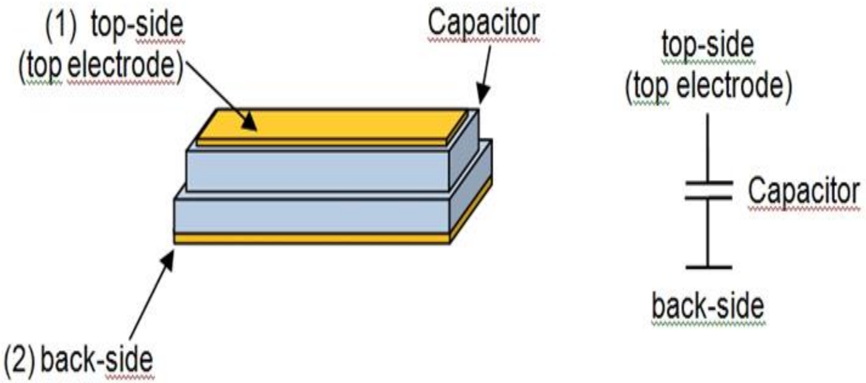


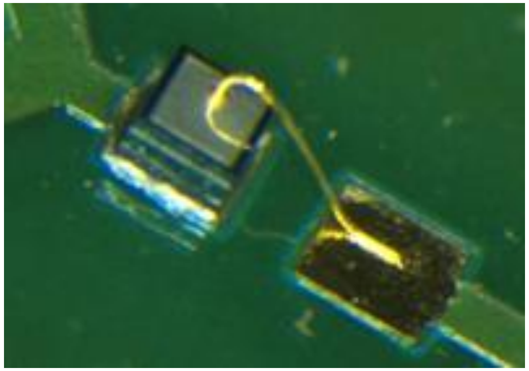
Tripods



Vertical 3D Silicon Capacitors

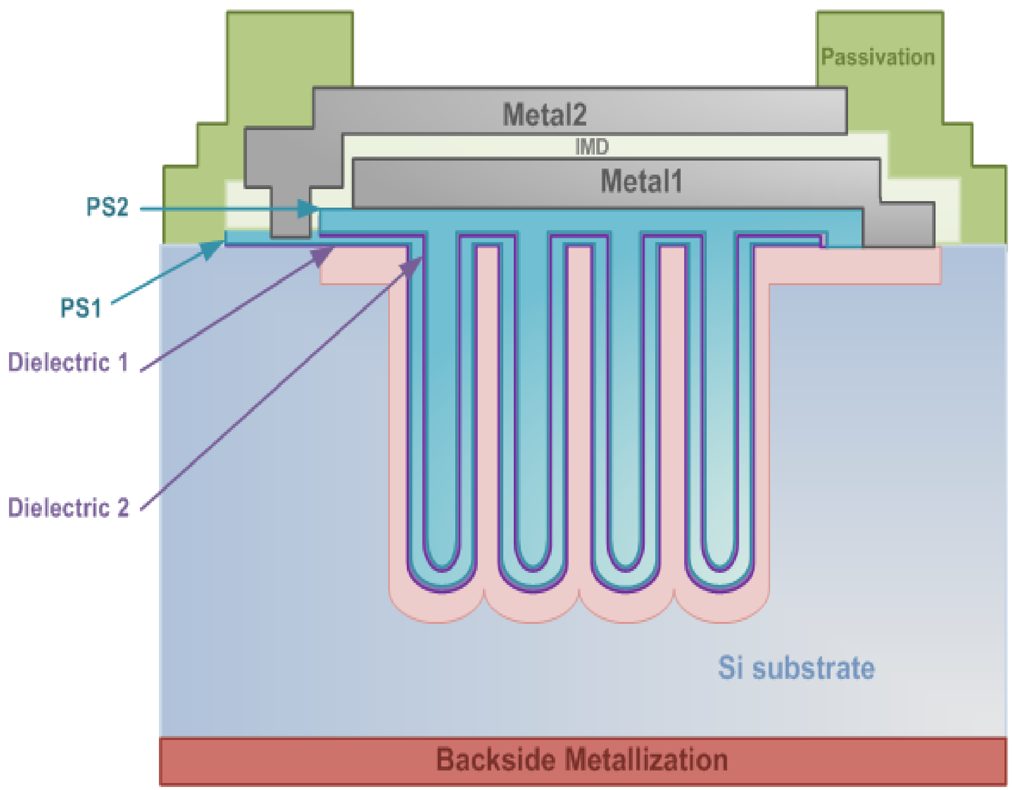


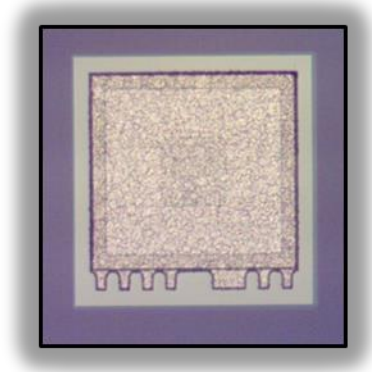


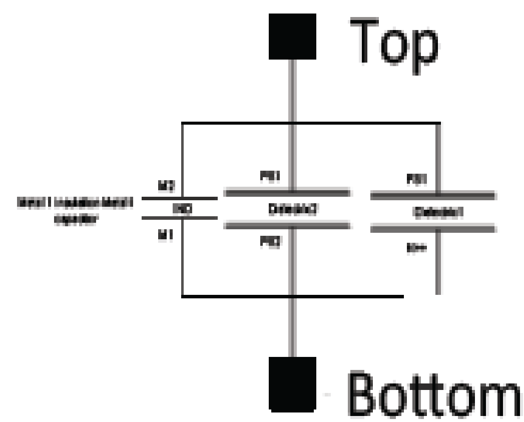


Capacitance
6nF/m² BV 150V

Vertical 3D Silicon Capacitors



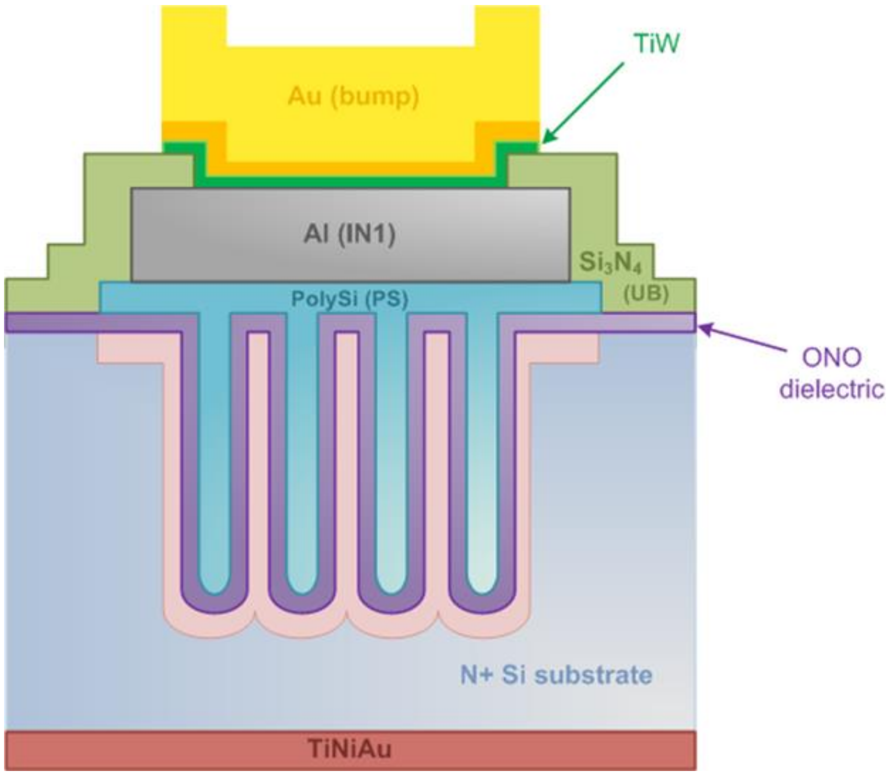




Capacitance

$20nF/m^2$ BV 100V

Low profile



Large range of die thickness from 100µm up to 400µm

100µm – 400µm

➔ Selected thickness depends on the Backside Metallization and the package constraints

Capacitor strength comparison between Ceramic and Silicon cap

Results after bending strength 3 points

	IPDIA Si CAP	Ceramic CAP
LW	0.5×1.0mm	1.0×0.5mm
T	100um	100um
Ave.[N]	2.8	1.3
Max.[N]	5.9	1.5
Min.[N]	1.4	1.0

0402 100nF 100µm thick

Silicon Capacitor is stronger than Ceramic Capacitor

Topside and backside metallization

- Topside : 3 to 5µm
  - Pure Aluminum
  - AlSiCu
  - TiWAu
  - TiCuNiAu T° >150° C , hermetic package

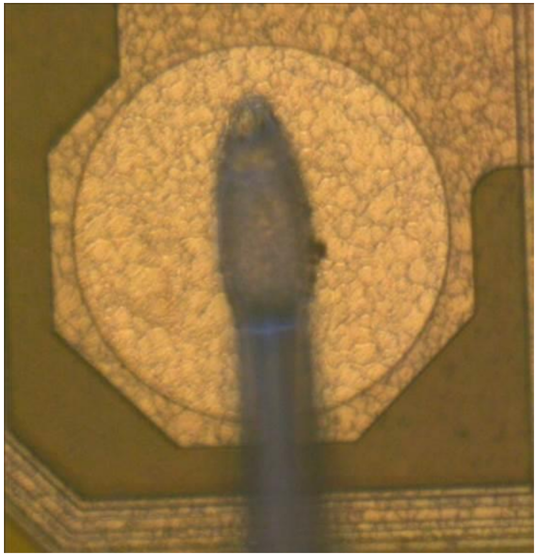
- Backside Metal : 3µm
  - Pure Au
  - TiNiAu

Wire bondable vertical Silicon Capacitor :

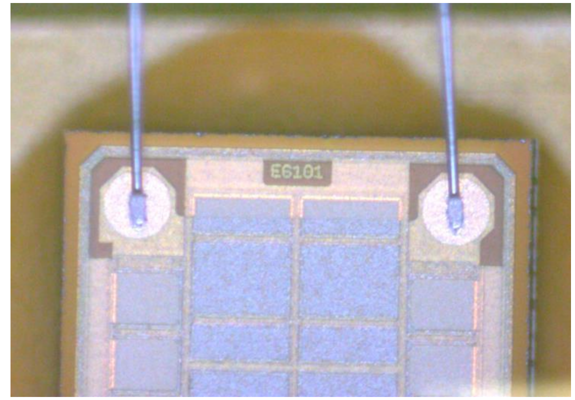
- Wedge bonding
  - Au wires
  - Al wires

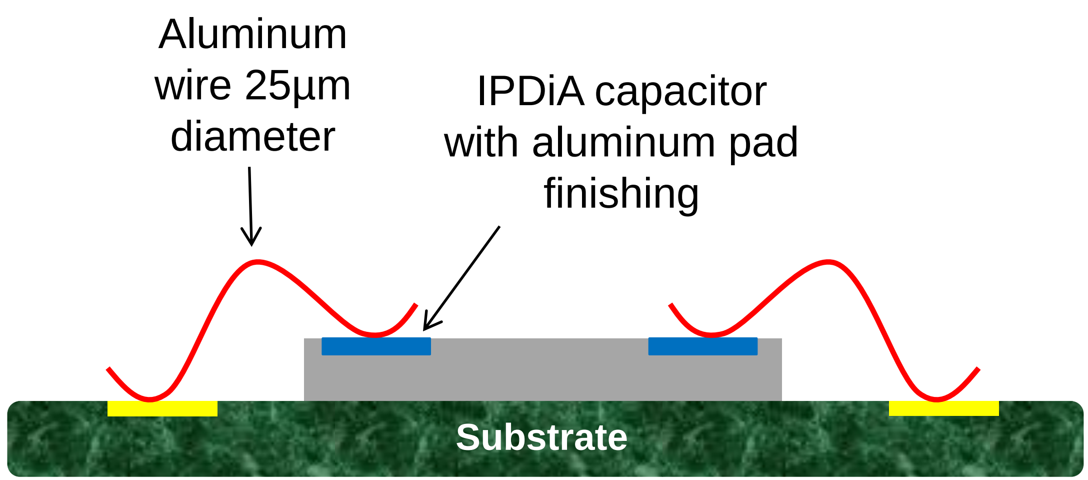
- Ball bonding
  - Au wires

Wedge bonding – Aluminum wire :



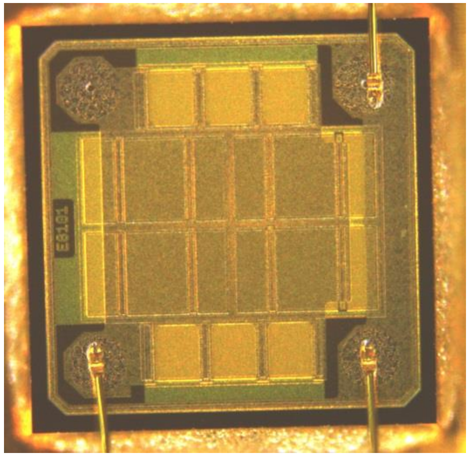
Bonding process : Wedge Alu	
Bonder	BJ820
Bonding Tool	CCNOE-1/16-1"-45-C-2020-MP
Wire	AL1%Si-SR-25-1-4%-17-19gf-12AL (SPM)
US	20% (400-440 mW)
Force	17 cN
Bonding time	10 ms - 20 ms
Deformation	25 - 35%
Temperature	Ambiant

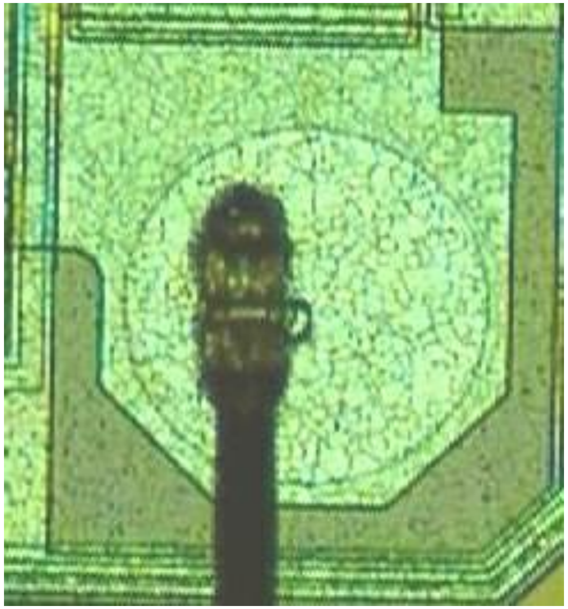




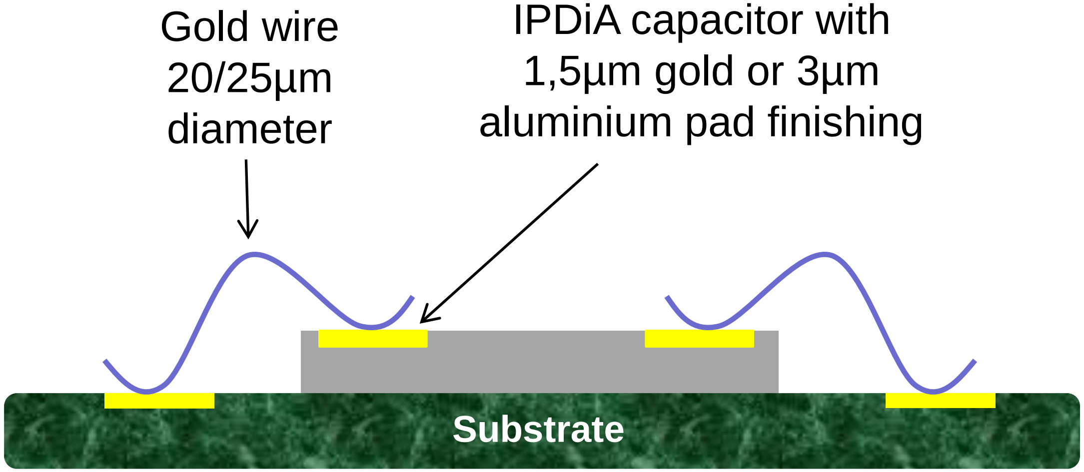
Combination of aluminum wire with aluminum pad is recommended if T >150° C to avoid Purple Plague issue !

Wedge bonding – Gold wire



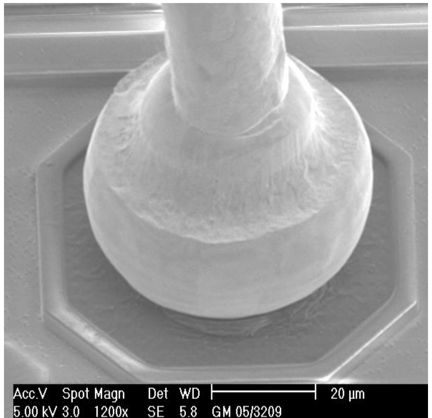


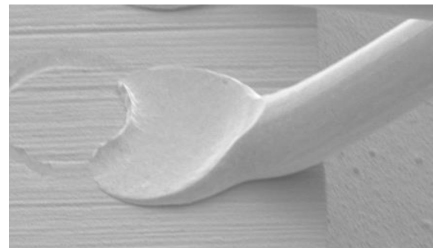
Bonding process : Wedge /Gold wire	
Bonder	BJ820
Bonding Tool	FP45B-TI-2015-1.00-CGM
Wire	Heraeus Au AW14 (>17cN et 0,5-3%)
US	20 – 30% (420 -600 mW)
Force	20 – 30cN
Bonding time	20ms
Deformation	25 – 35%
Temperature	115°c



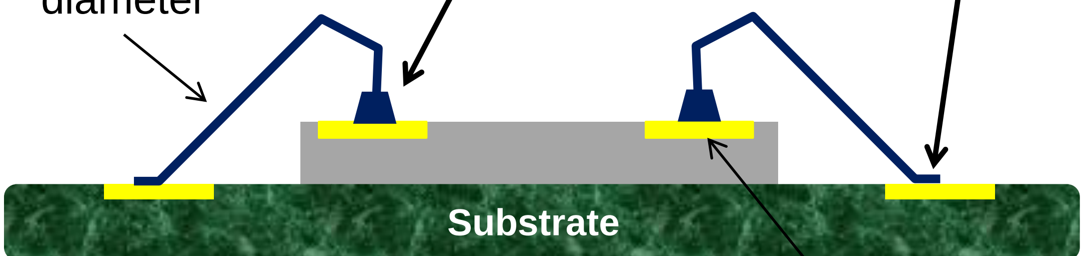
Combination of gold wire with gold pad is recommended if T >150° C to avoid Purple Plague issue !

Ball bonding – Gold wire





Gold wire
20/25µm
diameter

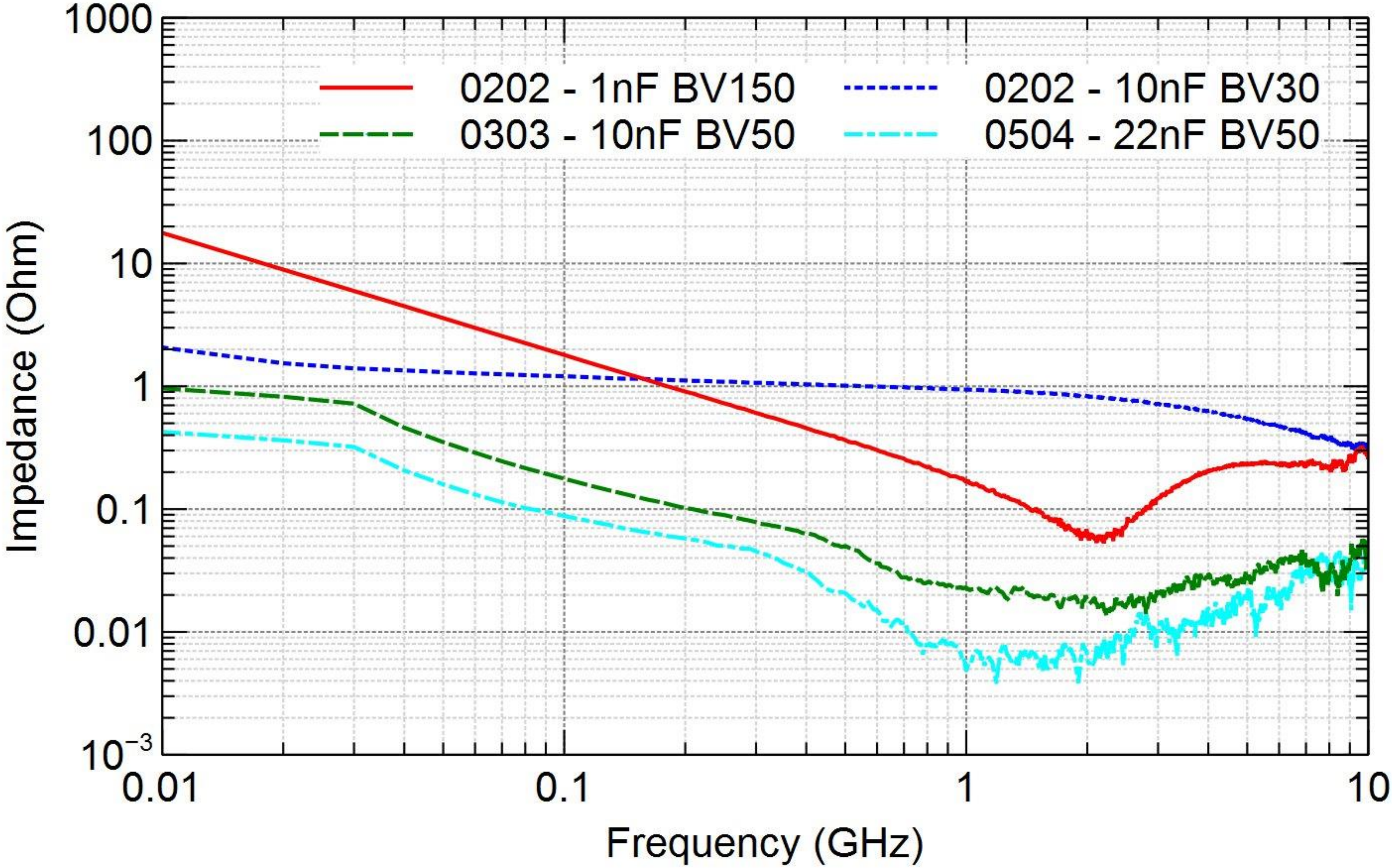


Combination of gold wire with gold pad is recommended if T >150° C to avoid Purple Plague issue !

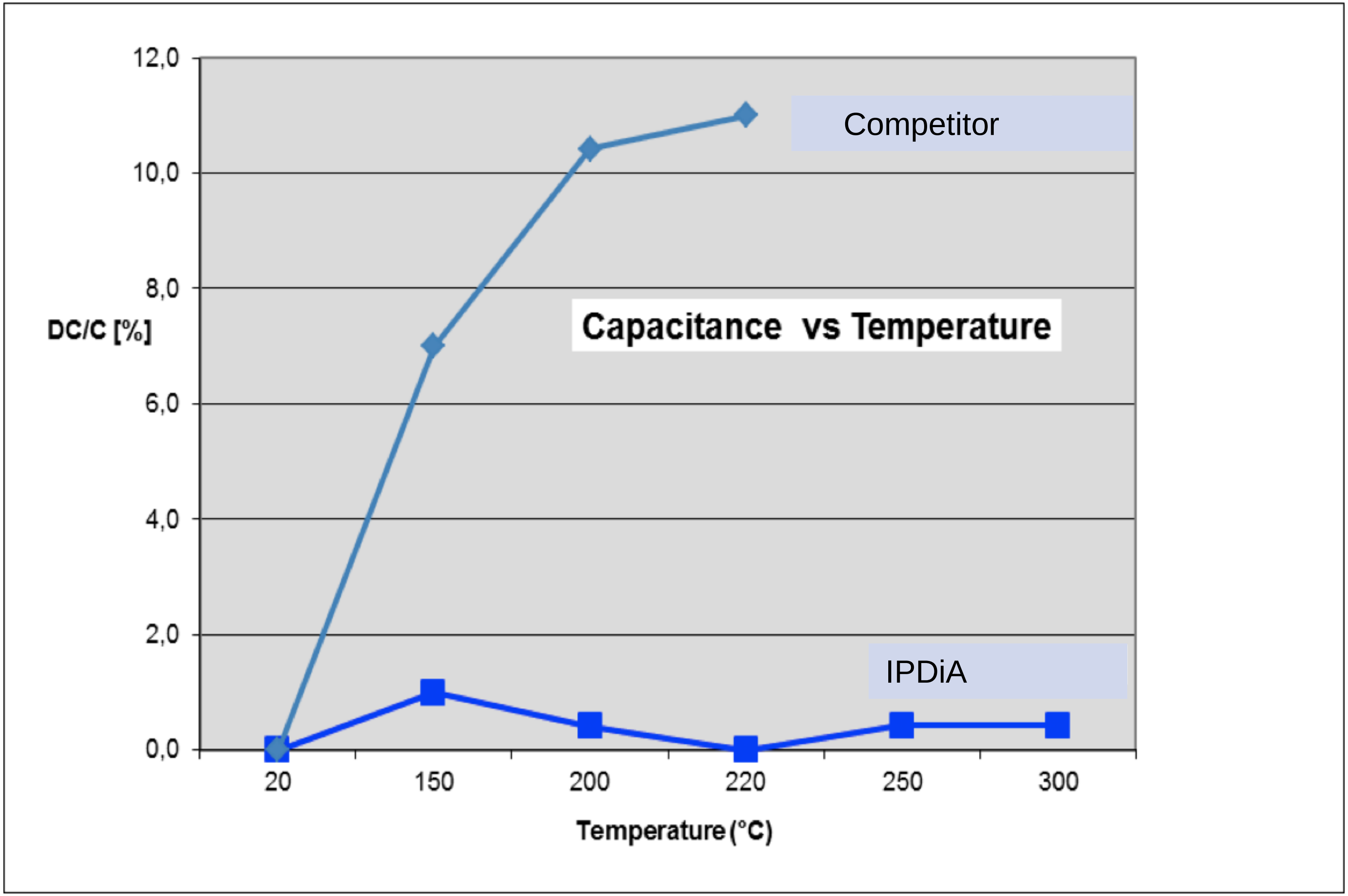
IPDiA capacitor with
1,5µm gold or 3µm
aluminum pad finishing

Ball bonding /Gold wire	
Bonder	5810 BONDTEC
Bonding Tool	UTS-38HG-AZM-1/16 16mm (SPT)
Wire	Heraeus HD2 (>7cN,2-6%)
US	215 – 230 mW
Force	30 – 40 g
Bonding time	24 ms
Temperature	125°c

RF performances

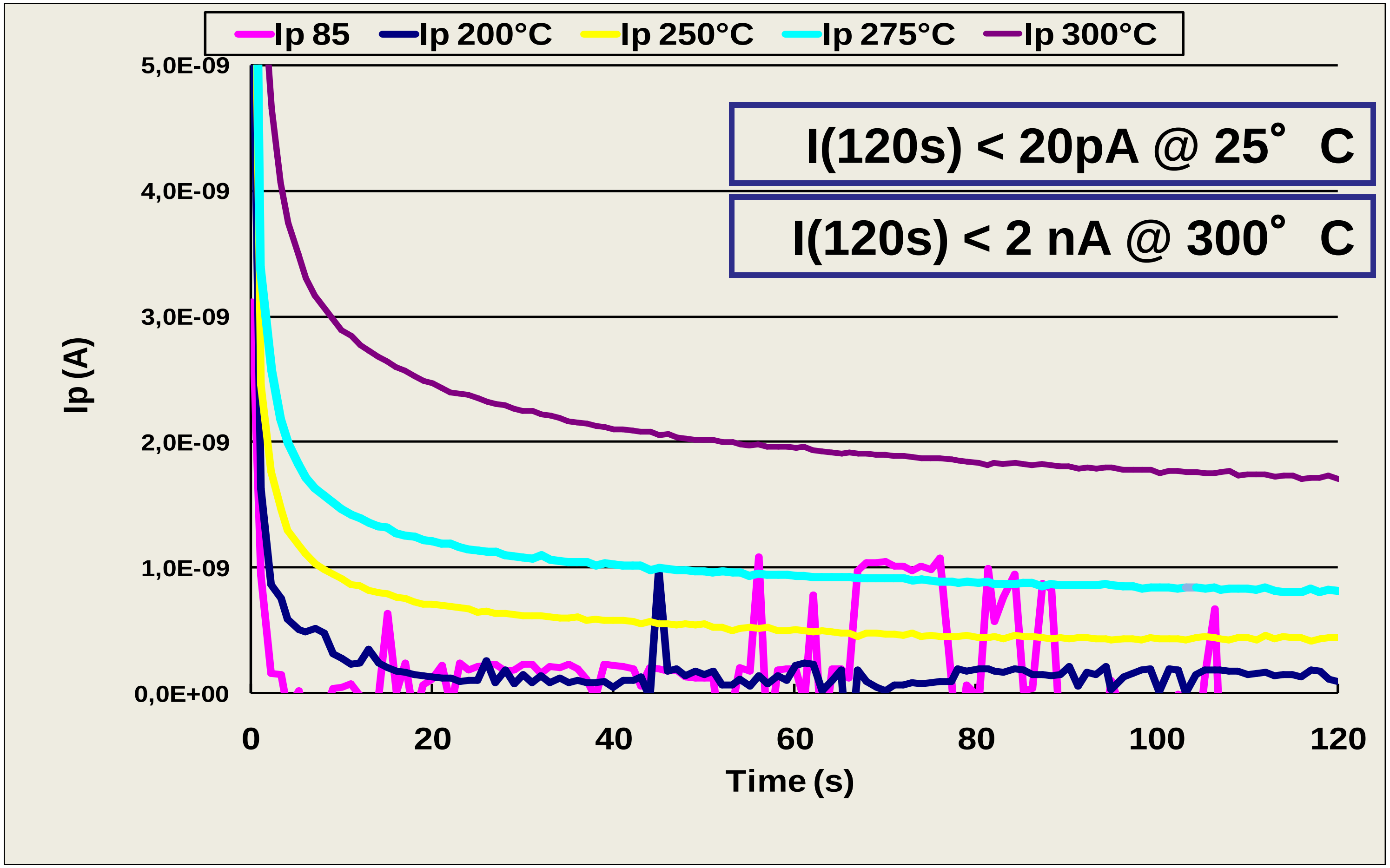


Temperature behaviour of Si Caps

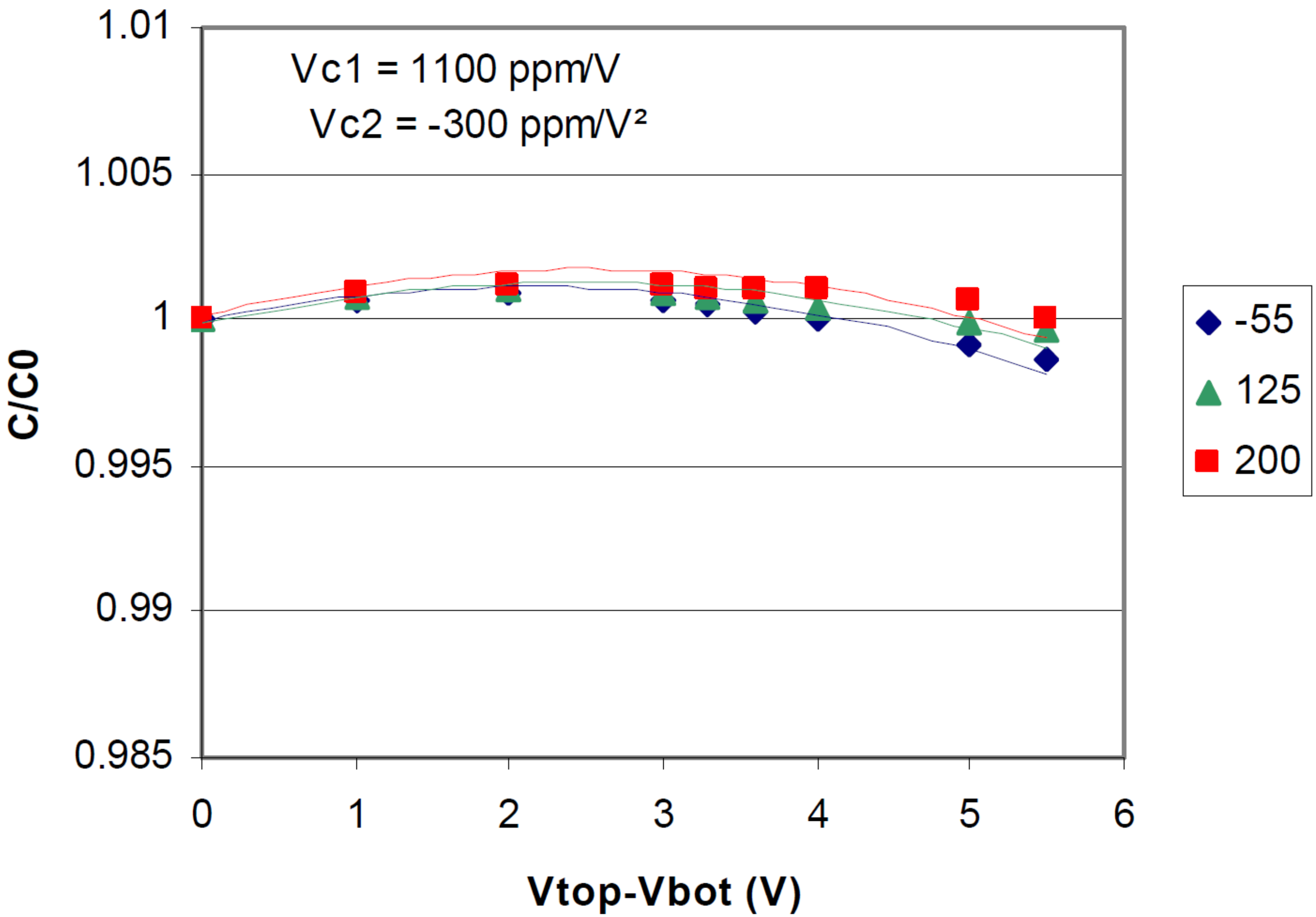


DC leakage current at high Temperature

C= 100nF (Amps @ 3V)



Capacitance dependance on DC bias and temperature



Performances

- Low leakage current <1nA/mm²
- Excellent temperature and voltage linearity
- High volume efficiency
- Low ESR , low ESL

IPDiA Capacitor failure mode

- Dielectric wear out accelerated under high voltage or high temperature conditions , getting visible by an increase of the leakage current to end up with a short .
- The main sensitivity or « degradation » factor is the increase of electrical field (voltage).
- There is no early failure
- The lifetime of 100 nF 0605 capacitor exceeds 18 000 hours at 200 ° C.
- As a comparison, X8R capacitors show a useful life of 10 000 hours at 125 ° C at the rated voltage.

Lifetime: Predictive models

$$t_{bd} = A_0 \cdot \exp(E_{Ao}/kT) \cdot \exp(-\gamma \cdot E_{ox})$$

→ A_0 = time constant

→ E_{Ao} = activation energy (eV) determined from the TDDB test

→ k = Boltzmann constant (8.6 × 10-5 eV/K)

→ γ = field acceleration factor

→ E_{ox} = field across the oxide given by the ratio of the applied voltage to thickness of the dielectric

PICSHV150

Vg (V)	37℃	100℃	150℃	225℃
30	496676 years	36581 years	8022 years	1458 years
45	20090 years	1480 years	324 years	59 years
60	813 years	60 years	13 years	2.4 years
75	33 years	2.4 years	194 days	35 days

Lifetime predictions at different values of stress voltage and temperature using the TDDB E-model at 0.1% cumulative failure

Take away on reliability

- IPDiA technology is facing numerous success stories with the high reliability top players .
- This technology is featuring a composite ONO dielectric
  - Si_3N_4 boost capacitance density
  - Thermal oxide barriers enhance leakage and wear-out performance
- Wear out of the Capacitor is similar to CMOS
  - Failure mechanisms are similar to FET gate
  - Predictive reliability models (tddb) are available accounting for T and V derating
- EFR screening is part of the wafer test setup
  - Does not require component burn-in
- No ageing
- No catastrophic failures
- Not sensitive to moisture

Reliability results

Stress test	Abbr.	Stress Conditions	Stress Duration	Results
Life time at V use	TDDB	3T° & 3 Voltages		> 10 years @ 100°C
Failure in Time	FIT	150°C		< 1 @225°C
High Temperature Operational Life	HTOL	150°C,Vuse	1008 hrs	0 failures
Thermo-mechanical cycling	TC	-65°C /+150°C	500 cycles	0 failures
High Temperature Storage Life	HTSL	150°C,unbiased	1008 hrs	0 failures
Unbiased Highly Accelerated Stress Test	UHAST	Preconditioning MSL3 260°C, 85% RH, unbiased	1056 hrs	0 failures
Temperature Humidity Bias Life Time	THB	85°C,85%RH,V use	1008 hrs	0 failures
Metallization Stress voiding		200°C	168 hrs	0 failures
Stress Migration(stress induced voiding)		200°C	904 hrs	0 failures
Corrosion	THNB		168 hrs	0 failures
Passivation integrity		45°C, H_3PO_4 or electroless NiAu	40 mn	0 failures

Conclusion

- The need for high-power and high frequency transistors is increasing
- The miniaturization of the RF power modules is a must
- The WB Silicon Capacitor is providing performiniaturization : a combination of high performance and power efficiency thanks to low parasitics and high capacitance in a very small package on top of an outstanding reliability .

Thank you for your attention !

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