High Efficiency Power Solutions by Chip Embedding
3D Integration

- Stacked & PoP
- Embedded
- TSV
Embedded Technology Introduction

**Embedded Components**

- **Passive**
  - Formed
  - Placed
    - Resistors
    - Capacitors

- **Active (Die)**
  - Wafer Level Embedded Die
  - Embedded Die in Substrate
    - FOWLP is based on a reconfigured molded wafer infrastructure
    - Embedded die in package is based on a PCB type of panel infrastructure

Materials are added to the printed circuit structure to create the passive element.
## Embedded Die Substrate Technology

**aEASI - Embedded Active System Integration**

<table>
<thead>
<tr>
<th>Type</th>
<th>Schematics</th>
<th>Content</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>aEASI</td>
<td><img src="image" alt="Schematic" /></td>
<td><strong>EAP - Embedded Active Package</strong>&lt;br&gt;Lead Frame based single or multi dies embedded in organic laminate material</td>
<td>1RDL 1Die passed reliability&lt;br&gt;3RDL 3Die mass production</td>
</tr>
</tbody>
</table>

**MOSFET**<br>3.4x3.0 mm²

**DC/DC Module**<br>4.5x6.6 mm²
a-EASI Product: DC/DC Converter

- Package: 6.65 x 4.55 x 0.8 mm³, 38L
- Chip Information: 2 MOSFETs + 1 Driver Chip
- Max. average current: 60 A
- Input Voltage range: 4.5 V to 16 V
- Fast switching > 750 kHz
- Power up Blade Server
Die Attach on L/F - TLPB

Transient Liquid Phase Bonding

Die Bond preparation on Die side

TLPB process

Die Bond on Lead Frame

Bumps stay solid until 280 °C is reached

High Temp. Pressure

Die Bond preparation on Die side

TLPB process

Die Bond on Lead Frame
Process Flow

1. Die Attach
2. Lamination
3. Lase Drill
4. Plating
5. Pattern
6. S/M
7. ENIG
8. Laser Marking
9. Solder
10. Printing
11. Singulation
Embedded Power Module Manufacturing

- Capacity & Yield
  - Yield = 97.6% in May ’16. Targeting 99% in Q4 ’16.
    - Important because of 3 KGD are embedded per device
  - Capacity of 3.3M unit/month (5x6 mm) today.
  - More than 40 M units delivered
aEASI - 2nd Generation (P2 Structure)

- Support BGA, QFN foot print
- Marking on Solder Mask
- Compatible with SMD process

Cavity Lead Frame
- Avoid die crack risk
- Uniform via depth for better laser & plating process control

Ag Sintering bond
- Compatible with conventional bonder
aEASI - P2 Results Patent pending

Die attach

Lamination

Laser drill

Plating & Patterning

S/M, Marking, Singulation

X-Ray result
Embedded Die Power Module

**Advantages**

- Smaller & Thinner package
- Excellent Thermal Dissipation
  - 2 sides cooling areas
- Excellent Electrical Performance
  - μ-via for Gate and Source, full surface Drain
  - Low resistance & inductance, good shielding
- Enhanced Reliability

**Markets**

- Power Devices, MOSFET
- DC/DC Converter Modules
- Fast switching Power & IGBT
Power Die - Reliability

Power Electronic Packages

- Al wire
  - Crack propagates through Al wire matrix
  - Increases electrical/thermal resistance

- Soft Solder
  - Crack formation in solder volume
  - Increases thermal / electrical resistance

Embedded Power Packages

- µ-via
  - Copper filled micro vias on Cu die pad
  - No crack expected

- TLPB / Ag Sintering
  - High melting point > 300°C
  - Stable against thermal stress
## Reliability Tests

<table>
<thead>
<tr>
<th>Test description</th>
<th>Abbr.</th>
<th>Condition</th>
<th>Readout</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-Conditioning J-STD-020D</td>
<td>PC</td>
<td>MSL3, 3x260°C, Reflow</td>
<td></td>
<td>Pass</td>
</tr>
<tr>
<td>Biased Highly Accelerated Stress Test JESD22 A110</td>
<td>HAST</td>
<td>Ta=130°C RF=85%</td>
<td>0 h precon 96 h</td>
<td>Pass</td>
</tr>
<tr>
<td>Temperature Cycling JESD22 A104</td>
<td>TC</td>
<td>T = - 55°C to 150°C</td>
<td>0 c precon 500c 1000c</td>
<td>Pass</td>
</tr>
<tr>
<td>High Temperature Storage Life JESD22 A103</td>
<td>HTSL</td>
<td>Ta = 150°C</td>
<td>0 h precon 168 h 500 h 1000 h</td>
<td>Pass</td>
</tr>
<tr>
<td>High Temperature Operating Life JESD22 A108</td>
<td>HTOL</td>
<td>Ta = 125°C Tj = 150°C</td>
<td>0 h 168 h 500 h 1000 h</td>
<td>Pass</td>
</tr>
<tr>
<td>Power Temperature Cycling JESD22 A105</td>
<td>PTC</td>
<td>T = - 40°C to 125°C</td>
<td>0 c precon 500c 1000c</td>
<td>Pass</td>
</tr>
</tbody>
</table>
PMIC Package Comparison

Standard PQFN Types
• PQFN 6x6 mm² Cu Clip
• PQFN 6x6 mm² Cu Wire Bond

Embedded Die Packages
• aEASI 4.5x6 mm²
• aEASI 4.5x6 mm² cavity
  Patent pending
PMIC Comparison - Thermal Resistance

Thermal Performance
Theta Jα simulated

<table>
<thead>
<tr>
<th></th>
<th>Theta Jα [°C/W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PQFN (Cu Clip)</td>
<td>32</td>
</tr>
<tr>
<td>PQFN (WireBond)</td>
<td>33</td>
</tr>
<tr>
<td>aEASI (P1)</td>
<td>31</td>
</tr>
<tr>
<td>aEASI Cavity (P2)</td>
<td>29</td>
</tr>
</tbody>
</table>

Thermal Performance
Theta JTop Data Sheets

<table>
<thead>
<tr>
<th></th>
<th>Theta JTop [°C/W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PQFN (Cu Clip)</td>
<td>20</td>
</tr>
<tr>
<td>PQFN (WireBond)</td>
<td>25</td>
</tr>
<tr>
<td>aEASI (P1)</td>
<td>4</td>
</tr>
<tr>
<td>aEASI Cavity (P2)</td>
<td>2</td>
</tr>
</tbody>
</table>
PMIC Comparison - Electrical Performance

**Resistance**

- PQFN (Cu clip): 15.00 mOhm
- PQFN (Cu wire): 34.15 mOhm
- DrBlade 2.5 (P1): 0.59 nH
- DrBlade 2.5 with Cavity (P2): 0.56 nH

**Inductance**

- PQFN (Cu clip): 0.48 nH
- PQFN (Cu wire): 0.37 nH
- DrBlade 2.5 (P1): 0.02 nH
- DrBlade 2.5 with Cavity (P2): 0.02 nH
Via Resistance & Inductance

• Resistance is analyzed at 0 Hz.
• Inductance is analyzed at 100 MHz.
• Conclusion: More via in parallel to share the current density introduce lower R & L interconnection
Electrical & Thermal Performance

Power Efficiency

Output current (A)

60%  65%  70%  75%  80%  85%  90%  95%  100%

- aEASI P1
- aEASI P2
- PQFN (wire)
- PQFN (Cu Clip)

LSMOS
Design Rule

- Detail design rule is available today for customer design study

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Normal</th>
<th>Advance</th>
<th>Prototype</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Die Pad Size</td>
<td>120</td>
<td>110</td>
<td>100</td>
</tr>
<tr>
<td>B</td>
<td>Die Pad Pitch</td>
<td>180</td>
<td>150</td>
<td>135</td>
</tr>
<tr>
<td></td>
<td>Die Pad Material (Cu Thickness)</td>
<td>5</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>C</td>
<td>Via Diameter (Top Diameter)</td>
<td>70</td>
<td>60</td>
<td>50</td>
</tr>
<tr>
<td>D/E</td>
<td>Line width/space</td>
<td>60/60 *35um Cu</td>
<td>40/40 *15um Cu</td>
<td>35/35 *12um Cu</td>
</tr>
<tr>
<td>RDL Layer</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Via aspect ratio</td>
<td>1.1</td>
<td>1.2</td>
<td></td>
</tr>
</tbody>
</table>
Embedding Benefits

- Smaller Outline
- Lower Thickness
- Electrical Performance
  - Shorter Tracks
  - Lower Resistance & Inductance
  - Shielding
- Thermal Performance
  - More Cooling Areas
- Less Delamination (similar materials)
- Enhanced Reliability
- Less Plagiarism
Embedded packaging business model

- Foundry
- Customer
- Pre Ass’y Bump, Grind, Dice, Sort
- Embedding in Substrate
- Module Final Test
- Component Test
- Module Assembly
- OSAT Package Assembly
- Final Test
- ASE GROUP
Summary

- Embedded Components can have more and more important benefits than smaller outline
- Embedded Power Modules show advantages in Thermal and Electrical Performance
- ASE brought aEASI – Embedded Die Power Modules to HVM
- Next Gen. aEASI shows enhanced manufacturability and flexibility
Thank You

www.aseglobal.com