



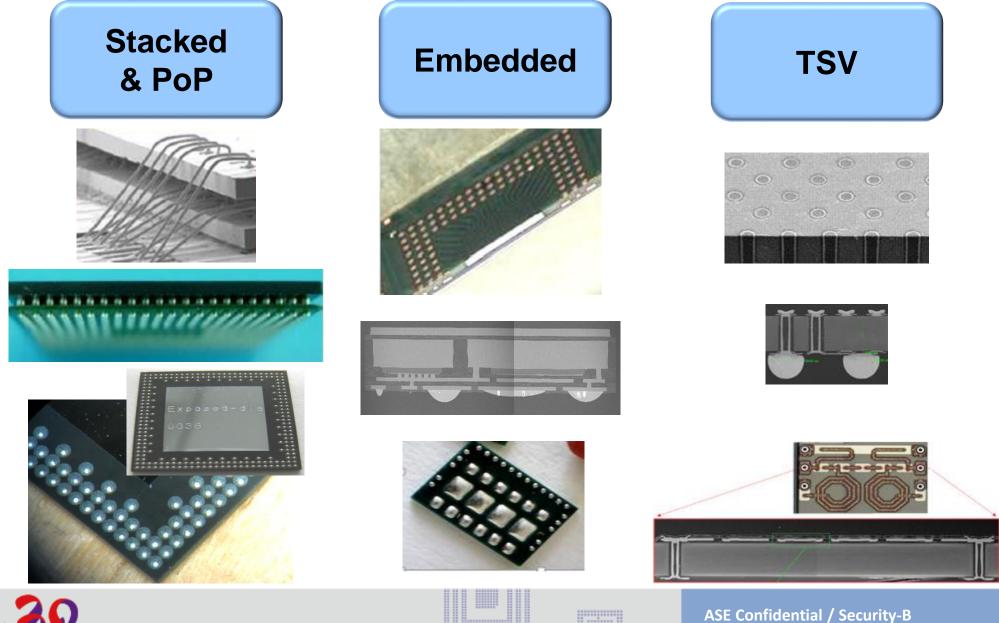
### High Efficiency Power Solutions by Chip Embedding

Dr. Kay Essig ASE June, 2016



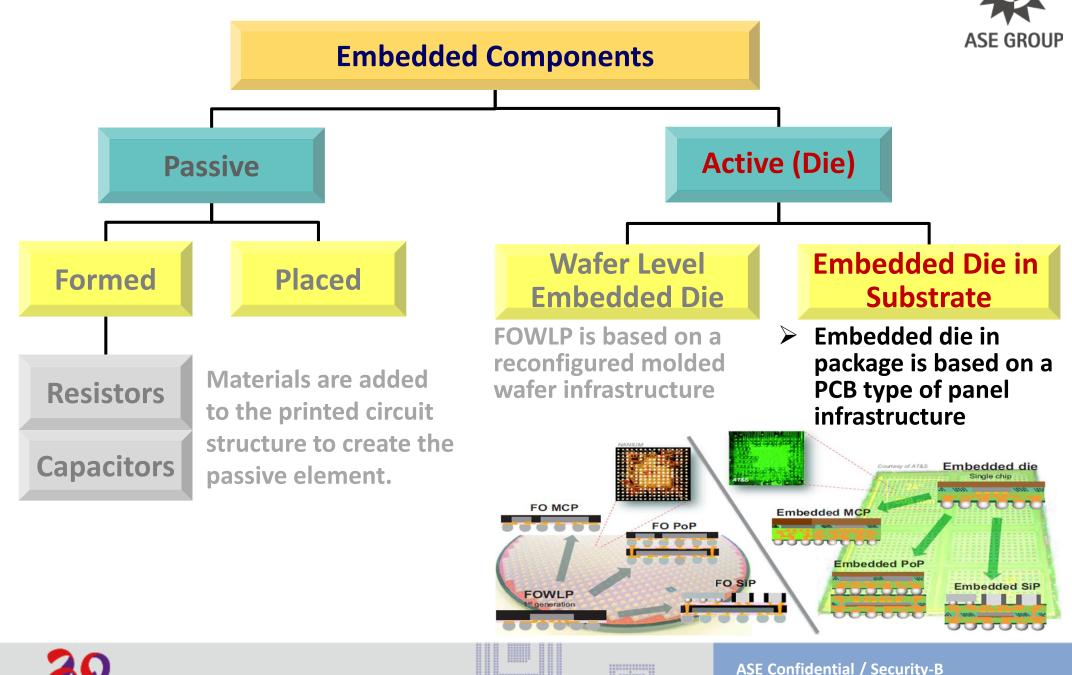
### **3D Integration**





1

### **Embedded Technology Introduction**



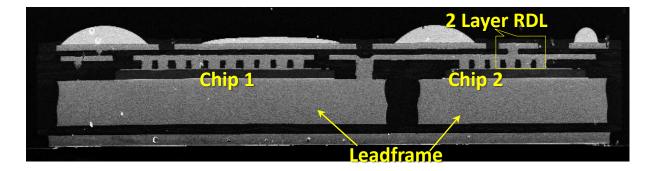
2

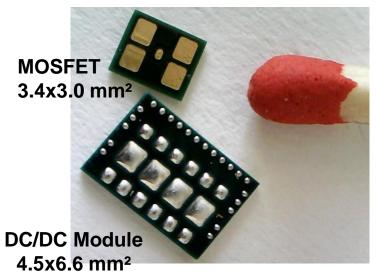
## **Embedded Die Substrate Technology**



### • aEASI - Embedded Active System Integration

Туре	Schematics	Content	Status	
aEASI		EAP - Embedded Active Package Lead Frame based single or multi dies embedded in organic laminate material	1RDL 1Die passed reliability 3RDL 3Die mass production	



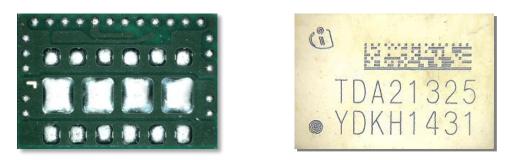




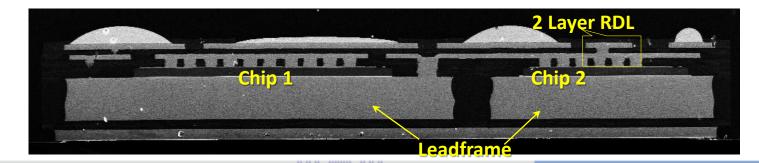


## a-EASI Product: DC/DC Converter





- Package: 6.65 x 4.55 x 0.8 mm<sup>3</sup>, 38L
- Chip Information: 2 MOSFETs + 1 Driver Chip
- Max. average current: 60 A
- Input Voltage range: 4.5 V to 16 V
- Fast switching > 750 kHz
- Power up Blade Server



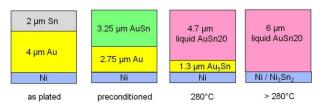


## **Die Attach on L/F - TLPB**



### **Transient Liquid Phase Bonding**

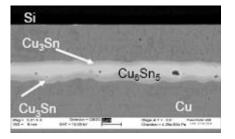
Bumps stay solid until 280 °C is reached



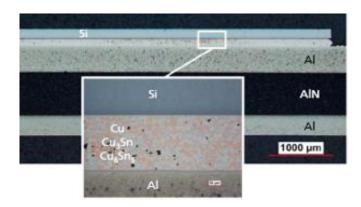
Die Bond preparation on Die side



TLPB process



#### **Die Bond on Lead Frame**

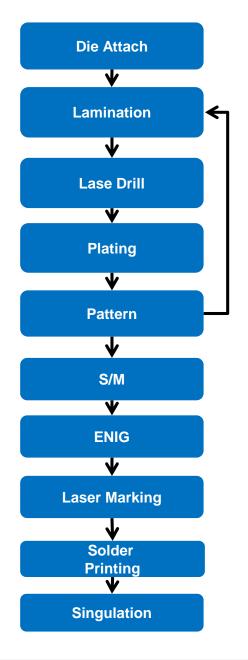


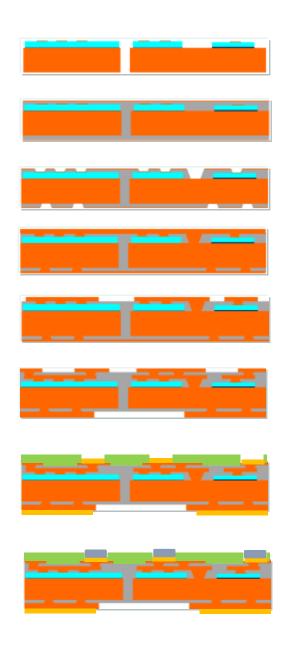


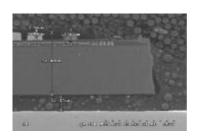


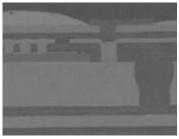


### **Process Flow**



















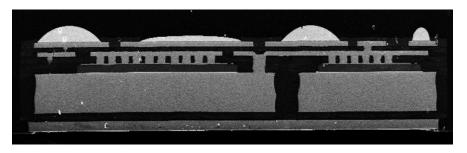
# **Embedded Power Module Manufacturing**

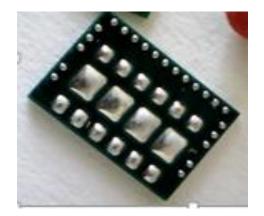


### • Capacity & Yield

- Yield = 97.6% in May '16. Targeting 99% in Q4 '16.
  - Important because of 3 KGD are embedded per device
- Capacity of 3.3M unit/month (5x6 mm) today.
- More than 40 M units delivered







ASE Confidential / Security-B © ASE Group. All rights reserved.

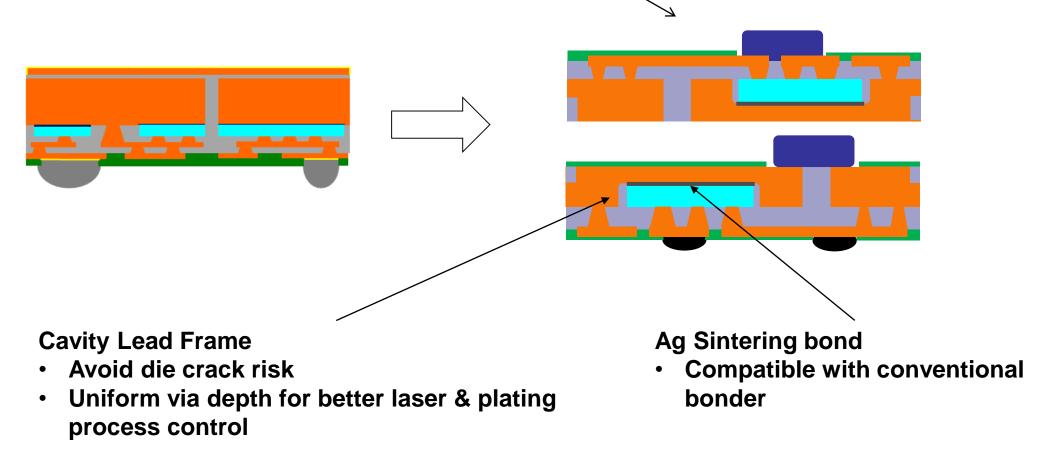




## aEASI - 2<sup>nd</sup> Generation (P2 Structure) Patent pending



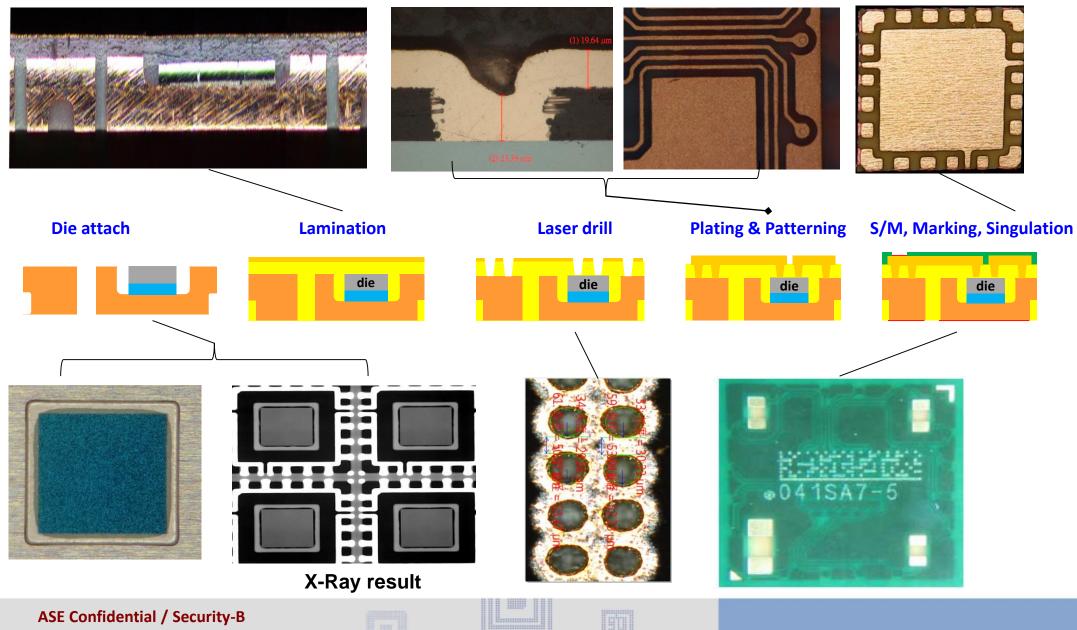
- Support BGA, QFN foot print
- Marking on Solder Mask
- Compatible with SMD process





### aEASI - P2 Results Patent pending





© ASE Group. All rights reserved.

## **Embedded Die Power Module**

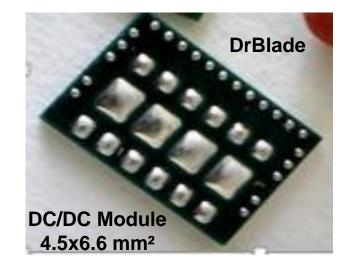


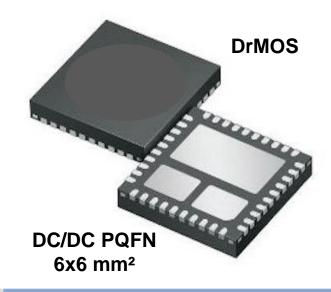
### > Advantages

- Smaller & Thinner package
- Excellent Thermal Dissipation
  - 2 sides cooling areas
- Excellent Electrical Performance
  - µ-via for Gate and Source, full surface Drain
  - Low resistance & inductance, good shielding
- Enhanced Reliability

### Markets

- Power Devices, MOSFET
- DC/DC Converter Modules
- Fast switching Power & IGBT

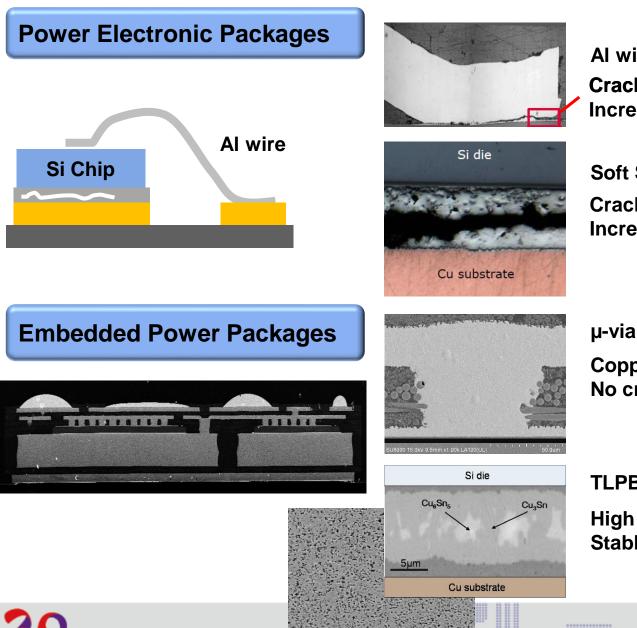






### **Power Die - Reliability**





#### Al wire

**Crack propagates through AI wire matrix** Increases electrical/thermal resistance

#### Soft Solder

Crack formation in solder volume Increases thermal / electrical resistance

Copper filled micro vias on Cu die pad No crack expected

**TLPB / Ag Sintering** 

High melting point > 300°C Stable against thermal stress

### **Reliability Tests**





Test description	Abbr.	Condition	Readout	Result
Pre-Conditioning J-STD-020D	РС	MSL3, 3x260°C, Reflow		Pass
Biased Highly Accelerated	HAST	Ta=130°C RF=85%	0 h precon	Pass
Stress Test JESD22 A110			96 h	Pass
Temperature Cycling	ТС	T = - 55°C to 150°C	0 c precon	Pass
JESD22 A104			500c	Pass
			1000c	Pass
High Temperature	HTSL	Ta = 150°C	0 h precon	Pass
Storage Life			168 h	Pass
JESD22 A103			500 h	Pass
			1000 h	Pass
High Temperature Operating	HTOL	Ta = 125°C Tj = 150°C	0 h	Pass
Life JESD22 A108			168 h	Pass
			500 h	Pass
			1000 h	Pass
Power Temperature Cycling	РТС	T = - 40°C to 125°C	0 c precon	Pass
JESD22 A105			500c	Pass
			1000c	Pass

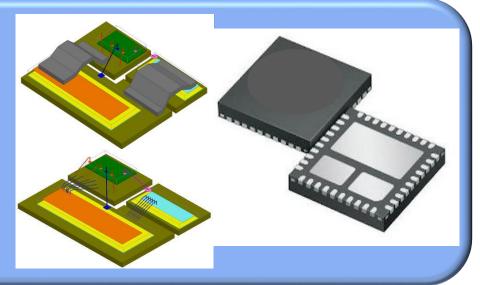


### **PMIC Package Comparison**



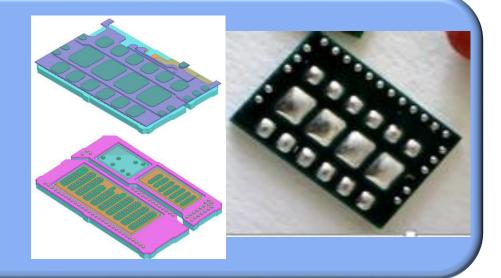
### **Standard PQFN Types**

- PQFN 6x6 mm<sup>2</sup> Cu Clip
- PQFN 6x6 mm<sup>2</sup> Cu Wire Bond



### **Embedded Die Packages**

- **aEASI** 4.5x6 mm<sup>2</sup>
- aEASI 4.5x6 mm<sup>2</sup> cavity
  Patent pending

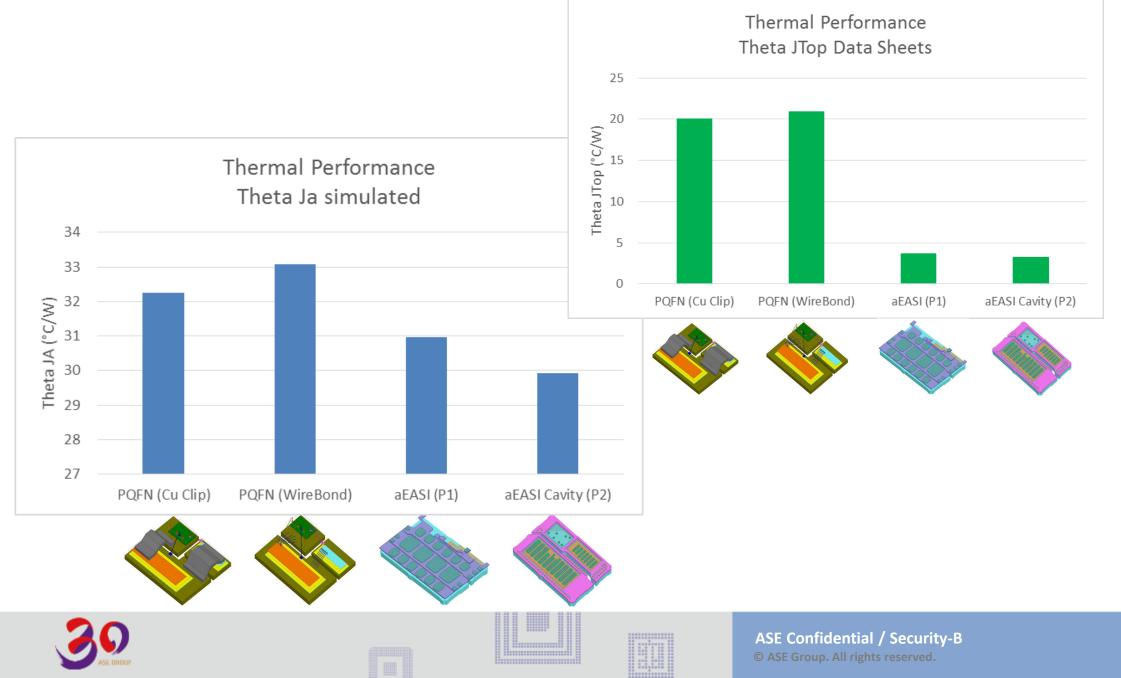




ASE Confidential / Security-B © ASE Group. All rights reserved.

### **PMIC Comparison - Thermal Resistance**





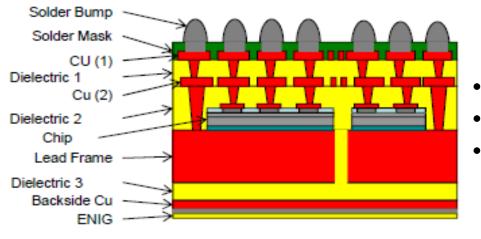
### **PMIC Comparison - Electrical Performance**





### Via Resistance & Inductance

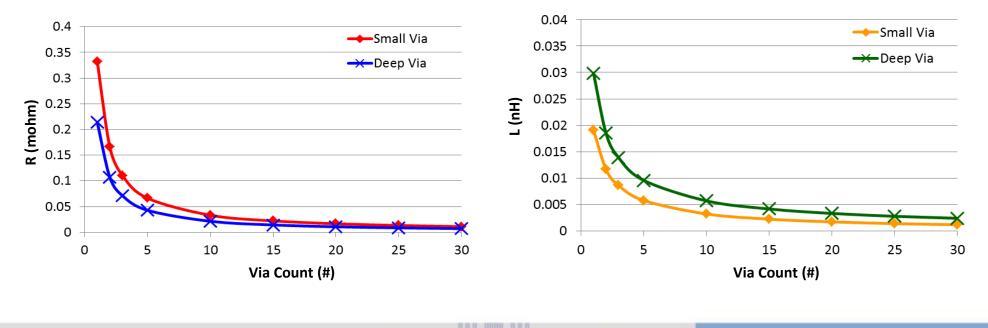




aEASI 4 layers Structure

### Resistance is analyzed at 0 Hz.

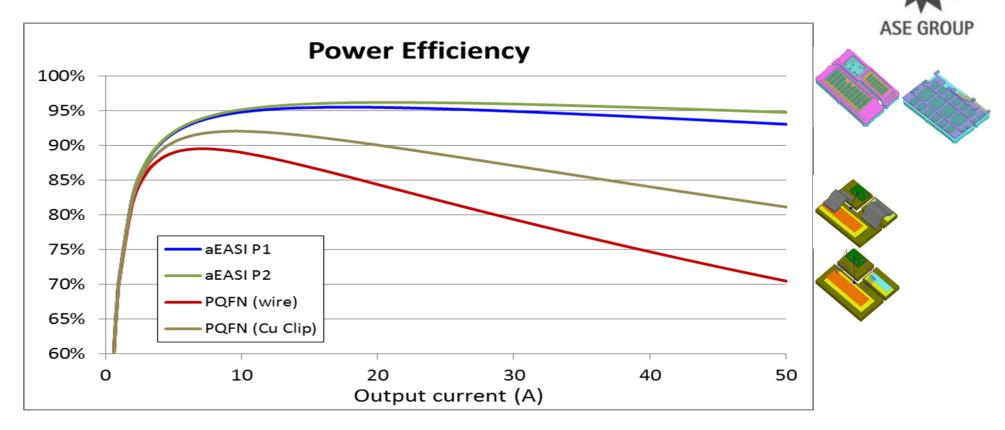
- Inductance is analyzed at 100 MHz.
- Conclusion: More via in parallel to share the current density introduce lower R & L interconnection

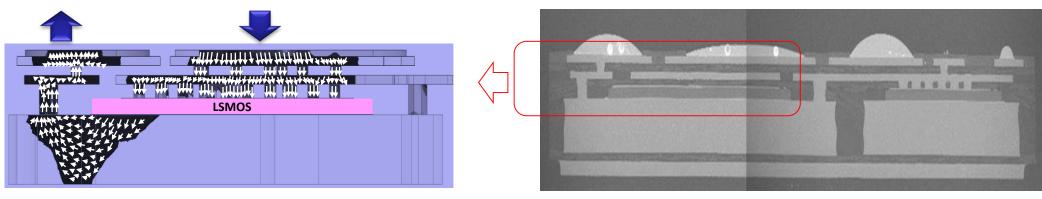


**ASE Confidential / Security-B** 

© ASE Group. All rights reserved.

## **Electrical & Thermal Performance**





#### ASE Confidential / Security-B

© ASE Group. All rights reserved.





### **Design Rule**



- $E \rightarrow e$
- Detail design rule is available today for customer design study

Unit: um

Symbol	Description	Normal	Advance	Prototype
А	Die Pad Size	120	110	100
В	Die Pad Pitch	180	150	135
	Die Pad Material (Cu Thickness)	5	4	3
С	Via Diameter (Top Diameter)	70	60	50
D/E	Line width/space	60/60 *35um Cu	40/40 *15um Cu	35/35 *12um Cu
	RDL Layer	2		
	Via aspect ratio 1.1		.1	1.2

**ASE Confidential / Security-B** © ASE Group. All rights reserved.

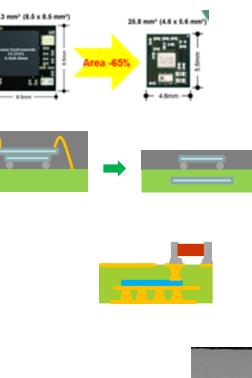


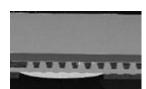


## **Embedding Benefits**

- Smaller Outline
- Lower Thickness
- Electrical Performance
  - Shorter Tracks
  - Lower Resistance & Inductance
  - Shielding
- Thermal Performance
  - More Cooling Areas
- Less Delamination (similar materials)
- Enhanced Reliability
- Less Plagiarism





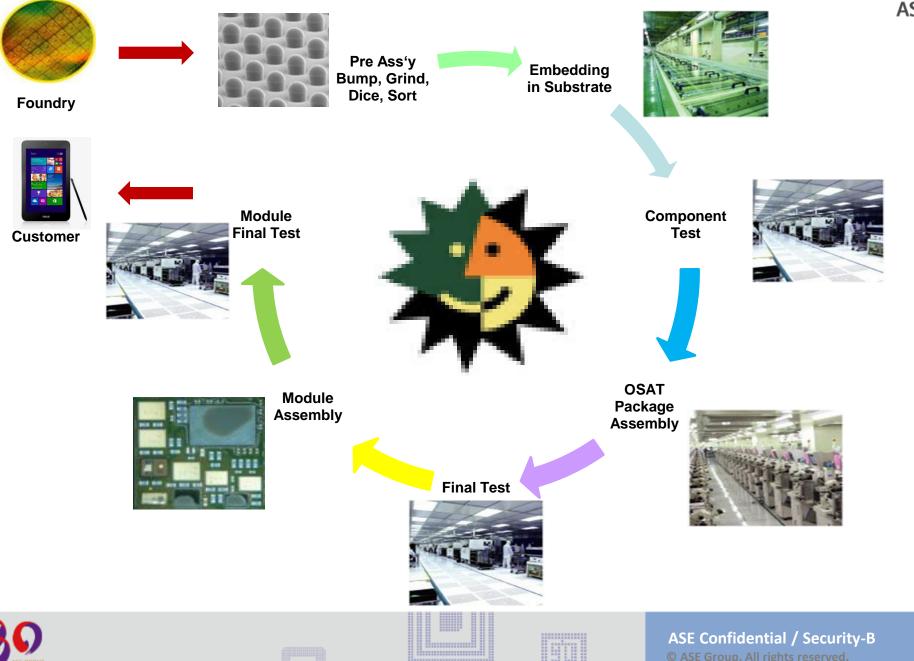






### Embedded packaging business model





### Summary



- Embedded Components can have more and more important benefits than smaller outline
- Embedded Power Modules show advantages in Thermal and Electrical Performance
- ASE brought aEASI Embedded Die Power Modules to HVM
- Next Gen. aEASI shows enhanced manufacturability and flexibility





## **Thank You**

www.aseglobal.com



**ASE Confidential / Security-B** © ASE Group. All rights reserved.