FEA-Based Thermal-Mechanical Design Optimization for DBC Based Power Modules

Yang Xu[1], Zelin Xu[2], Jeffrey W. Eischen[2], Douglas Hopkins[1]
1 Department of ECE, NCSU; 2 Department of MAE, NCSU

Abstract— DBC (direct bonded copper) is used as a standard power module substrate by industry. In this paper, the behavior of the thermal spreading for DBC based power modules is studied. To enhance thermal performance, design guide for choosing the optimized layer thickness and substrate size is discussed. Moreover, mechanical failures for difference materials in DBC substrate are briefly summarized. Based on these failure mechanisms, an objective function is used to develop an FEA (finite elements analysis) based optimization model for minimizing thermal-mechanical stress. The optimization platform converges and an optimized DBC substrate was generated successfully.

Keywords—power module, DBC, thermal management, mechanical failure, CTE mismatch, optimization design, FEA

I. INTRODUCTION

Power semiconductor modules are essential parts in power electronic systems. They can integrate power chips, circuits, drives and protection functions into one system with electrically insulated cooling. The recent development of new wide bandgap (WBG) power devices such as SiC and GaN transistors enables faster switching speed, higher current or voltage handling capability, which further increases the thermal, mechanical, electrical and power density demand for power modules design.

Temperature increase due to power semiconductor heat dissipation affects the device performance and reliability significantly. On resistance, switching time are all influenced by temperature. Of particular concern is the non-linear increase in failure rate:

$$F = Ae^{-E_A/KT} \tag{1}$$

A is a constant, E_A is activation energy (eV), K is Boltzmann constant; T is junction temperature [1, 2]. Detriments to the reliability include mechanical stresses induced at interconnects between metal, electrically insulating material and semiconductor due to elevated temperature.

For convenience of thermal analysis, the lump parameter spreading angle thermal resistance model is widely used by many package engineers. However, there are limits for this approach when significant lateral thermal spreading occurs, and it can only provide good estimation for simple single layer geometries [3]. More advanced 3D-FEA simulation approach must be applied for thermally-mechanically optimized DBC substrate design.

Fig.1 and 2 show a typical multi-chip power module and the vertical layer structure of DBC substrate. The bottom layer of copper is usually placed on to a base plate which is mounted on a heat sink. The top copper conducts electrical current and the bottom copper is to balance the mechanical stress under power semiconductor thermal dissipation. The elevated temperature of the power module leads to mechanical stress on the power device as well as the package due to the difference in coefficients of thermal expansion (CTE) of materials. The accumulated stress in each layer may cause power module's mechanical failure. Moreover, Due to its brittle nature, high stresses induced in the power semiconductor material could result in detrimental fracture in the die [4].

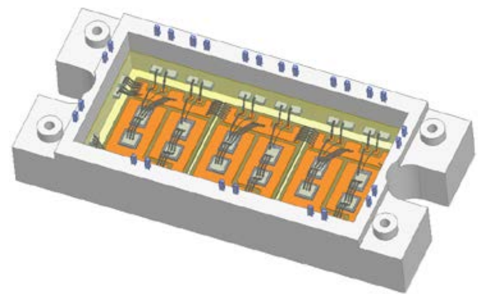

Fig. 1. DBC based power module

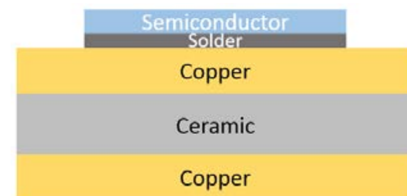

Fig. 2. Standard DBC structure

TABLE I. POWER MODULE MATERIAL PROPERTIES

Material	Thermal conductivity (w/mK)	CTE (ppm/K)	Young's Modulus (GPa)
Copper	400	17	110
Sn60Pb40	50	21	10
AlN	170	4.5	330
Alumina	27	8	300
Silicon	130	2.6	170

The fracture mechanisms of each material layers are different. For different geometries, the dominate failure layers are different. Based on geometry - fracture mechanisms relation, the mechanical design of standard DBC power module can be formulated to a multi-physics FEA based optimization problem.

II. THERMAL SPREADING

For any power module in operation, heat is conducted from a relatively small area in power semiconductor die to heatsink through a layered substrate structure in between. During the process, heat transfers not only vertically from die to heatsink but also laterally from chip to nearby area of the substrate. Heat is easier to spread out in material with higher thermal conductivity. Thus top copper layer is the most important interface for heat spreading within DBC substrate. If the copper is too thin, the cross-sectional area of heat path is small which leads to a high thermal resistance. If the copper is too thick, the heat path length is too long which leads to a high thermal resistance. Thus there exists an optimal thickness for the top copper thickness to achieve the minimal thermal resistance.

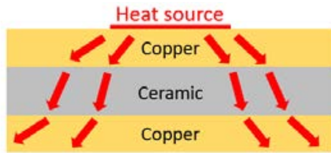

Fig. 3. Thermal spreading

To model the thermal spreading behavior with a lump parameter thermal resistance, 45° thermal spreading model was proposed by researchers. However, [3] stated those fixed angle models will introduce significant error in some conditions. In this paper, all thermal spreading is evaluated with FEA simulation.

To study the influence of top copper layer thickness to thermal resistance, FEA thermal simulation is conducted. Assuming a silicon power semiconductor chip of 5mm by 5mm by 0.12 mm is soldered on top of a 15 by 15 mm or 25 by 25mm DBC substrate. The DBC has a ceramic layer of 0.625mm (25mils). The chip dissipates 50w. The bottom side of the DBC is fixed at 20℃ degrees. The thermal resistances is simulated through sweeping the top copper thickness while keeping the bottom copper at 0.3mm (12mils) as in Fig. 3.

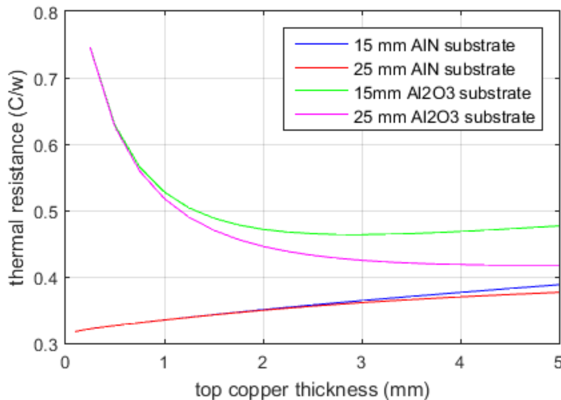

Fig. 4. thermal resistance vs. top copper thickness

For AlN substrate, the additional copper will not help the heat spreading out significantly due to the high thermal conductivity of AlN. However, for alumina DBC substrate, due to the huge difference in thermal conductivities between alumina and copper, the thermal spreading is significantly enhanced by adding top copper thickness. Only when the copper thickness is larger than about 3 to 4 mm which is unpractical for power substrate application, the thermal resistance begins to increase. By sweeping the alumina substrate size, thermal FEA simulation results indicate temperature vs substrate size and upper layer copper thickness. The substrate size or die keep out distance also influence the thermal spreading significantly.

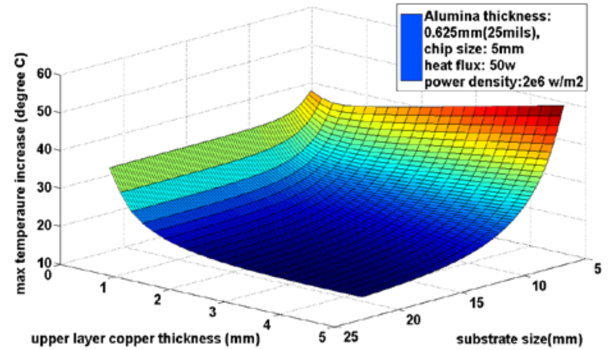

Fig. 5. Max temperature vs substrate size and top copper thickness

Thus, thermal spreading plays an important role for alumina DBC substrate thermal performance. The top copper layer thickness and substrate size needs to be carefully chosen to minimize thermal-mechanically introduced substrate failure.

III. THERMAL STRESS AND MECHANICAL FRACTURE CRITERION OF DIFFERENT MATERIALS

A. Copper Fracture

The von Mises stress is a scalar stress at which yielding is predicted to occur in ductile materials. Three-dimensional stress is illustrated in Fig.4. The von Mises stress σ' is defined as (1).

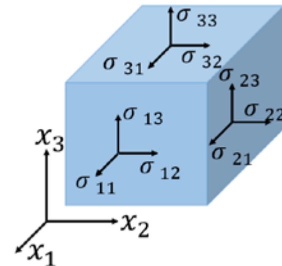

Fig. 6. 3-D Stress vector

$$\frac{1}{\sqrt{2}}\sqrt{(\sigma_{11}-\sigma_{22})^2+(\sigma_{22}-\sigma_{33})^2+(\sigma_{33}-\sigma_{11})^2+6({\sigma_{12}}^2+{\sigma_{23}}^2+{\sigma_{31}}^2)} \quad (1)$$

To determine the criterion for fracture within copper, Von Mises criterion suggests that the yielding of material begins when the von Mises stress reaches the material yielding stress. The yielding stress for copper is $200MPa$.

B. Ceramic Fracture

The measured fracture strengths of most ceramic materials are substantially lower than predicted by theory from interatomic bonding forces. This may be explained by very small and omnipresent flaws in the material that serve as stress concentration points at which the magnitude of an applied tensile stress is amplified [5]. Brittle fracture takes place without any appreciable deformation and by rapid crack propagation. The direction of crack motion is very nearly perpendicular to the direction of the applied tensile stress and yields a relatively flat fracture surface [5]. Ceramic's ability to resist fracture when a crack is present is defined as fracture toughness. The plane strain fracture toughness is

$$K_{IC} = Y\sigma\sqrt{\pi a} \tag{2}$$

Where Y is a dimensionless parameter depend on the relative geometry relation between crack and the specimen. σ is the applied stress and a is half of internal crack size. In this equation, K_{IC} is a material property, for %96 pure aluminum oxide (alumina), $K_{IC} = 3.9MPa\sqrt{m}$. Crack size is highly determined by ceramics fabrication process, here assuming half internal crack size a is $50\mu m$. Parameter Y can be calculated by equation:

$$Y(\frac{a}{w}) = \sqrt{\sec(\frac{\pi a}{w})} \tag{3}$$

Where w is the ceramics thickness. Thus σ can be calculated as a comparison stress for maximum Von Mises Stress in the ceramic to determine when ceramic layer fractures. Based on these 2 equations and the assumed crack length, the critical stress for alumina vs alumina thickness can be calculated in the following figure:

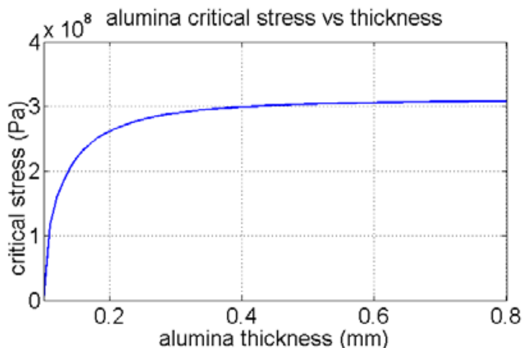

Fig. 7. Critical Stress of Alumina

The critical stress is 0 when the thickness is 0.1mm which is the crack size. This means that at the location of crack, the thick of ceramic is 0, it's already cracked at the thickness direction and cannot take any stress along the thickness.

C. Silicon Fracture

Silicon lattice is very brittle. It has a mechanical property similar to ceramic. By nature being a brittle material, moderate stress levels could result in detrimental failure such as cracking and fracture in the die. In addition, wafer processing steps such as thinning and sawing could further induce defects in the silicon die [3]. Both die size and thickness has influence on the silicon die failure stress (called silicon die critical stress in later sections) According to paper [4], the silicon die failure stress is about 400MPa for the thickness of 0.12 mm.

D. Solder Fracture

Die attach solder is a bypath for both electric current and heat flux. Tin-lead solder is still commonly used in traditional power modules. CTE mismatch between die and substrate introduces solder crack which harms the power module reliability. For the lead-tin system the solid phases are designated by α and β. α represents a solid-solution of tin and lead. For β, tin is the solvent and lead is the solute. Compared to copper and ceramics, Sn60Pb40 solder, for example, has a very small Young's modulus of 10GPa. The melting point of Sn60Pb40 is only 185°C which makes this material attractive as a low-temperature solder. Solder's mechanical strength is dependent on temperature. Book [8] shows the solder's mechanical loading capability with respect to temperature. Solder's mechanical strength decreases significantly after 120°C. For temperature within our concern, solder's mechanical strength changes less than 10% from room temperature. Thus, in this study we assume the solder's critical stress for fracture is fixed at 170MPa [6].

The interface failure such as the bondwire liftoff, solder crack and DBC delamination plays a very important role in overall package reliability. However, interface quality not only depends on geometry and material but also highly depends on process conditions such as wire bonder and reflow oven settings and environmental factors etc. Those factors can possibly be modeled in the FEA model on a case by case base. In this work, the interface failure mechanism is not modeled due to the purpose of multi-physics FEA optimization procedure development.

IV. DBC Copper Thickness Optimization

The failure mechanisms that limit the number of power cycles are caused by the coefficient of thermal expansion mismatch between the materials used in the IGBT modules. As paper [7] states the common failure mechanism for a IGBT module include: emitter bonding wire lifting failure, solder degradation, cracks in silicon die and substrate, electro-migration in bonding wires and surface degradation in emitter bonding pads. However, interface quality not only depends on geometry and material but also highly depends on process conditions such as wire bonder and reflow oven settings and environmental factors etc. Those factors can possibly be modeled in the FEA model on a case by case base. In this work, the interface failure mechanism is not modeled due to the purpose of multi-physics FEA optimization procedure development. Based on the failure mechanism mentioned in the previous sections, an optimization model can be formulated to minimize thermal-mechanical stress.

A. Design Variables

Due to the symmetry property of the geometry, only one quarter of the geometry is studied. In this case, optimization involves determining the thickness of each material layers and

substrate size for achieving the least possibility of mechanical failure. Chip size, chip thickness and solder thickness are fixed at 5 mm, 0.12 mm, 0.1 mm respectively. Substrate size, top copper thickness, bottom copper thickness and ceramics thickness are design variables in the optimization algorithm. The constraints of the design variables are listed in TABLE 2.

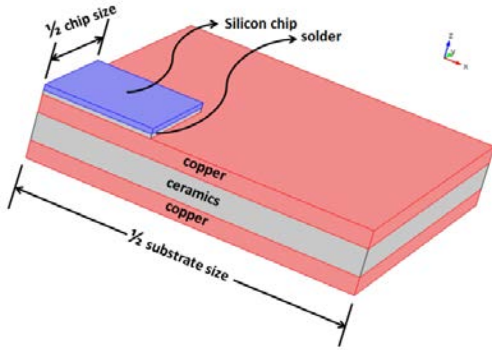

Fig. 8. DBC model for optimization

TABLE II. DESIGN VARIABLE CONSTRAINTS (IN MM)

Variables	Lower Bound	Upper Bound	Initial Value
DBC Size	6	20	15
Top Cu	0.1	1	0.4
Al_2O_3	0.1	1.2	0.625
Bottom Cu	0.1	1	0.4

For ceramic thickness, we can also add additional boundary limit based on voltage specification for high voltage module design.

B. Objective Function

The Von Mises stress criterion for material fracture to occur is summarized in (4). In order to define an objective function that takes care of all different material fracture criteria, the objective function is defined as in (5). The optimization process will minimize this function and guarantee a less than 1 value.

$$\begin{cases} \sigma'_{\mathrm{Cu_max}} > \sigma_{\mathrm{Cu_yield}} \\ \sigma'_{\mathrm{ceramic_max}} > \sigma_{\mathrm{ceramic_critical}} \\ \sigma'_{\mathrm{semiconductor_max}} > \sigma_{\mathrm{semiconductor_critical}} \\ \sigma'_{\mathrm{solder_max}} > \sigma_{\mathrm{solder_critical}} \end{cases} \quad (4)$$

$$\mathrm{Max}\begin{pmatrix} \frac{\sigma'_{\mathrm{Cu_max_top}}}{\sigma_{\mathrm{Cu_yield}}}, \\ \frac{\sigma'_{\mathrm{ceramic_max}}}{\sigma_{\mathrm{ceramic_critical}}}, \\ \frac{\sigma'_{\mathrm{semiconductor_max}}}{\sigma_{\mathrm{semiconductor_critical}}}, \\ \frac{\sigma'_{\mathrm{solder_max}}}{\sigma_{\mathrm{solder_critical}}}, \end{pmatrix} \quad (5)$$

C. Optimization Algorithm

Nelder Mead is a commonly used heuristic direct search method used for nonlinear optimization problems. It belongs to the simplex method family and sometimes is referred to as downhill simplex method. It is based on evaluating a function at the vertices of a simplex, then iteratively shrinking the simplex as better points are found until some desired bound is obtained [8]. The method does not require any derivative information which makes it possible for problems with non-smooth functions.

In many practical problems, like parameter estimation and process control, the function values are uncertain or subject to noise. Therefore, a highly accurate solution is not necessary, and may be impossible to compute. The Nelder-Mead method frequently gives significant improvements in the first few iterations and quickly produces acceptable results. This is important in applications where each run of the simulation is very expensive or time-consuming. In many numerical tests, the Nelder-Mead method succeeds in obtaining a good reduction in the function value using a relatively small number of evaluations.

D. FEA Simulation based Optimization Implementation

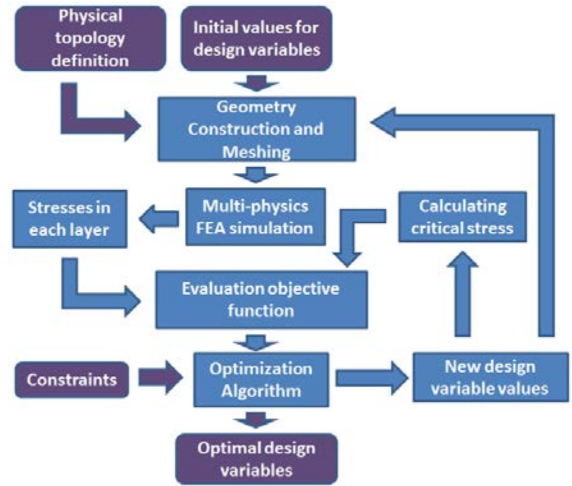

Fig. 9. FEA based Optimization Flow Chart

Based on the quarter symmetry geometry defined in Fig.8, the FEA simulation is set up in COMSOL multi-physics. The thermal stress module is applied which includes the heat transfer and solid mechanics simulation at the same time. A 25w of heat flux is applied to the top surface of the silicon chip which represents 100w applied to the total chip. The bottom of the lower copper is fixed at room temperature of 20°C. All the other surfaces are thermally insulated. No thermal convection is studied in this case. The center point of the bottom copper is mechanically fixed. Two vertical walls with chip center are also fixed mechanically.

E. *Optimization Results*

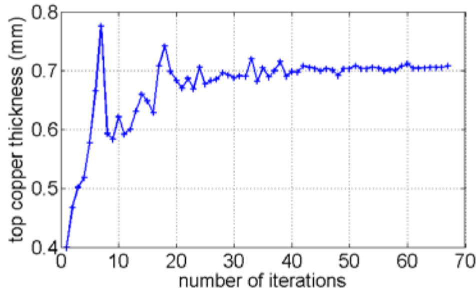

Fig. 10. Top copper thickness change during iteration

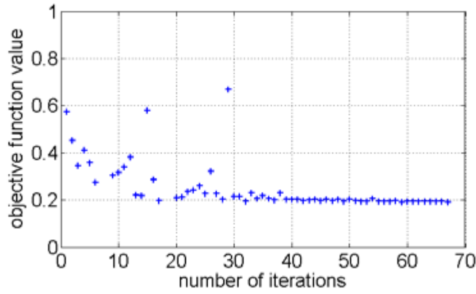

Fig. 11. Objective function change during iteration

TABLE III. OPTIMIZED VARIABLES

Design Variable	Top Cu	Bottom Cu	Ceramic	Substrate size
Opt value (mm)	0.707	0.415	0.132	12.880

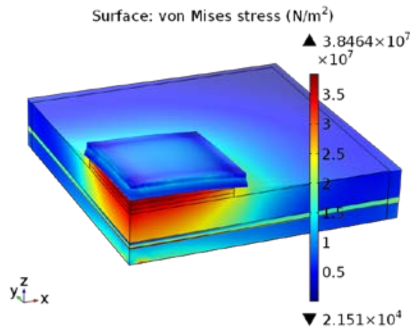

Fig. 12. Von Mises stress distribution

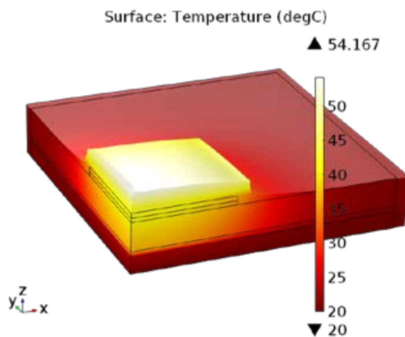

Fig. 13. Temperature distribution

V. CONCLUSION

Thermal spreading has significant impact to thermal-mechanical behavior of power substrate. DBC layer thicknesses and size can be optimized to minimize thermal stress. A methodology was developed to optimally design a power semiconductor substrate in a FEA based multi-physics environment. A basic DBC model is created and design parameters are defined. Objective function and optimization algorithm are chosen. The optimization algorithms converged to an optimum design within the design boundary condition. This methodology can be extended to the design of Power Modules for any current, voltage rating. Other design variables, objective functions and optimization algorism can also be implemented in a similar way.

This optimization is based on the pre-defined geometry topology which is the traditional DBC copper-ceramics-copper planar structure. With the promising 3-D printing technology, it's possible in near future to print metal-ceramic system for non-standard topology which enables very complex geometries with high degree of accuracy. Substrate can be fabricated with non-rectangular shapes, and thickness of each material layers does not need to remain the same throughout the layer. Thus this work can be extended to optimizing a non-fixed topology which maximizes thermal, mechanical, electrical performances and minimize material consumption and potentially cost.

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