3D-PEIM

Decomposition and Electro-Physical Model Creation of the CREE 1200V, 50A 3-Ph SiC Module

3D-PEIM 2016 - Tuesday June 14, 2016

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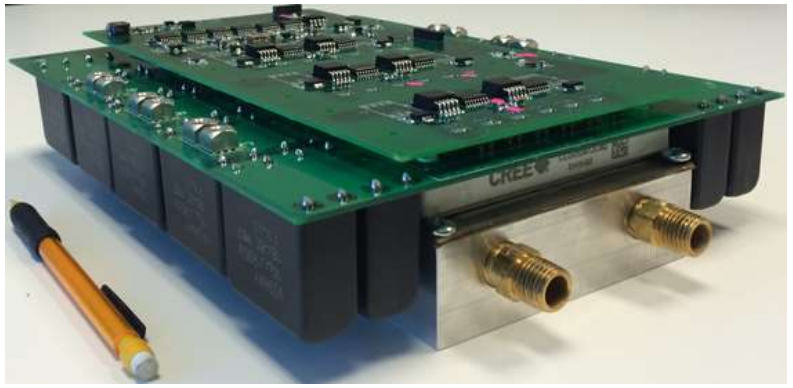
Introduction – Motivation & Application



- Development of an automotive EV inverter platform using WBG semiconductor power devices in an "open-source" manner

- DoE 2020 target for power density is 13.4 kW/L, achievable with WBG devices
- Enables shrinking of passive components → improvements over similar Si-based EV inverter systems:
  - Volume reduction: 56%
  - Weight reduction: 51%
  - Loss reduction: 48%

- Simulate WBG-based power modules within their systems in order to witness multi-physical performance improvement → justify the cost, stimulate adoption

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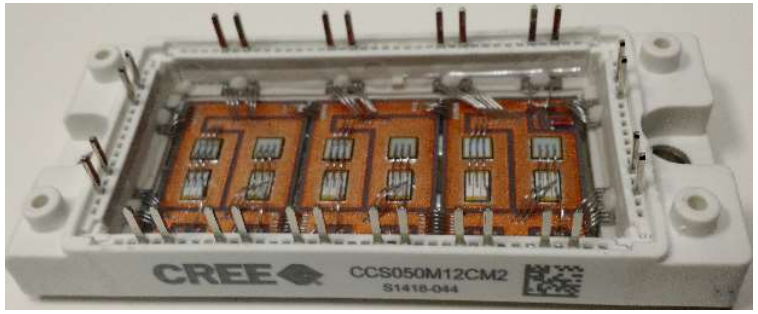
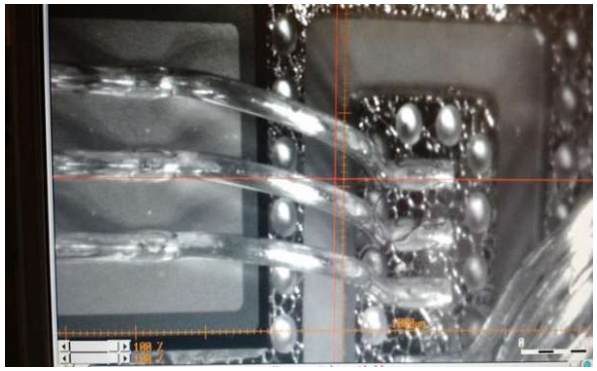
Tear-Down Approach of the CREE Module

- CREE Module: 1200V/50A, 25mΩ 6-Pack SiC MOSFET module (CCS050M12CM2)
- Reverse-engineering technique is developed and applied to the CREE Module power stage
- Hesse Mechatronics BJ939 Heavy Wire/Ribbon Bonder digital camera system, accurate to within 10μm, was used to measure die, interconnect, and substrate length and width dimensions





- For opaque modules, use a minimal parasitic test circuit to analyze switching waveforms, compare with device datasheets, extract parasitic parameters

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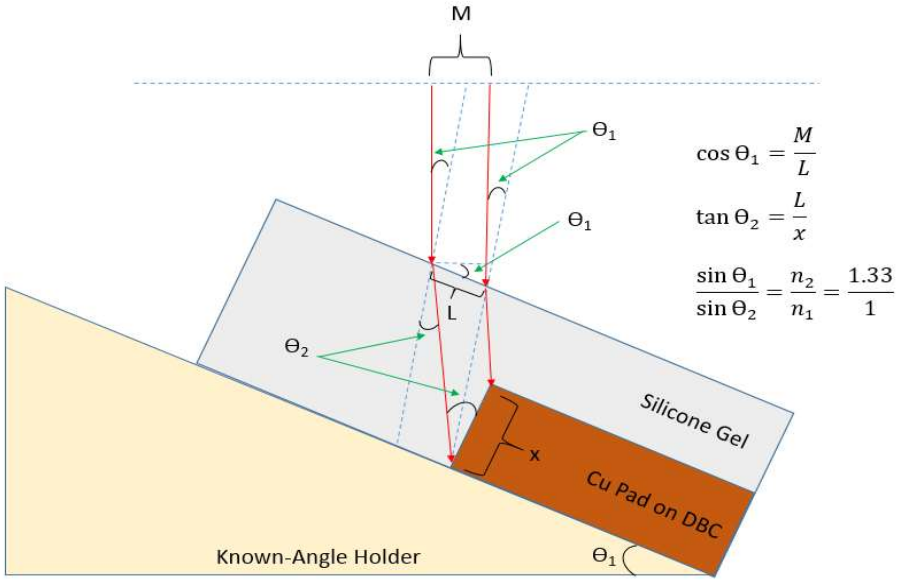
Tear-Down Approach of the CREE Module

- Non-destructive measurement procedure was developed in order to not disturb the power stage of the power module and allow it to still be used in converter circuits after analysis
- Initial heights and thicknesses were measured through a 45° angled holder
- Trigonometric relationships in conjunction with Snell's Law were used for determining the internal layer thicknesses of the substrate and die

1. Place the opened module onto the known angled holder within BJ939
2. Use camera system target reticle to measure the horizontal distance, between the top and bottom edges of each material layer
3. Calculate layer thicknesses using trigonometric relationships and Snell's Law



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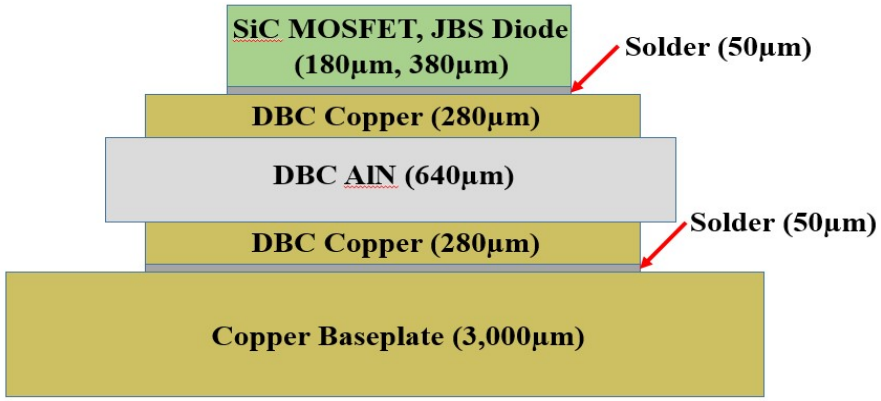
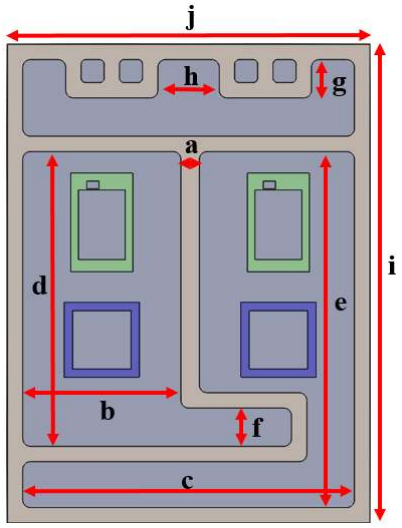
Destructive Tear-Down Validation

- CREE module was disassembled and manually measured to within ±25.4µm (1mil), to validate the measurement procedure
- Solder layers were assumed to be 50µm (SEM technique not used)



DBC AlN	Nondestructive	Destructive	% Error
Thickness	24.2 mils	25 mils	3.2 %
Length	1210 mils	1236 mils	2.1 %
Width	885 mils	902 mils	1.9 %



Dimension	Size (mm)
a	1.2
b	10.3
c	21.6
d	19.24
e	23.24
f	2.5
g	2.5
h	4.0
i	31.24
j	23.6

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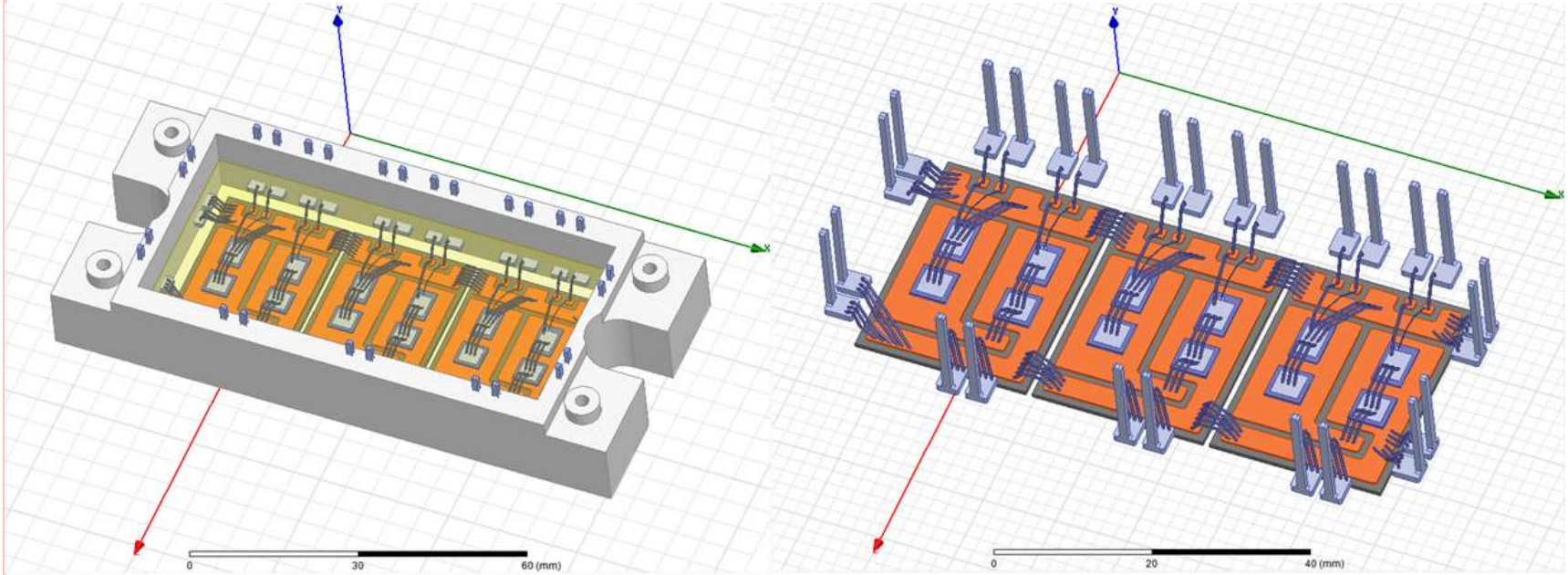
Full 3D-CAD Model of CREE Module

- Complete 3D-CAD model of the power stage, based on the measured dimensions, was created in SolidWorks
- Model includes the module housing, baseplate, die attachment, DBC substrate, wire bonds, SiC MOSFETs and diodes, and terminals



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Parasitic Extraction & Current Distribution

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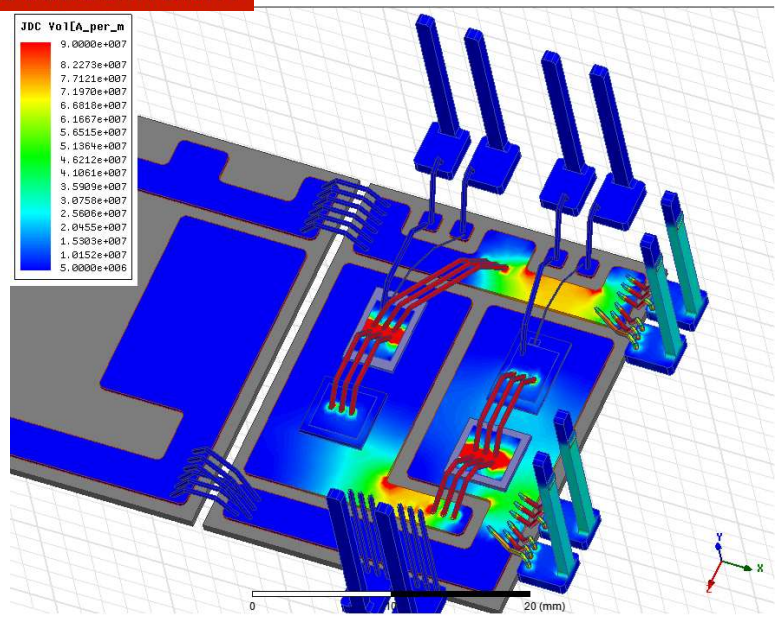

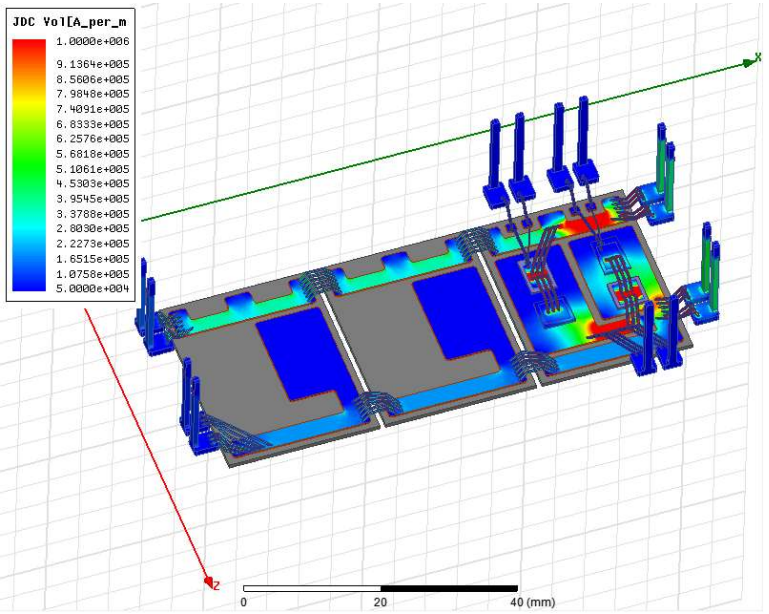

Phase	Freq. (Hz)	DC	10k	100k	1M	10M	100M
A	L(nH)	115.7	102.2	83.66	78.91	74.16	73.43
B	L(nH)	81.73	74.8	61.9	56.52	54.78	54.22
C	L(nH)	47.39	46.49	40.89	37.41	36.23	35.86
A	R(mΩ)	7.33	8.13	12.49	47.26	73.16	219.1
B	R(mΩ)	6.11	6.61	9.83	20.76	55.55	165.6
C	R(mΩ)	4.54	4.71	6.56	13.44	35.48	105.3

Phase	Freq. (Hz)	DC	10k	100k	1M	10M	100M
A	L(nH)	43.37	42.20	36.21	32.76	31.61	31.24
B	L(nH)	51.52	48.72	40.46	36.54	35.25	34.85
C	L(nH)	41.56	40.44	34.80	31.56	30.48	30.13
A	R(mΩ)	4.83	4.98	6.90	14.12	37.28	110.6
B	R(mΩ)	5.04	5.31	7.59	15.64	41.34	122.7
C	R(mΩ)	4.76	4.90	6.79	14.13	37.72	112.5

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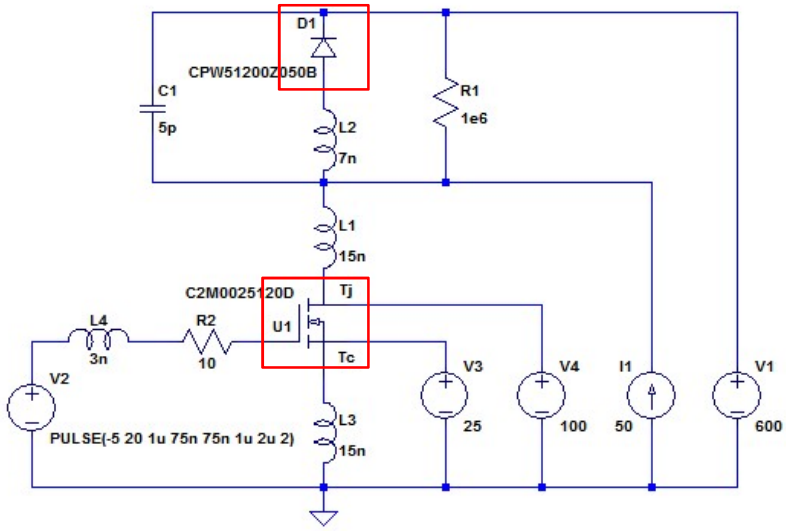
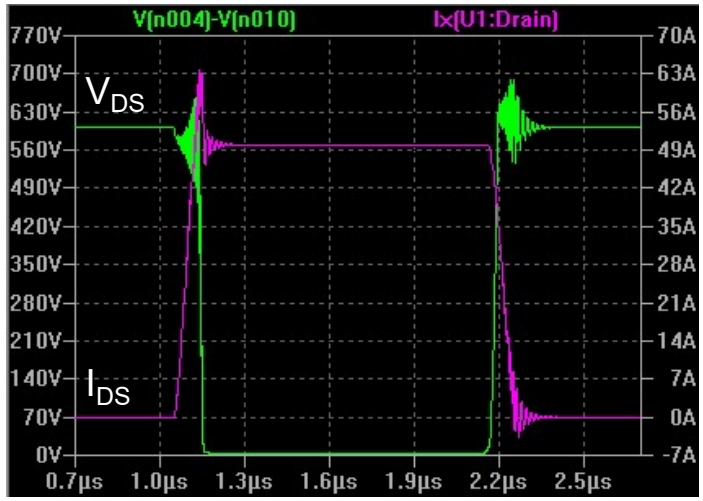
SPICE Model Development & Transient Characterization

- Double-pulse test circuit simulated in LT- SPICE around the CREE module SiC MOSFET and JBS diode device models
- Major extracted parasitic parameters from ANSYS Q3D Extractor were included to observe packaging influences on transient performance
- Series parasitic inductance extending from the MOSFET has been modeled as 15nH on each side of the source and drain





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Parasitic Analysis of Altium Designer PCB

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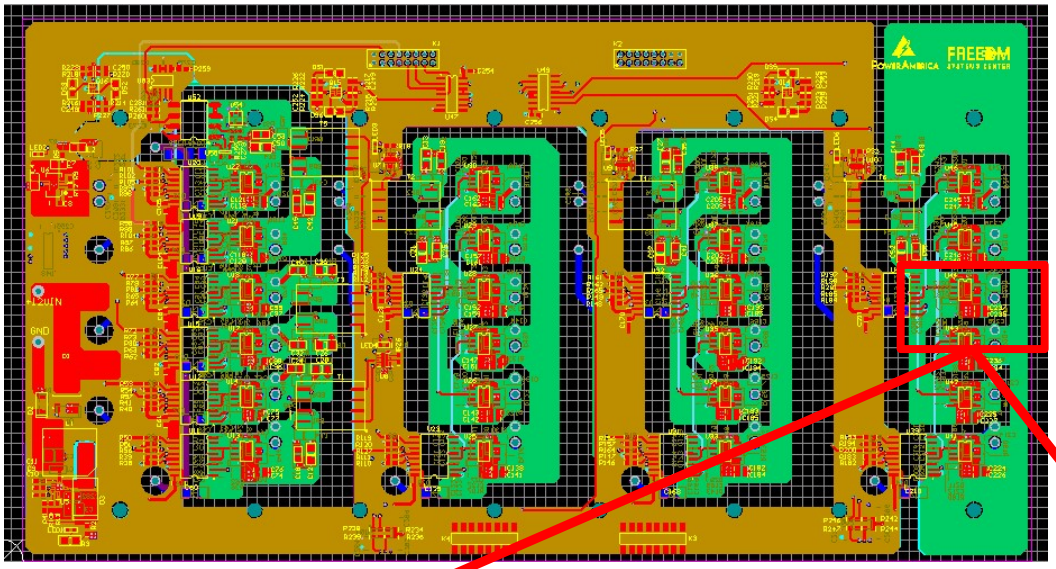
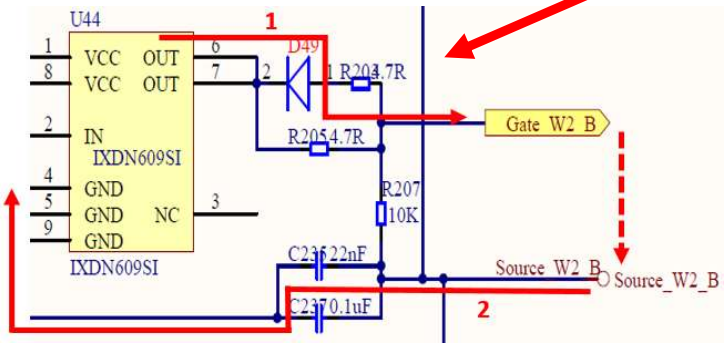
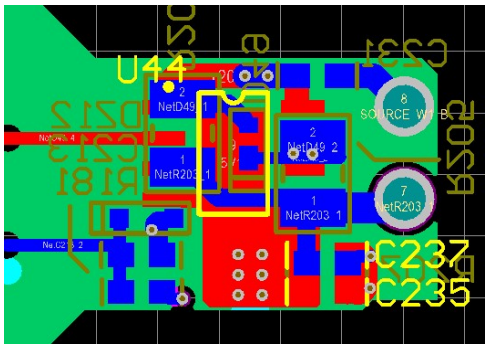
- Electro-physical non-ideality interactions with connected gate drive PCB







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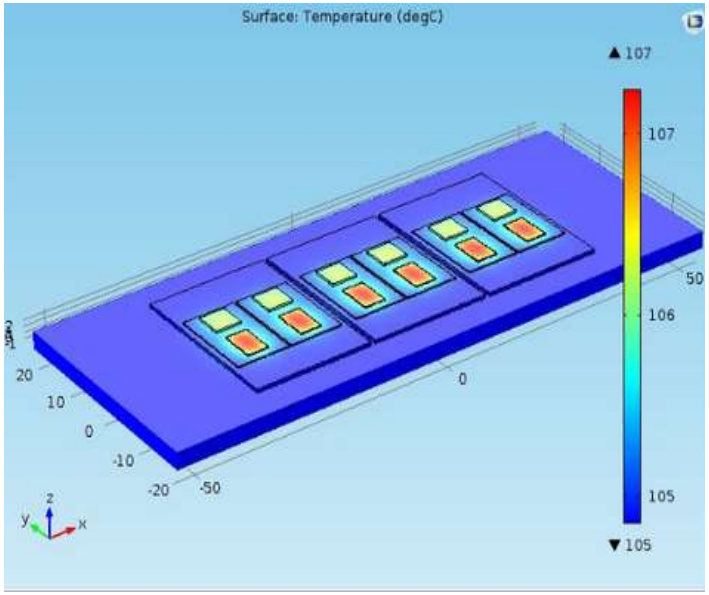
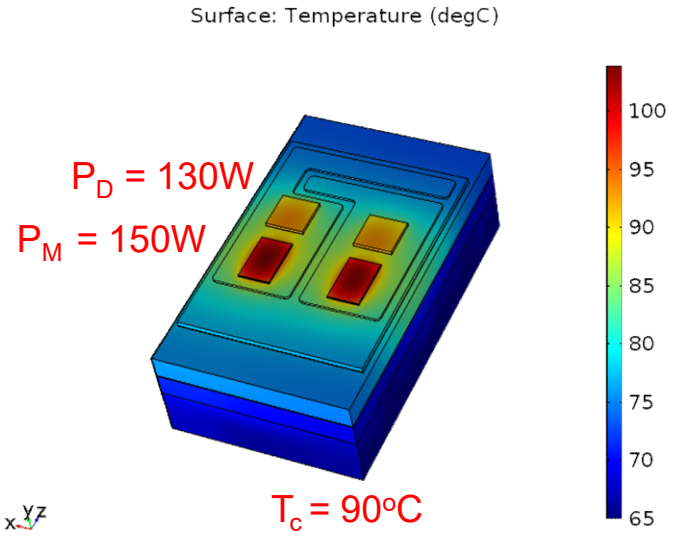
Thermal Model Extraction

- Multi-physics simulator provides in-situ thermal maps of the power stage for various application scenarios



Full 3Ø Power Stage

Single Phase-Leg



- A thermal interface material and pin fin heat sink to capture the thermal spreading from junction to case

R_{th,JC_D} = 0.41 °C/W

R_{th,JC_M} = 0.47 °C/W

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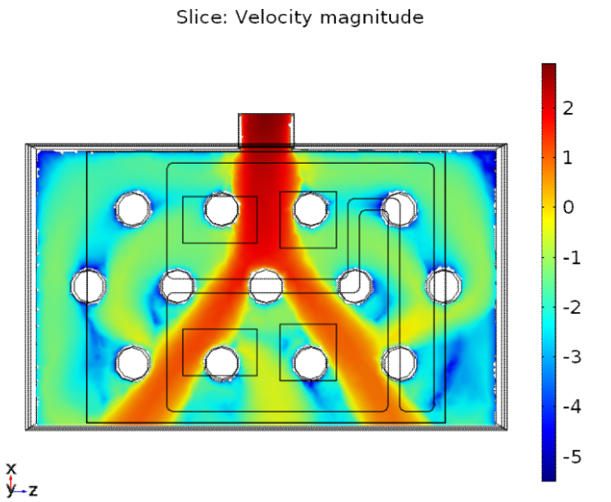
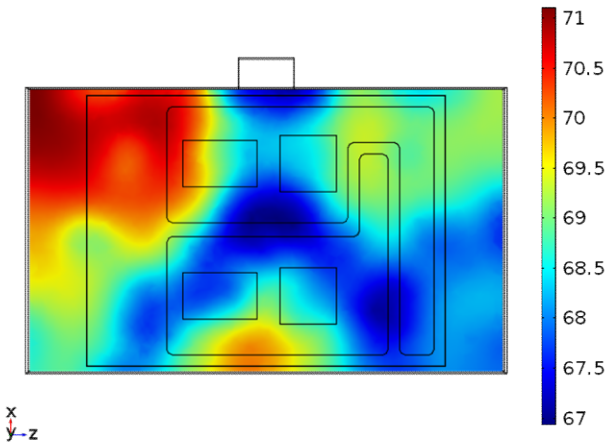
In-Situ Thermal Application Example

Simulation Conditions

- Thermal Interface material
  - Thickness = 100µm
  - Thermal conductivity = 1 W/m-K
  - Pin-fin heat sink water inlet velocity = 0.1L/s

- Model is capable of yielding a detailed thermal map for a given TIM and heat sink application
- Vertical thermal profiles through the power stage are decomposed to capture the thermal spreading from junction to case
- Gain insight into what cooling method to use based upon the applied conditions to the back side of the CREE module





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Large System Application Example

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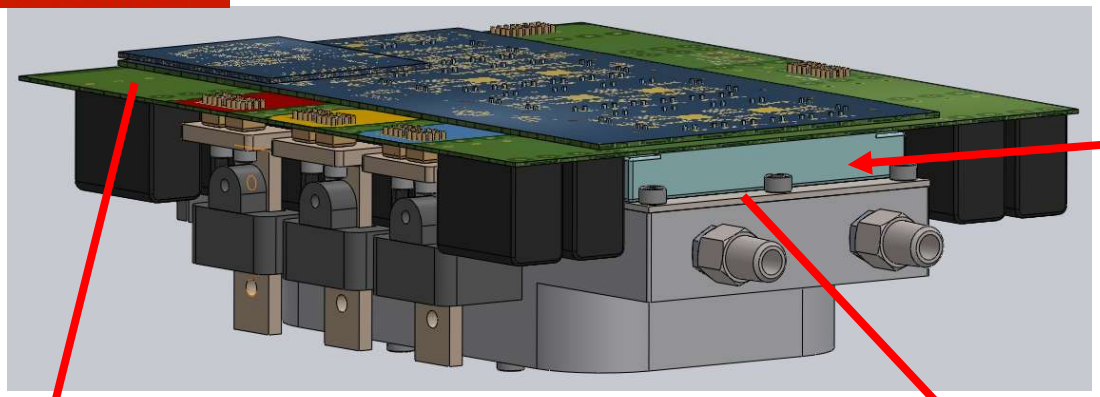
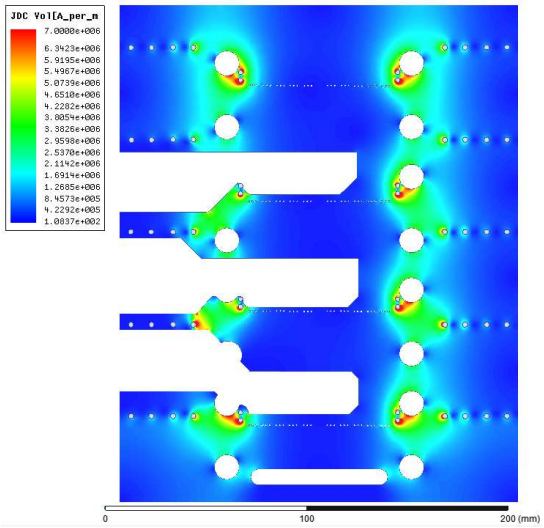
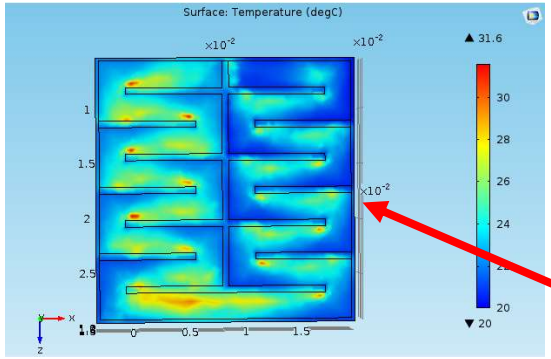


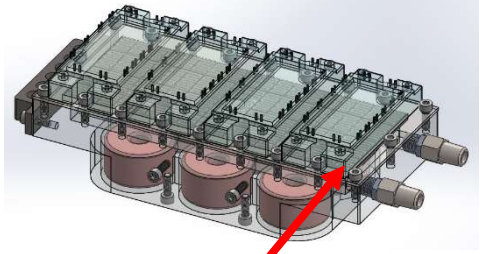
CREE modules within EV inverter system

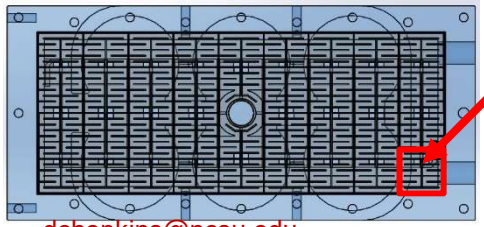
Current distribution between modules and DC-link capacitors



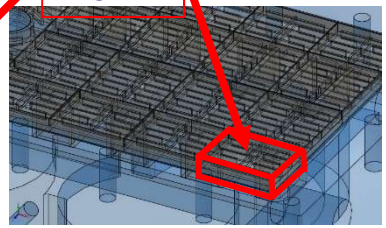
Cold plate simulation between modules and turbulator cell







Turbulator Cell



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Summary

- The developed non-destructive reverse engineering technique allows for an electro-physical model of the CREE module to be created
- Design engineers can use this open-source model to better understand WBG device performance within their systems
- Systems designed around Si-based technology can now be tailored to WBG-based technology → harness full capability of WBG devices

Potential Design Applications

- Better understand how their level 2+ system packaging affects the electrical behavior of the WBG devices
- In-depth insight into how generated heat, under a given operating point, is spreading throughout the entire power stage
- Improve overall system robustness using simulation to design against:
  - Harmful current and voltage overshoots
  - Devices exceeding their allowable junction temperature

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Acknowledgements & Disclaimer

The information, data, or work presented herein was funded in part by the Office of Energy Efficiency and Renewable Energy (EERE), U.S. Department of Energy, under Award Number DE-EE0006521 with North Carolina State University, PowerAmerica Institute.

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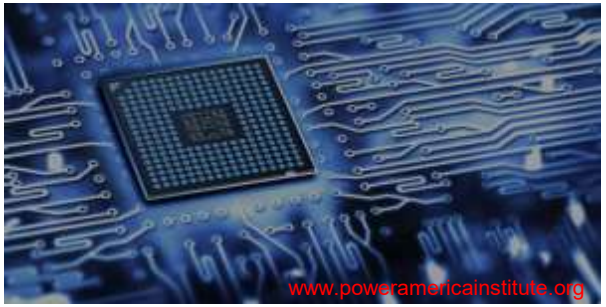
PowerAmerica - Mission

- Eliminate 90% of the power losses in electricity conversion compared to current Si-based technology
- Speed up the proliferation of wide-bandgap (WBG) semiconductor devices into the market's commercial, consumer, and industrial sectors
- Enable design engineers to more easily simulate WBG-based power modules within their systems in order to witness multi-physical performance improvement
- Provide an open-source design tool that provides the basis to create an entire power module model library



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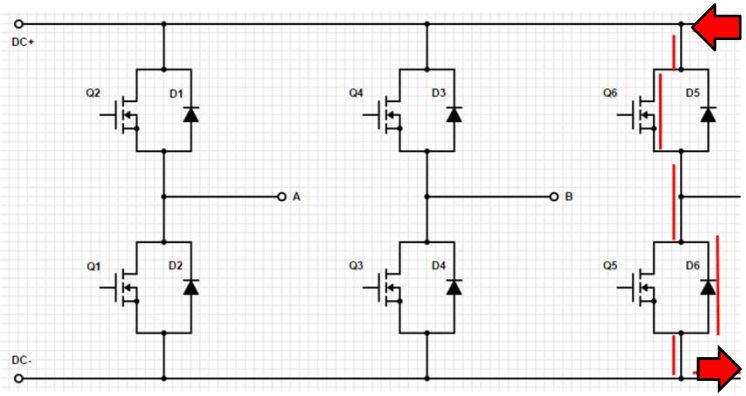
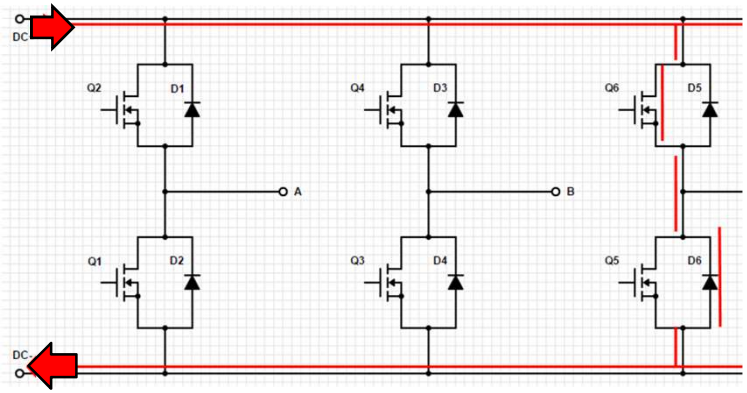
Reference Slides



Connection configuration A and Q3D conduction path of CREE module terminals



Connection configuration B and Q3D conduction path of CREE module terminals

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Maximum Ratings (T_C = 25°C unless otherwise specified)

L_{Stray}	Stray Inductance	30	nH	Measured from pins 25-26 to 27-28	

Comparison with Datasheet

Thermal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
R_{thJCM}	Thermal Resistance Junction-to-Case for MOSFET		0.37	0.40	°C/W	T_c = 90 °C, P_D = 150 W	
R_{thJCD}	Thermal Resistance Junction-to-Case for Diode		0.42	0.43		T_c = 90 °C, P_D = 130 W	