A Folded GaN VRM with High Electrical and Thermal Performance

Bo Gao, Dr. D. C. Hopkins
NSF FREEDM System Center
NC State University
Raleigh, USA
bgao@ncsu.edu

***Abstract*—A concept of using folded flexible PCB as substrate for high density power converter modules was proposed in this paper. Then, a 10MHz VRM based on this concept and GaN technology was used to demonstrate electrical and thermal properties of this concept. Finally, the design proposed here was compared with previous GaN power converters.**

***Index Terms*—Flexible PCB, GaN, VRM, 3D Packaging**

I. Introduction

Modern processors, both CPU and GPU, have reached ~1% power density of the surface of the sun, as a result of higher leakage current and higher switching frequency, both caused by ever shrinking process node. It is very crucial to supply high enough power to those devices when they need, and change output voltage on the fly to reduce idle power consumption. Maintaining control loop stability while allowing rapid change of output voltage requires high enough switching frequency, as well as control loop's respond speed. At the same time, the market is also pursuing smaller, lighter and more power efficient devices, which calls for smaller, more efficient power converters. This also translates to higher switching frequency, since this allows the use of smaller, thinner inductive and capacitive components[1]. Current silicon based commercially available VRMs can operate at up to 600kHz with greater than 90% peak efficiency[1]. However, since the latest processors internally change their power states faster, and the VRM can not catch up, some power is wasted. Fully integrated voltage regulator (FIVR), as the ones integrated in Intel Haswell processors, solved this problem by fixing VRM at a higher voltage, and generates local voltage rails directly on die using package's integrated inductors and MIM on die capacitors[2] as well as capacitors soldered on package interposer. As a result, this increases die size as well as power consumption, as well as package EMI radiation. In addition, this introduces ~10% additional loss.

GaN (gallium nitride) is a wide band gap semiconductor material that is suitable for high frequency, high current applications thanks to its very high electron mobility and critical field strength[3]. By using the term GaN device, in this paper we mean GaN HEMT devices. GaN HEMT devices has some valuable advantages compared to traditional silicon devices, notably lower gate to source and drain to source capacitance, no reverse recovery charge for its body diode, and much lower on state resistance for the same die size. By using much faster GaN devices, modern off chip on board VRM can operate at well beyond 1MHz while maintaining above 90% efficiency. This allows fast and efficient voltage scaling of processors without the use of on die voltage regulators and complicated packaging technology. The following table lists specifications and challenges of a modern on board VRM module:

TABLE I. Specifications and Challenges

Parameter	Value	Challenge
Power	1.2V 100W	Heat dissipation in limited space.
Footprint	10mm*25mm	Limited space for passives.
Height	10mm	Limited space for passives.
DVFS speed	100mV/us	Requires fast control loop speed.
Challenge	**Solution**	
Heat density	Reduce thermal resistance from devices to heat sink.	
	Increase conversion efficiency.	
Limited space	Increase switching frequency to use smaller passives.	
	Increase layout density.	
Fast control loop	Use higher switching frequency.	

II. Approach

The goal is subdivided into 4 smaller goals: higher switching frequency, higher efficiency, high power density and lower thermal resistance between power devices to heatsink. Higher switching frequency requires better layout to battle common source inductance and drain-source loop inductance. The reduction of parasitic parameters also yields higher efficiency. In addition, higher switching frequency allows the use of smaller inductors and capacitors, which also increases power density. By using flexible PCB as substrate of the converter, we can now fold the converter to overlap different components, to save PCB footprint size. The use of flexible PCB also allows us to directly attach power dice to anodized heatsink since the Young's modulus of flexible PCB is very

low, it serves as a strain relief mechanism. In this design, we chose GaN devices as active switches due to the fact that GaN devices has lower on state losses compared to silicon devices of similar size, and GaN devices has much lower input and output charges compared to silicon devices of similar voltage and on state resistance.

The common source inductance, as shown below, reduces effective gate driving voltage during turning on, and increased effective gate voltage during turning off. If we simplify the GaN HEMT model into ideal switch that turns on/off at threshold voltage, and assuming the converter operates in CCM with low enough ripple current, then the common source inductance induced additional rise/fall time can be expressed as $I_{SW}*L_{CS}/(V_G-V_{th})$, where I_{SW} is average output current per converter phase, L_{CS} is common source inductance of high side switch (determines rise time) or low side switch (determines fall time), V_G-V_{Th} is the voltage difference between gate driver's output voltage and HEMT's threshold voltage.

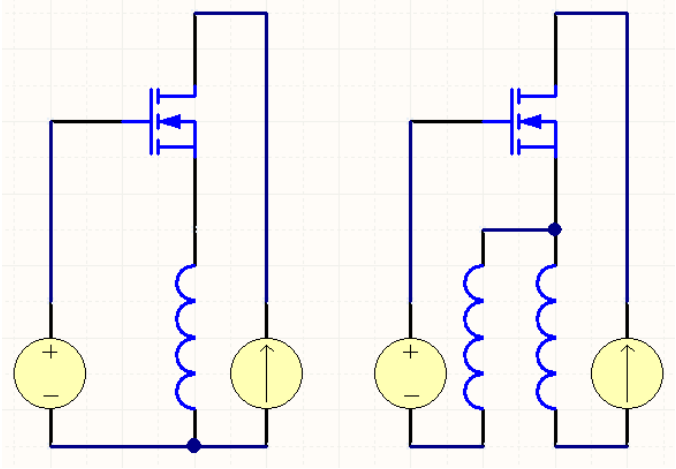

Fig. 1. Common source inductance and Kelvin connection

By using Kelvin connection (aka. 4-wire connection), common source inductance can be reduced to effectively zero in ideal case where gate driving signal shares no drain-source current path. In reality this may not be possible due to intrinsic device package inductance and layout inductance. In addition to common source inductance, gate to source inductance and drain to source inductance (high side drain, high side source, low side drain, low side source and decoupling capacitors circulating current path inductance) are also crucial to efficiency, hence minimizing them is also a design goal. The proposed layout is shown below:

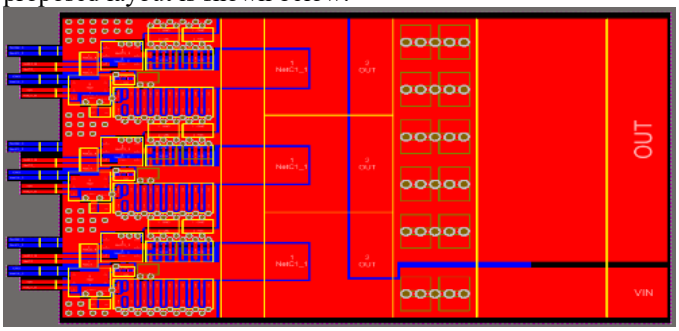

Fig. 2. Proposed flexible PCB layout

Three channels are placed in parallel, with their input and output parallel connected, controlled by a three phase interleaved controller. Controller and gate pre-drivers are not shown here. The gate drivers for high and low side GaN devices are identical, isolated and discrete gate drivers each consisting of a pair of complementary output MOSFETs, a Schmitt trigger, an isolated pulse transformer and a timing generator. On the left side is the power stage of the gate driver, then the gate drivers' bootstrapping diodes and decoupling capacitors are placed right next to the gate drivers. Output of the gate drivers are closely connected to power GaN devices. Since the gate drivers are placed very close to the GaN devices, and the gate return path is not the power ground path, the common source inductance is very low. Decoupling capacitors for the power path (drain-source decoupling capacitors) are placed right next to input 12V and ground. Since the flexible PCB substrate is very thin, the mutual inductance between the top side current path and bottom side current path greatly reduces the self inductance of the top and bottom current path.

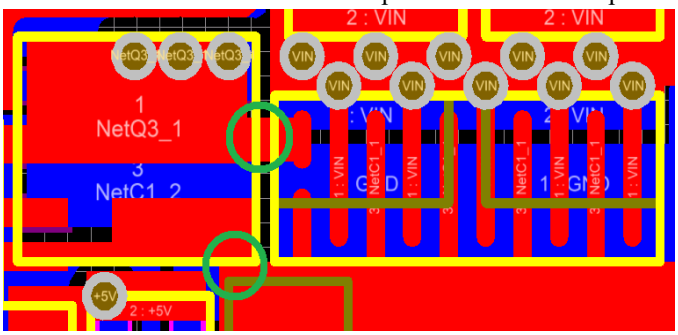

Fig. 3. Details of proposed GaN power device layout shows direct Kelvin connection of gate driving signal

This module is then folded along yellow lines shown in figure 1, thus creating a folded structure. This folded structure is designed such that low power dissipation components, such as output filtering inductors and capacitors, are placed inside the module, while high power dissipation devices such as gate drivers and GaN power devices, are placed on the very top side in order to be coupled thermally to the heatsink. The GaN power devices and gate drivers are bonded to the heatsink with thermally conductive epoxy glue, without any insulation materials in between, to ensure very low thermal resistance. Despite the substrate of GaN devices are connected to their source electrode, the voltage is blocked by 20um of anodized surface of the heatsink, thus at lower voltage (<170V), insulation materials are not needed.

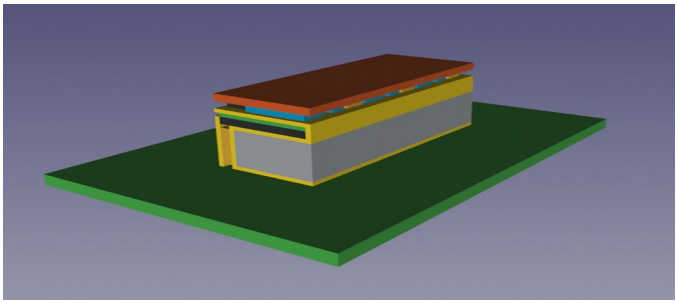

Fig. 4. 3D render of the folded module sitting on a carrier board

The proposed folded module measures at 25mm by 25mm by 10mm, totally 6.25cm^3 (0.38in^3). Its designed output current is 30A per phase, totally 3 phases. At 1.2V, 1.8 and 2.5V output voltage, its power densities is 17.28W/cm^3, 25.92W/cm^3 and 36.00W/cm^3 respectively.

III. Simulation Results

Electrical and thermal simulations are done on the proposed module. Our main focus is on the gate driver's capability of driving GaN devices at 10MHz, the output stage's efficiency, as well as temperature. In order to prevent the gate drivers from dissipating too much power due to shoot through, the output stage of the gate driver is designed to have a very short dead time. The following waveform shows the break before make behavior of the output stage of a single gate driver channel:

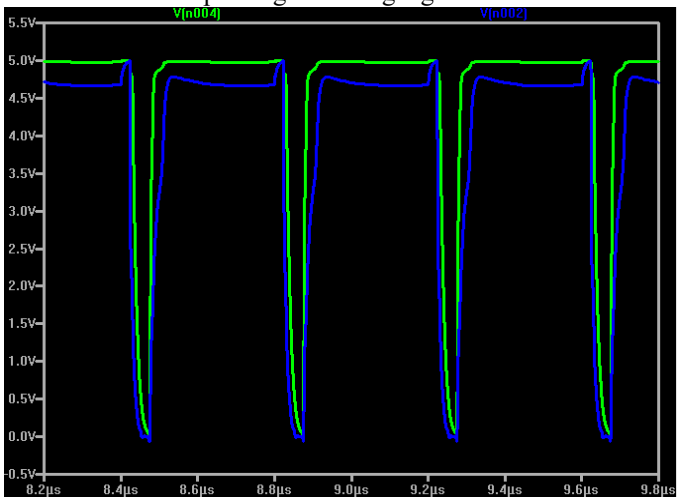

Fig. 5. Break before make behavior of gate driver, green trace is P-MOS's gate signal, blue trace is N-MOS's gate signal

The output of the gate driver shows clean and fast switching waveform, the rise and fall time under a 4nF load at 5V output amplitude is 1.16ns and 2.26ns respectively.

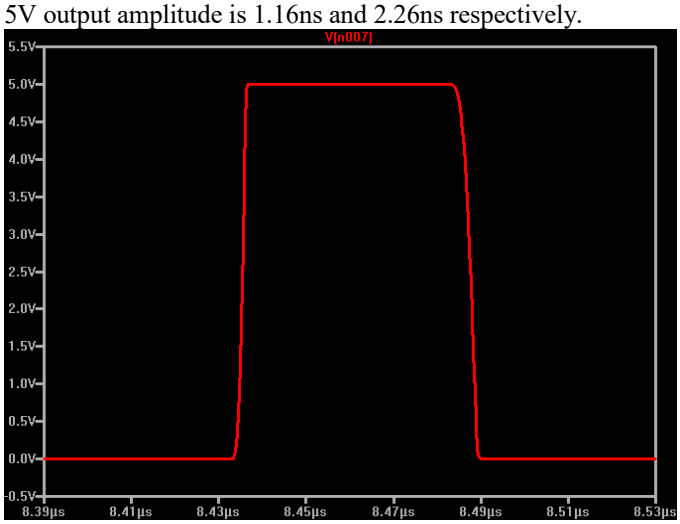

Fig. 6. Gate driver's output waveform

The switching node waveform of a phase leg is shown below. It shows some degree of oscillation due to parasitic drain to source input decoupling current loop inductance.

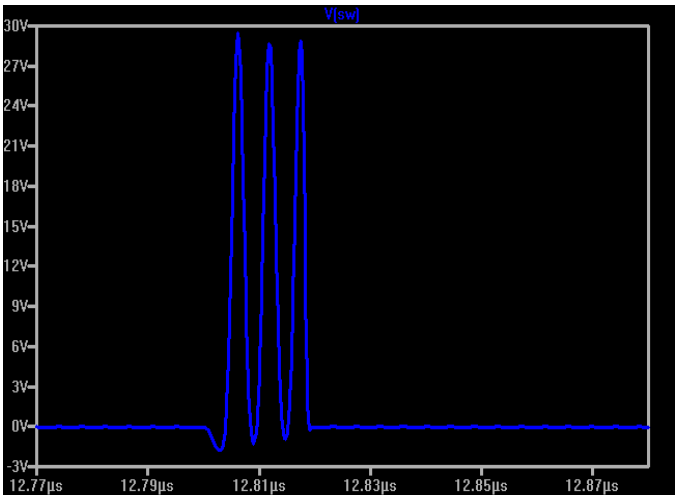

Fig. 7. Switching node waveform of a single cycle

The proposed circuit achieved 88.22% efficiency (power stage only, gate driver loss and power distribution network loss not counted) at 10MHz switching frequency when converting 12V to 1.8V, 30A per phase using active GaN devices EPC2015C and EPC2023 with Coilcraft SRP1649 70nH output inductor and ceramic decoupling capacitors. At 2.5MHz, the converter achieved greater than 96% efficiency at the same input and output conditions.

TABLE II. Efficiency Comparison with Existing Designs

Proposed by	Efficiency	Comments
Briere[1].	80.00%	12V→1.2V 20A 5MHz
Briere[1].	83.40%	12V→1.2V 20A 3MHz
Briere[1].	92.45%	12V→1.2V 20A 600kHz
Wilson, et al[4].	>94%	12V→1V 20A
Reusch[5].	>90%	12V→1.2V 10A 1MHz
Edward, et al[2].	~90%	1.7V→1.05V Haswell FIVR

This shows Kelvin connection indeed reduces switching loss compared to other designs, and the reduction of drain to source input decoupling current path inductance due to the use of very thin flexible PCB substrate and compact layout also reduces switching loss.

Based on electrical simulation result, a thermal simulation was carried out to investigate temperature distribution of the module when operating at 12V to 1.8V, 30A, 10MHz. Since the power dissipation of output LC filter is very low, their power loss can be dissipated by convection and stray air flow of the processor's heatsink fan. The thermal coupling between the top side power devices and output inductor is neglected because thermal resistance is very high between flexible PCB and inductors due to the air gap in between. Here are the parameters input to thermal simulator:

TABLE III. THERMAL PARAMETERS

Parameter	Value
High side switch loss	4.29W per device
Low side switch loss	2.25W per device
Gate driver FET loss	0.5W per pair
Heatsink temperature	40°C at top side
Heatsink material	2mm pure copper
Heatsink insulation	20μm anodizing, no TIM
FPCB copper thickness	34.8μm, rounded to 40μm

The thermal simulation shows the proposed thermal solution that directly attaches power devices to heatsink with neither insulating pads nor TIM has very low thermal resistance, and since the flexible PCB has very low Young's modulus, it relieves the strain caused by directly bonding devices onto heatsink. The thermal simulation shows thermal pad temperatures of active devices.

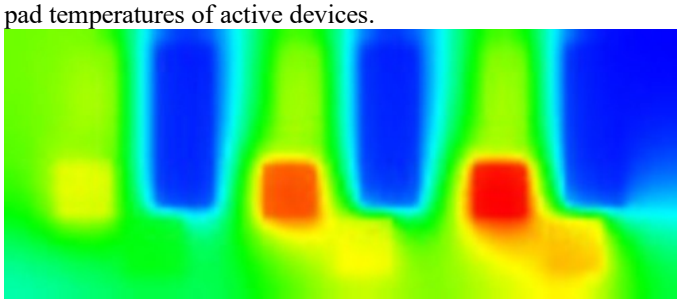

Fig. 8. Thermal plot of proposed design

The simulation plot uses rainbow color schema, where blue represents 41.00°C, and red represents 45.66°C. The gate drivers are hotter than GaN devices due to they are plastic molded devices, hence their die to heatsink thermal resistance is higher. From the simulation we know the thermal performance of the proposed design is excellent compared to traditional solutions based on silicon devices and thermal interface materials.

IV. CONCLUSION

In this paper the authors proposed a folded flexible PCB based GaN VRM design for modern processors. The proposed layout and construction yield high conversion efficiency, and the proposed novel thermal solution eliminates the additional thermal resistance caused by thermal interface materials. As a result, the temperature of proposed design's power devices are only less than 6°C higher than its heatsink when converting 12V to 1.8V 30A at 10MHz.

ACKNOWLEDGMENT

The authors of this paper thanks to Texas Instruments for supporting this project by providing TI device samples and simulation models as well as valuable design feed back.

REFERENCES

[1] Michael A. Briere, *"Advanced Power Devices for Many-core Processors Power Supplies,"* IEEE IEDM, pp. 13.6.1-4, 2010.

[2] Edward A. Burton, et al and William J. Lambert, et al, *"FIVR—Fully Integrated Voltage Regulators on 4th Generation Intel Core SoCs,"* IEEE APEC, pp. 432-439, 2014.

[3] Alex Lidow and Johan Strydom, "*Gallium Nitride (GaN) Technology Overview,*" http://epc-co.com/epc/Portals/0/epc/documents/papers/Gallium%20Nitride%20GaN%20Technology%20Overview.pdf

[4] Christopher G. Wilson, et al, "*Hard Switching Speed Improvements in GaN-based Synvhronous Buck Converters,*" IEEE WiPDA, pp. 76-79, 2013.

[5] David Reusch, "*Optimizing PCB Layout,*" http://epc-co.com/epc/Portals/0/epc/documents/papers/Optimizing%20PCB%20Layout%20with%20eGaN%20FETs.pdf