MONDAY
Tutorials
Additive Manufacturing
System Integration
Thermal Packaging
Keynotes
Additive Manufacturing

TUESDAY
Systems Integration
Thermal Management
Multiphysics Design Tools
Materials
Manufacturing Technologies

WEDNESDAY
Embedding Technologies
Heterogeneous Integration
Quality and Reliability
Maryland Lab Tours
MESSAGE FROM THE CHAIRPERSON

Welcome to the 2nd International Symposium on 3D Power Electronics Integration & Manufacturing (3D-PEIM). Your professional colleagues and the world’s leading Packaging and Manufacturing societies and associations are sponsoring this symposium to bring together world-class experts representing electrical, materials and manufacturing perspectives to discuss the latest advances in the technologies, design and manufacturing of 3D power electronics systems. This symposium will offer both oral presentations and interactive sessions in which speakers will have the opportunity to display their hardware during the breaks and receptions. So please take advantage of the breaks and receptions to look, touch and feel the great technologies our presenters are talking about.

We also thank the Power Sources Manufacturers Association (PSMA) who is underwriting the event, along with the IEEE Electronics Packaging Society (EPS); the University of Maryland; North Carolina State University; and Virginia Tech.

Welcome to Maryland, and we wish you a productive and enjoyable time at the symposium!

Sincerely,

Dr. F. Patrick McCluskey
General Chair
University of Maryland, College Park

GENERAL CHAIR
Dr. Patrick McCluskey, University Of Maryland

TECHNICAL PROGRAM CHAIRS
Chair
Dr. Guo-Quan Lu, Virginia Tech

Co-chairs
John Bultitude, KEMET
Dehong Xu, Zhejiang University, China

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Dimeji Ibitayo, ARL
Yunhui Mei, Tianjin University
Steven Miner, Naval Academy
Brian Narveson, PSMA
Khai Ngo, Professor, VT
Michael Ohadi, University Of Maryland
Ernie Parker, Manager, Crane
Brandon Passmore, Wolfspeed

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Abhijit Dasgupta, University Of Maryland
Douglas Devoto, NREL
Edward Herbert, PSMA
Doug Hopkins, Professor, NCSU

Brian Peaslee, GM
P. Markondeya Raj, Georgia Tech
Matt Romig, TI
Ryan Sochol, University of Maryland
Katsuaki Suganuma, Osaka University
Michael Tonne, Danfoss
Eckhard Wolfgang, ECPE
7:30 AM – 2:00 PM  
REGISTRATION OPEN

7:30 AM – 8:00 AM  
BREAKFAST

8:00 AM – 12:15 PM  
TUTORIALS  
“Additive Manufacturing” Dr. Christopher Williams, Virginia Tech (DREAMS Lab)  
“System Integration” Prof. Douglas Hopkins, NCSU (NSF FREEDOM LAB)  
“Integrated Thermal Packaging” Dr. Michael Ohadi, U. of MD

12:15 PM – 1:15 PM  
LUNCH - Tutorial Attendees Only & Networking

1:15 PM – 1:25 PM  
OPENING REMARKS BY SYMPOSIUM GENERAL CHAIR  
Prof. Patrick McCluskey, University Of Maryland

1:25 PM – 2:45 PM  
SK SYMPOSIUM KEYNOTE CHAIR  
Prof. Guo-Quan Lu, Virginia Tech  
“Small Quiet Robust and Affordable: Delivering the Integrated Promise”  
Prof. Mark Johnson, U. of Nottingham, UK  
“Embedding Technologies: for Planar Power Electronics Modules”  
Prof. Rolf Aschenbrenner, Fraunhofer Institute, Berlin, Germany

2:45 PM – 3:15 PM  
BREAK & NETWORK (Photo)

3:15 PM – 5:00 PM  
S1: ADDITIVE MANUFACTURING CHAIRS  
Dimeji Ibitayo (ARL) and Ryan Sochol (U. of MD)  
Keynote: “TBD”  Dimeji Ibitayo, ARL  
Invited: “Additive Manufacturing Methods and Materials Requirements for the Fabrication of 3D Printed Hybrid Electronic Circuits”  Daniel Hines U. of MD (LPS)  
Invited: “Additive Manufacturing in Power Development”  Lauren Boteler, ARL  
Invited: “Additive Manufacturing in Power Magnetics”  Prof. Guo-Quan Lu, Virginia Tech

5:00 PM – 7:00 PM  
WELCOME RECEPTION & VENDOR EXHIBITS
8:00 AM – 9:45 AM S2: SYSTEMS INTEGRATION & THERMAL MANAGEMENT - CHAIRS
Lauren Boteler, ARL and Mike Ohadi (U. of MD)
Keynote: “Heterogeneous Integration Roadmap Update - Integrated Power Electronics” Prof. Douglas Hopkins, NCSU (NSF FREEDOM LAB)
Invited: “Package Configuration and Thermal Analysis of Enhanced Durability Power Electronic Packages” Dr. Darshan Pahinkar, Georgia Tech
Invited: “Thermal Management and Packaging of High Temperature Automotive Power Electronics” Gilbert Moreno, NREL
“Design of SiC Power Modules Integrated with Metal Foam and Phase Change Material for Pulsed Load Applications” W. Shao, L. Ran, Z. Zeng, and P. Mawby, Chongqing University, China
9:45 AM – 10:15 AM BREAK & NETWORKING
10:15 AM – 12:00 PM S3: MULTIPHYSICS DESIGN AND TOOLS - CHAIRS
Abhijit Dasgupta (U. of MD) and Steven Miner (Naval Academy)
Keynote: “Reduced Order CoDesign Analysis for Design Space Evaluation of Power Electronic Modules” Lauren Boteler, ARL
Invited: “Thermal Models of Multilayer Ceramic Capacitors for 3-D Power Electronics” Allen Templeton, KEMET
Invited: “Applications of COOLCAD to Power Electronics” Neil Goldsman, U. of MD
Invited: “Reliability Modeling Software for Electronic Systems” Mike Osterman, U. of MD (CALCE)
12:00 PM – 1:00 PM LUNCH & NETWORKING
1:00 PM – 2:45 PM S4: MATERIALS - CHAIRS
John Bultitude (Kemet) and Yunhui (Joe) Mei (Tianjin University)
Keynote: “New bonding Cu ink by using low temperature sinterable Cu particles” Dr. Jung-Lae Jo, Mitsui Mining & Smelting Co, Ltd
Invited: “Soft magnetic Metal-Flake Composite Material Suitable for Highly Integrated Power Modules” Kenichi Chatani, Tokin a KEMET company
Invited: “The Development of Materials for 3D Packaging of Power Products” Mr. Ken Araujo, Namics USA
“Improvement of Ag Sintering Quality on Cu Surface at Hydrogen Atmosphere” Testu Takemasa, Minoru Ueshima, Jinting Jiu, Seino Junko, Katsuaki Suganuma, Osaka University
2:45 PM – 3:15 PM BREAK & NETWORKING
3:15 PM – 5:00 PM S5: MANUFACTURING TECHNOLOGIES - CHAIRS
William Chen (ASE) and Brian Narveson (Narveson Innovative Consulting)
Keynote: “Challenges of Heterogeneous Integration for Power Electronics” Dr. William Chen, ASE
Invited: “Advanced PCB Solutions Supporting Next Generation Power Applications” David Warner, AT&S
Invited: “High Reliability Silver Sintering for Power Modules” Gyan Dutt, Alpha Assembly Solutions
Invited: “Vacuum-assisted Sintering in Mass Production: Challenges and Solutions” Aaron Hutzler, PINK GmbH
5:00 PM – 7:00 PM NETWORKING RECEPTION, POSTER SESSION, VENDOR EXHIBITS, WITH DINNER BUFFET AT 6:00 PM
8:00 AM – 9:45 AM

**S6: EMBEDDING TECHNOLOGIES – CHAIRS**
Khai Ngo (Virginia Tech) and Brandon Passmore (Wolfspeed)

Keynote: “TBD” Dimeji Ibitayo, ARL

Invited: “SiC Power Electronics Systems With High Level of Mechatronic Integration for Automotive and Aircraft Application”
Dr. Maximilian Hofmann, Fraunhofer IISB

Dr. Cyril Buttay, Centre National de la Recherche Scientifique (Ampere Lab)

Invited: “Thick-film Embedded Passives for Power Modules”
Dr. Taner Dosluoglo, Endura

9:45 AM – 10:15 AM

BREAK & NETWORKING

10:15 AM – 12:00 PM

**S7: HETEROGENEOUS INTEGRATION OF COMPONENTS – CHAIRS**
Matt Romig (Texas Instruments) and Pulugurtha Markondey Raj (GA Tech)


Invited: “Integration of Energy Storage into Power Module by Magnetic Molding”
Khai Ngo, Virginia Tech

Invited: “High-density Power Package with Improved Reliability, Electrical and Thermal Performances for Automotive Drivetrain”
Vanessa Smet GA Tech

“A High Density and High Voltage Power Module with 3D Through Ceramic Via Providing Integration Solutions for Pulsed System”
Long Zhang, Gang Dai, Juntao Li, Yingkun Yang, Tingrui Gong, Kun Zhou, Fen Qin, Lei Gao, Chinese Academy of Engineering Physics, PR China.

12:00 PM – 1:00 PM

LUNCH & NETWORKING

1:00 PM – 2:45 PM

**S8: QUALITY & RELIABILITY – CHAIRS**
Mike Azarian (U. of MD) and Doug DeVoto (NREL)

Keynote: “From Fit for Standard to Fit for Application” Eckard Wolfgang, ECPE

Invited: “Quality and Reliability Issue in Integrated Power Electronics”
Mike Azarian, U. of MD

Invited: “Live Condition Monitoring of High-Power Switching Devices using Smart Modulation” Faisal Khan, U. of Missouri

“Impact of Accelerated Stress-Tests on SiC MOSFET Precursor Parameters”
Joseph Kozak, Douglas DeVoto, Joshua Major, Khai Ng, NREL

2:45 PM – 3:15 PM

BREAK & NETWORKING

3:15 PM – 5:00 PM

**NETWORKING & LABORATORY TOUR – CHAIR**
Prof. Patrick McCluskey (U. of MD)

Assisting: Dr. Daniel Shen, U. of MD

Assisting: Mr. Subramani Manoharan, U. of MD
Professor C Mark Johnson received the BA degree in engineering and the PhD degree in electrical engineering from the University of Cambridge, UK, in 1986 and 1991 respectively.

From 1990 to 1992 he was a Research Associate at the University of Cambridge and in 1992 he was appointed Lecturer at the Newcastle University, UK, where his research included the design, analysis and characterisation of power semiconductor devices, resonant power conversion and instrumentation.

From 1998 to 2001 he managed the UK national programme on Silicon Carbide electronics and in 2000 he became Reader of Power Electronics at Newcastle University. In 2003, Professor Johnson was appointed as Rolls-Royce/RAEng Research Professor of Power Electronic Systems at the University of Sheffield and in 2006 he was appointed to a personal chair at the University of Nottingham, where he leads research into power semiconductor devices, power device packaging, reliability, thermal management, power module technologies and power electronic applications.

He is Director of the UK Engineering and Physical Sciences Research Council (EPSRC) Centre for Power Electronics, which combines the UK’s best academic talent to address the key research challenges underpinning power electronics and is leader of the Advanced Propulsion Centre (APC) Thematic Spoke in Power Electronics.

Small Quiet Robust and Affordable: Delivering the Integration Promise

C Mark Johnson, University of Nottingham

Wide band-gap semiconductors offer many potential benefits to designers of power electronic systems. Lower switching losses allow operation at higher switching frequencies, which in principle allows a reduction in passive component values in many converter applications. However, efficient operation at higher switching frequencies requires increased voltage and current transition rates. Currents induced through parasitic capacitances, as a result of high $dv/dt$ and voltages induced in parasitic inductances, as a result of high $di/dt$, can both be expected to be higher with WBG devices. With conventional packaging and circuit construction, the resulting transient voltage spikes and ringing will add to the electromagnetic interference (EMI) emitted from the system. Additionally, the typical design of power module substrate results in a relatively high capacitance from the switching node to the module baseplate and hence to ground if, as is typical, the module is mounted on a grounded, metal heatsink. This can lead to unacceptable levels of common mode current flow. To mitigate these effects in conventional modules, the switching speeds of WBG devices are often limited by introducing additional gate resistance. Outside the commutation cell, fast voltage transitions may lead to unacceptably high levels of conducted and radiated EMI, so approaches involving the local filtering of converter outputs are attractive. Here we examine the design and realisation of “Converter-in-Package” (CiP) modular blocks for system power levels from 100s W to 100s kW, incorporating individual commutation cells with close-coupled gate drives, input/output filtering and electromagnetic screening/shielding.
SYMPOSIUM KEYNOTE ADDRESS

Rolf Aschenbrenner

Rolf Aschenbrenner received the B.S. degree in mechanical engineering from the University for Applied Science, Gießen, Germany, in 1986 and the M.S. degree in physics from the University of Gießen, Germany, in 1991. From 1991 to 1992 he has worked at the University of Gießen and in 1993, he joined the Research Center for Microperipheric Technologies at the Technical University of Berlin. Since March 1994 he has been employed at the Fraunhofer Institute for Reliability and Microintegration Berlin (IZM) where he is presently the Deputy Director and Head of the Department System Integration and Interconnection Technologies.

He received the iNEMI International Recognition Award in 2005, the CPMT David Feldman Outstanding Contribution Award 2013 and the European Semi Award 2016.

As a member of the IEEE EPS Society Board of Governors Rolf Aschenbrenner has worked as a European representative on the Conference Advisory Board Committee, and has played an active role in the globalization of IEEE EPS in terms of membership and chapter development. He served as IEEE CPMT Vice President, Technical and IEEE EPS Vice President, Conferences. From January 2010 until December 2011 he was IEEE EPS President and in 2012 he became IEEE Fellow.

Embedding Technologies for Planar Power Electronic Modules

R. Aschenbrenner

Fraunhofer Institute for Reliability and Microintegration
Gustav-Meyer-Allee 25, D – 13355 Berlin, Germany
Email: aschenbrenner@izm.fraunhofer.de, phone: + (49) 30 464 03 164

In most of these packages the power semiconductors are connected by bond wires, resulting in large resistances and parasitic inductances. Power chip packages have to carry semiconductors with increasing current densities. Conventional wire bonds are limiting their performance. Today’s power modules are based on DCB (Direct Copper bonded) ceramic substrates. IGBT switches are mounted onto the ceramic and their top side contacts are connected by thick Al wires. This allows one wiring layer only and makes an integration of driver chips very difficult. Additionally bond wires result in a high stray inductance which limits the switching frequency. Especially the use of ultra-fast switching wide-bandgap semiconductors, like SiC and GaN, is very difficult.

The embedding of chips offers a solution for many of the problems in power chip packages and power modules. While chip embedding was an academic exercise a decade ago, it is now an industrial solution. This presentation will show today’s available power packages and power modules realized in industrial production as well as in European research projects. The presentation try to show what concrete form such systems may take in the industrial reality, what requirements these package types will be subjected to and where the development trends may lead in the future. This presentation addresses the impact of the IC and end product requirements on packaging, interconnect technology, and assembly.
ROOM LAYOUT: THE STAMP

Colony Ballroom

Charles Carroll

(27) rectangle linens - all tables

REGISTRATION

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