3D SiP with Embedded Chip Providing Integration Solutions for Power Applications

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3D-PEIM
June 14, 2016
Outline

- Introduction of UTAC and System in a Package (SiP) Sites
- Multi-chip Package (MCP) / SiP Forecast & Attributes
- Trends & Applications, Trade offs for 3D SiP w/ Embedded Chip
- Adoptions of Embedded Chip Packaging in Power and High Density Applications
- 3D SiP with Embedded Chip UTAC / AT&S Collaboration
- Summary
UTAC at a Glance

• Outsourced Semiconductor Assembly and Test services (“OSAT”) provider in support of Analog, Mixed-Signal, Logic, Power and Memory products.

• UTAC 2015 Revenue $878M; Ranked 6th in the Top Ten OSAT

• Focus – Assy, Test and Turnkey; Test comprises 35% in 2015.

• 1997 Established in Singapore

• HQ in Singapore; Mfg - Singapore, Taiwan, Malaysia, Indonesia, Thailand, China.

• >260K M² Manufacturing Space and about 12K Employees Globally.

• Sales offices located worldwide.

• Markets: Mobile Phone, Automotive, Security, Wearable’s, Industrial & Medical.
UTAC SiP Sites Summary

**UTAC Dongguan, China (UDG)**
[Since 1988, >500k sq ft, China Logistics, WW distribution]
BGA, LGA, QFN, Memory Cards, USB, SiP, 3D SiP w/ Embedded chip

**UTAC Thailand (UTL)**
[Since 1973, 640k sq ft, Auto & Security certs.]
QFN, GQFN, LGA, MIS  MEMS, Cu Clip

**UTAC Shanghai, China (USC)**
[90k sq ft, WGQ Free trade zone]
QFN, FBGA, LGA, MIS
### SiP/MCP FORECAST

<table>
<thead>
<tr>
<th>Product/Package Type</th>
<th>Volume (Bn Units)</th>
<th>2014</th>
<th>2019F</th>
<th>Leading Suppliers/Players</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stacked Die In Package and Memory Card</td>
<td>8.3</td>
<td>10.5</td>
<td></td>
<td>Samsung, Micron, SKHynix, Toshiba, SanDisk PTI, ASE, SPI, Amkor, STATS ChipPAC</td>
</tr>
<tr>
<td>Stacked Package on Package: Bottom Package Only</td>
<td>0.95</td>
<td>1.2</td>
<td></td>
<td>Samsung, Apple, Qualcomm, Mediatek Amkor, STATS ChipPAC, ASE, SPI</td>
</tr>
<tr>
<td>PA Centric RF Module</td>
<td>4.5</td>
<td>5.9</td>
<td></td>
<td>Qorvo, Skyworks, Anadigics, Avago, Amkor, ASE, Inari, HEG, JCET, Unisem, ShunSIN</td>
</tr>
<tr>
<td>Connectivity Module (Bluetooth/WLAN)</td>
<td>0.5</td>
<td>0.7</td>
<td></td>
<td>Murata, Taiyo Yuden, Samsung, ACSIP, ALPS, USI</td>
</tr>
<tr>
<td>Graphics/CPU or ASIC MCP</td>
<td>0.25</td>
<td>0.20</td>
<td></td>
<td>Intel, AMD, Nvidia, Xilinx, Altera</td>
</tr>
<tr>
<td>Leadframe Module (Power/Other)</td>
<td>3.2</td>
<td>4.7</td>
<td></td>
<td>NXP, STMicro, TI, Freescale, Toshiba, Infineon/IR, Renesas, ON Semi</td>
</tr>
<tr>
<td>MEMS and Controller</td>
<td>5.4</td>
<td>8.2</td>
<td></td>
<td>ST, Analog, Bosch, Freescale, Knowles, InvenSense, Denso</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>23.1</strong></td>
<td><strong>31.4</strong></td>
<td></td>
<td>Source: Prismark</td>
</tr>
</tbody>
</table>

**SiP Attributes:**
- Heterogeneous integration into a **standard package** format (BGA, LGA, leadless or leaded leadframe)
- **Multiple ICs** typ. w/ diverse device functions (logic + memory, RF or analog + digital, control + sensors)
- **Passive** Components (discrete - SMT, embedded; IPD – stacked, embedded or planar 2D)
- **Mixed assembly** technologies (SMT, Wirebond, FC, Embedded / RDL - wafer / panel level)

**MCP (multi chip package) attributes:**
- Multiple ICs in a standard package but typically few or no passives
- Typically not diverse device functions (Memory – RAM + Non volatile, Logic + Logic)
- Die stacking is widely used in Memory MCP
Trend to 3D SiP with Embedded Chip

- CMOS driver
- GaAs FET die
- Other passive components

SiP Integration Density

3D integration
Chip Embedding

3D Interconnect
2 side cooling
Shielding

Co-Design
Optimization

SiP Performance (size, electrical & thermal)
# Applications for 3D SiP with Embedded chip

## Embedded die potential applications matrix


<table>
<thead>
<tr>
<th>Stand-Alone active die packages</th>
<th>Embedded SiP Modules</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cell phones</strong></td>
<td>Cellular Radio: IPD-RF, Transceiver, PA</td>
</tr>
<tr>
<td><strong>Portable media players</strong></td>
<td>WLAN Module: IPD-RF, DC/DC converter</td>
</tr>
<tr>
<td><strong>Notebooks</strong></td>
<td>Bluetooth/GPS/FM: DC/DC converter, processor</td>
</tr>
<tr>
<td><strong>Digital cameras</strong></td>
<td>CPU/GPU: Embedding of stacked ICs in PoP</td>
</tr>
<tr>
<td></td>
<td>Memories: Embedding of stacked ICs in PoP</td>
</tr>
<tr>
<td></td>
<td>Baseband: Embedding of stacked ICs in PoP</td>
</tr>
<tr>
<td></td>
<td>Audio Module: IPD-ESD, IPD-Capa, Audio codec/driver</td>
</tr>
<tr>
<td></td>
<td>Digital TV Module: IPD-Capa, Video decoder, DC/DC converter</td>
</tr>
<tr>
<td></td>
<td>Camera Modules: Sensor, DC/DC ISP, AF driver</td>
</tr>
<tr>
<td></td>
<td>MEMS/Sensor Modules: Sensor(s), ASIC</td>
</tr>
<tr>
<td></td>
<td>Oscillators, Si-microphones, pressure sensors, inertial sensors, magnetic Hall sensor, RFID</td>
</tr>
<tr>
<td></td>
<td>LED Modules: LED driver, MOSFET</td>
</tr>
<tr>
<td><strong>Medical &amp; industrial</strong></td>
<td>Hearing Aids: IPD-ESD, IPD-Digital, processor, memory</td>
</tr>
<tr>
<td></td>
<td>Pacemakers: IPD-ESD, IPD-RF, IPD-Digital, processor, memory</td>
</tr>
<tr>
<td></td>
<td>Wireless Sensor Node applications: RFID, thin-film battery, magnetic hall sensor</td>
</tr>
<tr>
<td><strong>Automotive</strong></td>
<td>Engine Control Module: MCU, memory, IPD</td>
</tr>
<tr>
<td></td>
<td>Telematics/Car information units: GPS, NFC</td>
</tr>
<tr>
<td></td>
<td>MEMS/Sensor Modules: Sensor(s), ASIC</td>
</tr>
<tr>
<td></td>
<td>Camera Modules, Hall Sensors, TPMS, IMU modules, RFID</td>
</tr>
</tbody>
</table>

3D SiP w/ Embedded Chip Pros / Cons

Miniaturization:
+ Reduced SiP component footprint area
- Increased SiP component mounted Z height

Design flexibility:
+ Tailor the interconnect technology (embedded via, wirebond, FC or SMT)
  Allows embedded chip technology to provide higher wiring density solutions.
  (Co-design methodology is required to optimize for system and device
cost / performance trade-offs. Chips first assembly techs require co-design for):
- KGD requirements, design for test & yield optimization.

Electrical performance:
+ Improved signal integrity or power efficiency thru shorter vertical (via)
  interconnects,
  power / ground planes in embedded chip substrates and lower package parasitics.
+ EMI / RFI shielding and isolation of digital and RF devices thru ground planes and
  plated via ground fences along with ability to shield the top side assembly.
+ 3D SiP architecture enables closer placement of critical passives
  (inductors, capacitors, filters, etc…) to IC devices.
Comparison of Package Area vs. Thermal Resistance

Source: GaN Systems, AT&S IMAPS 2014
What are Dialog's milestones?
- Eng sample date
- Release to production date
- Annual volumes 2017, 2018, 2019
- Max. allowed pkg height
Power QFN with Cu Clip

Replaces traditional wire bond interconnection, used for high performance MOSFETs (reference DrMOS)

Cu clip replaces multiple Cu or Al wire bonds

Cu clip provides lower resistance and inductance than multiple wire bonds

Cu clip improves thermal performance

*Image Source: Electronic Design*
TI MicroSiP™ (Introduced 2011)
> 20 products Step-down & Boost Converters

Thermal Evaluation

Thermal Image of MicroSiP™ when IC is dissipating 0.45W. Ambient temperature is 22°C, max junction temperature is 72°C. For thermal modeling, a value of \( \Theta_{JA}=125^\circ C/W \) provides an excellent initial estimate of thermal performance.

Board-Level Reliability Data

<table>
<thead>
<tr>
<th>Test Parameters</th>
<th>Results (t_{first fail})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drop</td>
<td>1500G/1.0ms pulse</td>
</tr>
<tr>
<td>Temp Cycle</td>
<td>-40/125°C, 2 cycles/hr</td>
</tr>
</tbody>
</table>
Embedded Chip Technology – adoption accelerating in Power Applications

Infineon’s embedded chip DrBlade™

Buck converter with driver and high-side and low-side switches
TDK’s SESUB Technology shrinks Power Management section 60% in BlackBerry™ Z10 Phone
Embedded Chip Technology – for high density / bandwidth 3D Pkg (2.5D architecture w/out TSVs)

**EMIB Construction** (Embedded Multi-die Interconnect Bridge)

An Alternative Architecture for High Density Multi-Chip Package Connections

Source: Intel Corp. (IMAPS March 2016)
## Intel EMIB vs. 2.5D Silicon Interposer: Evaluation Matrix

<table>
<thead>
<tr>
<th></th>
<th>Silicon Interposer</th>
<th>EMIB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wiring Density</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chip-to-Chip Signal Integrity</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Through Package Signal Integrity</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Through Package Power Delivery</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Silicon Processing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Substrate Processing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assembly Processing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Chip/Si Area on Package</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall Cost</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Final Recommendation</strong></td>
<td></td>
<td>✔</td>
</tr>
</tbody>
</table>

Source: Intel Corp. R. Mahajan keynote IMAPS DPC 2016
3D SiP Supply Chain UTAC / AT&S Collaboration

Alignment on Design
Rules & Roadmaps
- Substrate design
- Assembly design
- Design integration

Co-Design

Wafer to Die

Substrate embedded chip

Package assembly

Test

Customer Consigned Option

Customer Specs

KGD test
RDL
Thin / Dice
Inspect / TnR

Substrate manufacturing
Embedded chip
Strip Test

SMT
Top FC / under fill
Cap or Mold
Solder Ball Attach
Package saw

Package level test
Reliability test

March 2015 - Joint marketing / supply chain agreement
AT&S over 5 years production embedding experience.
UTAC / AT&S 3D SiP Process Flow

- *WLP Back-end*
  - Back Grind
  - Wafer Saw
  - Inspect, KGD Test
  - T&Reel

- Laser-Drilling of fiducials + overlay
- Component/Die Attach
  - Printing of adhesive
  - Attachment
- Layup & Pressing
- Laser Drilling
- Mechanical Drilling

- Desmearing
- Metallization
  - Imaging
  - Copper Plating
  - Stripping + Etching
- Auto-Inspection
- Solder Mask
- Routing
- E-Test

- Surface Finish (OSP/ENEPIG/NiPdAu)
- Final Inspection
- SMT flow
  - FC – U/F optional
  - Over mold or Lid Attach
- Solder Ball Attach
- Package Saw
- Visual Inspection
- Packaging Level Test

* Die require 5-10um thick Cu pads for embedding at > 200um pad pitch
## Sarda Technologies Rev. 1 HIPS

**Package Type:** 4.5 x 7.2mm LGA-SIP  
**Highlights:** 2 embedded die + 24 passive components on substrate top side

<table>
<thead>
<tr>
<th>Package size / Type</th>
<th>4.5 x 7.2 mm LGA-SIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Thickness</td>
<td>560 um ±10%</td>
</tr>
<tr>
<td></td>
<td>320um core</td>
</tr>
<tr>
<td>Die thickness</td>
<td>200 um Max.</td>
</tr>
<tr>
<td>Surface finish (Die DAP)</td>
<td>Electrolytic NI/AU</td>
</tr>
<tr>
<td>Surface finish (Land Pad)</td>
<td>Electrolytic NI/AU</td>
</tr>
<tr>
<td># of Passive Component (Top of substrate surface)</td>
<td>24ea Passive</td>
</tr>
<tr>
<td>Component Sizes</td>
<td>Passive</td>
</tr>
<tr>
<td></td>
<td>10ea 01005, 10ea 0402, 4ea 0201.</td>
</tr>
<tr>
<td># of embedded chip</td>
<td>2</td>
</tr>
<tr>
<td>Strip Size</td>
<td>188x64mm</td>
</tr>
<tr>
<td>Substrate Metal layer</td>
<td>4 Layer</td>
</tr>
</tbody>
</table>

**Assy Layout**

- CMOS Driver Die
- GaAs FET Die

*Courtesy of Sarda Technologies, Inc.*
# 3D SiP with Embedded Chip Reliability Summary

**AT&S Reliability Data and UDG Laminate Reliability Requirements**

## AT&S

<table>
<thead>
<tr>
<th>Method</th>
<th>Specification</th>
<th>Result</th>
<th><strong>UDG Laminate Requirements</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Moisture Sensitivity Level</td>
<td>Peak @ 260 C</td>
<td>Minimum MSL3</td>
<td>MSL3</td>
</tr>
<tr>
<td>Thermal Cycling</td>
<td>-55 C / +150 C</td>
<td>1000cycles passed (TC Grade 1)</td>
<td>-55 C / +125 C ; 1000 cycles</td>
</tr>
<tr>
<td>HAST</td>
<td>110 C @ 85%RH @ 5VDC</td>
<td>264 hours passed</td>
<td>uHAST - 130 C/85%RH; 96 hours</td>
</tr>
<tr>
<td>High Temperature Storage</td>
<td>@125 C</td>
<td>1000hours passed (TH Grade 2)</td>
<td>150 C ; 1000 hours</td>
</tr>
<tr>
<td>Temperature/ Humidity</td>
<td>85 C / 85%RH</td>
<td>1000hours passed (TH Group A)</td>
<td>Per customer</td>
</tr>
<tr>
<td>Board bending</td>
<td>5mm/s</td>
<td>80K bends passed</td>
<td>Per customer</td>
</tr>
<tr>
<td>Random vibration</td>
<td>3 g (rms) (5-500) Hz</td>
<td>30 min per axis passed</td>
<td>Per customer</td>
</tr>
<tr>
<td>Shock</td>
<td>10kg @ 0.2ms</td>
<td>3 per direction passed</td>
<td>Per customer</td>
</tr>
<tr>
<td>Reflow sensitivity</td>
<td>Pb-free profile (255 C)</td>
<td>30 cycles passed</td>
<td>Per customer</td>
</tr>
<tr>
<td>Drop Test</td>
<td>1500g @ 0.5ms</td>
<td>10 drops passed (MS Group F)</td>
<td>Per customer</td>
</tr>
</tbody>
</table>

## Components:

**Material:** Silicon  
**Component type:** Daisy Chain  
**Component size:** 0.9mm x 0.9mm to 5.9mm x 5.9mm

---

**PCB:**  
No of layers: 4  
Base material: Panasonic R 1570  
PCB size: 120mm x 120mm  

**UDG can perform Reliability Testing as required per Customer Specs.**
Summary

- System in a package (SiP) is a strategic focus area for UTAC
- 3D SiP with Embedded Chip provides integration, size and performance benefits over 2D planar SiP solutions
- 3D Embedded Chip technology adoption is accelerating in Power and High Density Interconnect Applications
- Supply chain collaboration with AT&S for emerging 3D SiP solutions with embedded chip technology will advanced the technology and provide FTK supply solution for customers