3D SiP with Embedded Chip Providing Integration Solutions for Power Applications

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Outline

- Introduction of UTAC and System in a Package (SiP) Sites
- Multi-chip Package (MCP) / SiP Forecast & Attributes
- Trends & Applications, Trade offs for 3D SiP w/ Embedded Chip
- Adoptions of Embedded Chip Packaging in Power and High Density Applications
- 3D SiP with Embedded Chip UTAC / AT&S Collaboration
- Summary

UTAC at a Glance

- Outsourced Semiconductor Assembly and Test services (“OSAT”) provider in support of Analog, Mixed-Signal, Logic, Power and Memory products.
- UTAC 2015 Revenue $878M; Ranked 6th in the Top Ten OSAT
- Focus – Assy, Test and Turnkey; Test comprises 35% in 2015.
- 1997 Established in Singapore
- HQ in Singapore; Mfg - Singapore, Taiwan, Malaysia, Indonesia, Thailand, China.
- >260K M^2 Manufacturing Space and about 12K Employees Globally.
- Sales offices located worldwide.
- Markets: Mobile Phone, Automotive, Security, Wearable’s, Industrial & Medical.

UTAC SiP Sites Summary

UTAC Dongguan, China (UDG)

[Since 1988, >500k sq ft, China Logistics, WW distribution]

BGA, LGA, QFN, Memory Cards, USB, SiP, 3D SiP w/ Embedded chip

UTAC Thailand (UTL)

[Since 1973, 640k sq ft, Auto & Security certs.]

QFN, GQFN, LGA, MIS MEMS, Cu Clip

UTAC Shanghai, China (USC)

[90k sq ft, WGQ Free trade zone]

QFN, FBGA, LGA, MIS

SiP/MCP FORECAST

Product/Package Type Volume (Bn Units)	2014	2019F	Leading Suppliers/Players
Stacked Die In Package and Memory Card	8.3	10.5	Samsung, Micron, SKHynix, Toshiba, SanDisk PTI, ASE, SPIL, Amkor, STATS ChipPAC
Stacked Package on Package: Bottom Package Only	0.95	1.2	Samsung, Apple, Qualcomm, Mediatek Amkor, STATS ChipPAC, ASE, SPIL
PA Centric RF Module	4.5	5.9	Qorvo, Skyworks, Anadigics, Avago, Amkor, ASE, Inari, HEG, JCET. Unisem, ShunSin
Connectivity Module (Bluetooth/WLAN)	0.5	0.7	Murata, Taiyo Yuden, Samsung, ACSIP, ALPS, USI
Graphics/CPU or ASIC MCP	0.25	0.20	Intel, AMD, Nvidia, Xilinx, Altera
Leadframe Module (Power/Other)	3.2	4.7	NXP, STMicro, TI, Freescale, Toshiba, Infineon/IR, Renesas, ON Semi
MEMS and Controller	5.4	8.2	ST, Analog, Bosch, Freescale, Knowles, InvenSense, Denso
Total	**23.1**	**31.4**	Source: Prismark

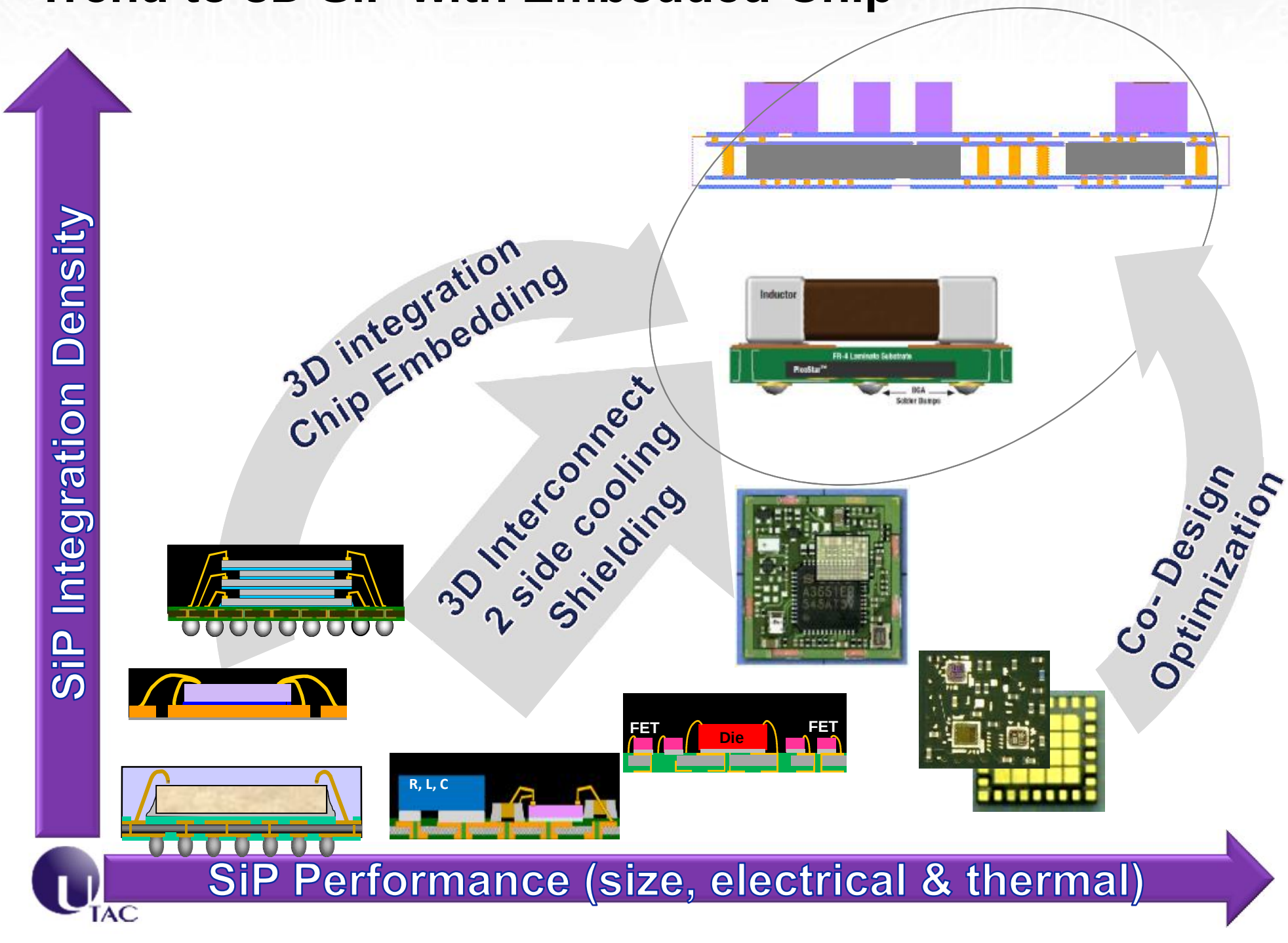
SiP Attributes:

- Heterogeneous integration into a **standard package** format (BGA, LGA, leadless or leaded leadframe)
- **Multiple ICs** typ. w/ diverse device functions (logic + memory, RF or analog + digital, control + sensors)
- **Passive** Components (discrete - SMT, embedded; IPD – stacked, embedded or planar 2D)
- **Mixed assembly** technologies (SMT, Wirebond, FC, Embedded / RDL - wafer / panel level)

MCP (multi chip package) attributes:

- Multiple ICs in a standard package but typically few or no passives
- Typically not diverse device functions (Memory – RAM + Non volatile, Logic + Logic)
- Die stacking is widely used in Memory MCP

Trend to 3D SiP with Embedded Chip



Applications for 3D SiP with Embedded chip

Embedded die potential applications matrix

(Source: Fan-Out and Embedded Die: Technologies & Market Trends report, Yole Développement, Feb. 2015)






	Stand-Alone active die packages	Embedded SiP Modules
Cell phones **Portable media players** **Notebooks** **Digital cameras**	○ IPD - ESD protection ○ IPD – RF ○ DC/DC converters ○ IC Drivers: **Audio codec, battery charger, display interface, LED driver)** ○ Power Management Unit ○ Transceivers ○ Bluetooth/GPS/FM: **Processor**	○ Cellular Radio: **IPD-RF, Transceiver, PA** ○ WLAN Module: **IPD-RF, DC/DC converter** ○ Bluetooth/GPS/FM: **DC/DC converter, processor** ○ CPU/GPU: **Embedding of stacked ICs in PoP** ○ Memories: **Embedding of stacked ICs in PoP** ○ Baseband: **Embedding of stacked ICs in PoP** ○ Audio Module: **IPD-ESD, IPD-Capa, Audio codec/driver** ○ Digital TV Module: **IPD-Capa, Video decoder, DC/DC converter** ○ Camera Modules: **Sensor, DC/DC ISP, AF driver** ○ MEMS/Sensor Modules: **Sensor(s), ASIC** ➢ Oscillators, Si-microphones, pressure sensors, inertial sensors, magnetic Hall sensor, RFID ○ LED Modules: **LED driver, MOSFET**
Medical & industrial	○ Power Applications: **MOSFET, IC drivers, Thin-film batteries**	○ Hearing Aids: **IPD-ESD, IPD-Digital, processor, memory** ○ Pacemakers: **IPD-ESD, IPD-RF, IPD-Digital, processor, memory** ○ Wireless Sensor Node applications: **RFID, thin-film battery, magnetic hall sensor**
Automotive	○ IPM *"Intelligent Power Modules"* **MOSFET, IGBT, IC driver, Sensor**	○ Engine Control Module: **MCU, memory, IPD** ○ Telematics/Car information units: **GPS, NFC** ○ MEMS/Sensor Modules: **Sensor(s), ASIC** ➢ Camera Modules, Hall Sensors, TPMS, IMU modules, RFID

3D SiP w/ Embedded Chip Pros / Cons

Miniaturization:

+ Reduced SiP component footprint area
- Increased SiP component mounted Z height

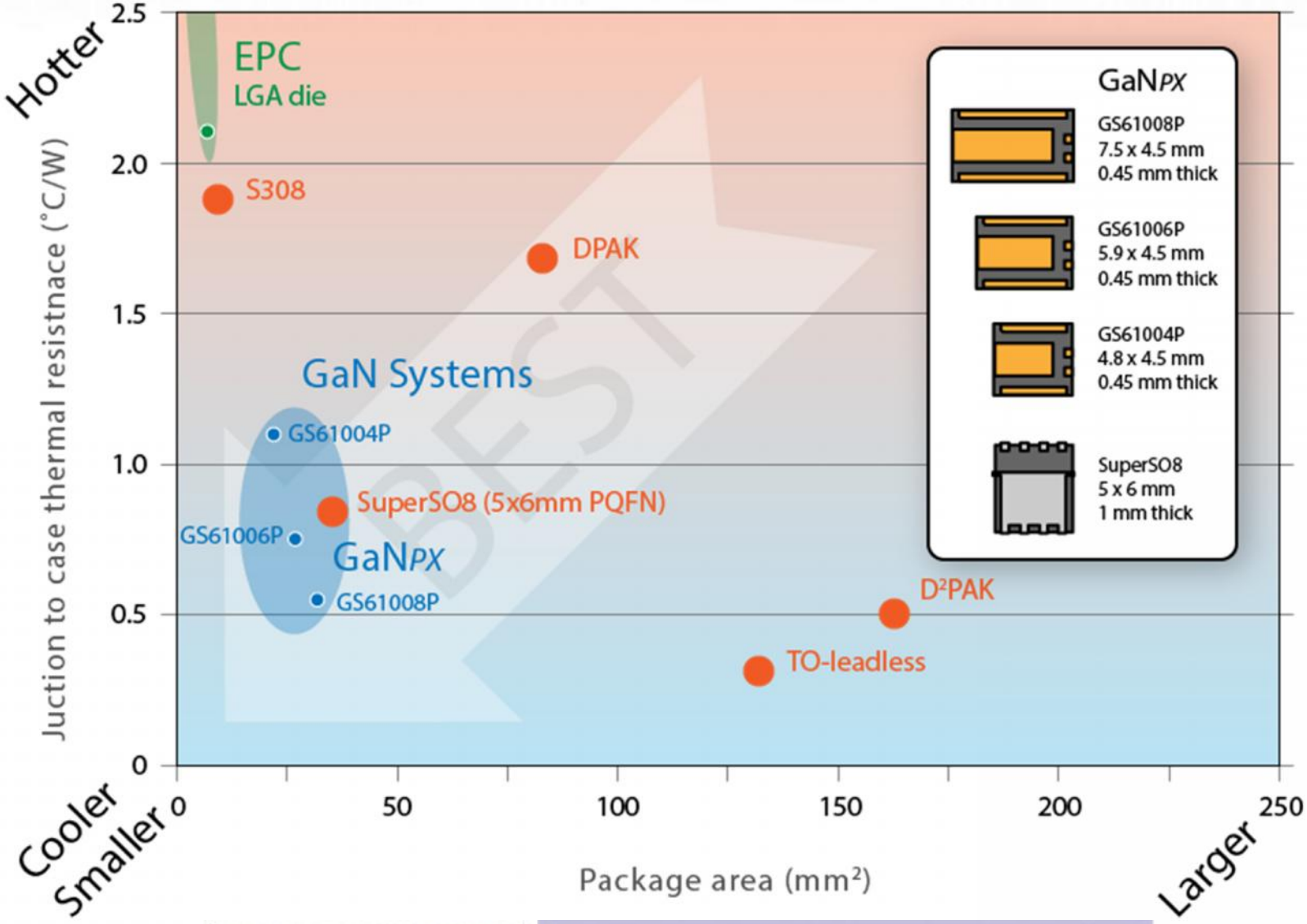
Design flexibility:

+ Tailor the interconnect technology (embedded via, wirebond, FC or SMT)
  Allows embedded chip technology to provide higher wiring density solutions.
  (Co-design methodology is required to optimize for system and device
  cost / performance trade-offs. Chips first assembly techs require co-design for):
- KGD requirements, design for test & yield optimization.

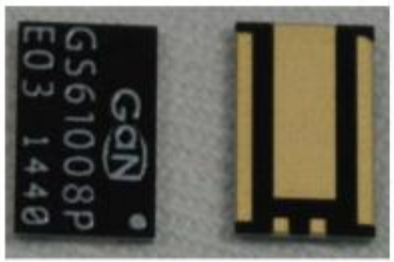
Electrical performance:

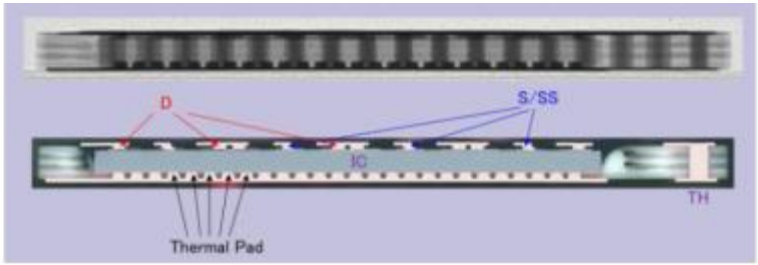
+ Improved signal integrity or power efficiency thru shorter vertical (via) interconnects,
  power / ground planes in embedded chip substrates and lower package parasitics.
+ EMI / RFI shielding and isolation of digital and RF devices thru ground planes and
  plated via ground fences along with ability to shield the top side assembly.
+ 3D SiP architecture enables closer placement of critical passives
  (inductors, capacitors, filters, etc…) to IC devices.

Comparison of Package Area vs. Thermal Resistance

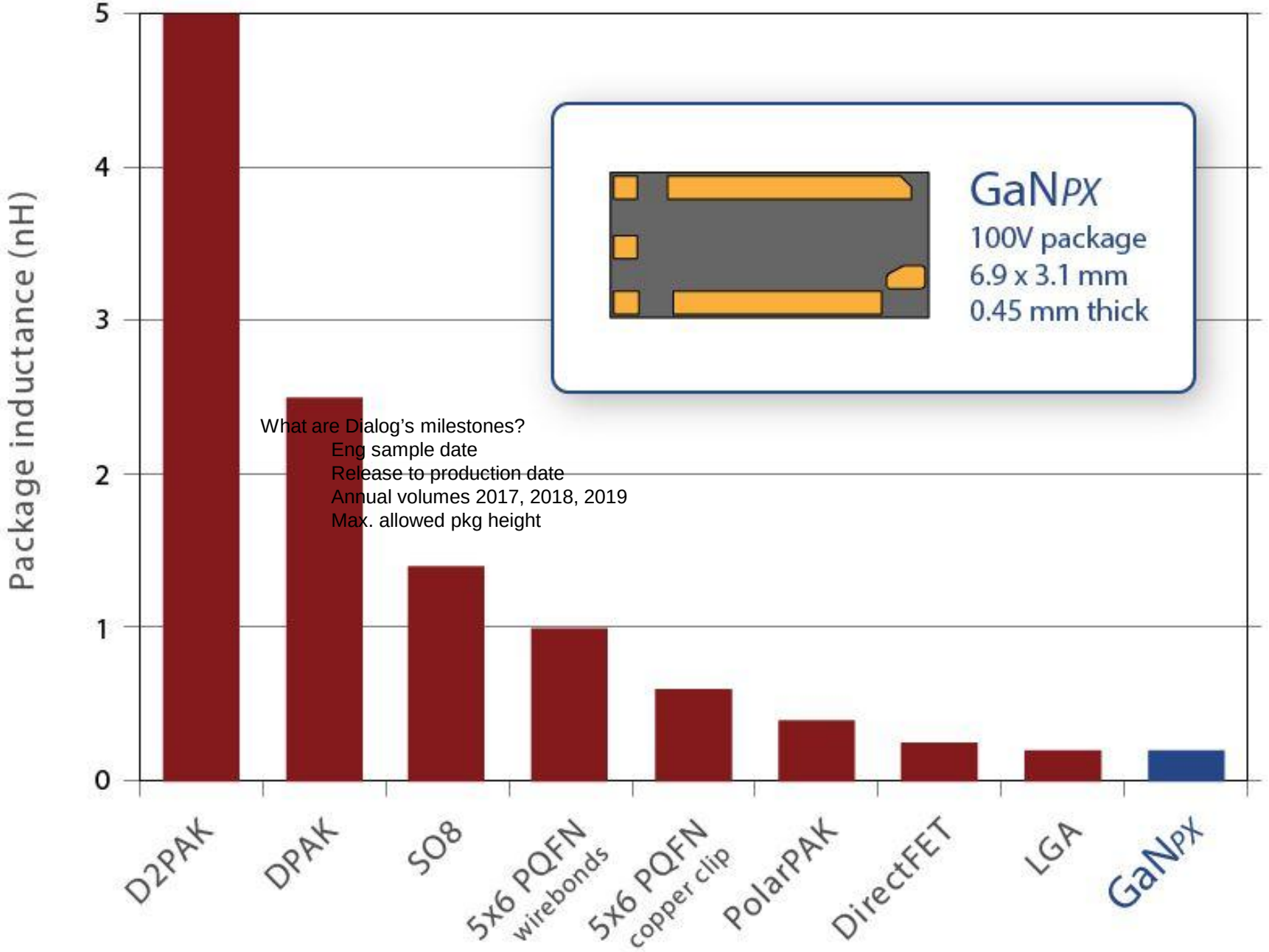


Source: GaN Systems, AT&S IMAPS 2014





Package Inductance Ranking

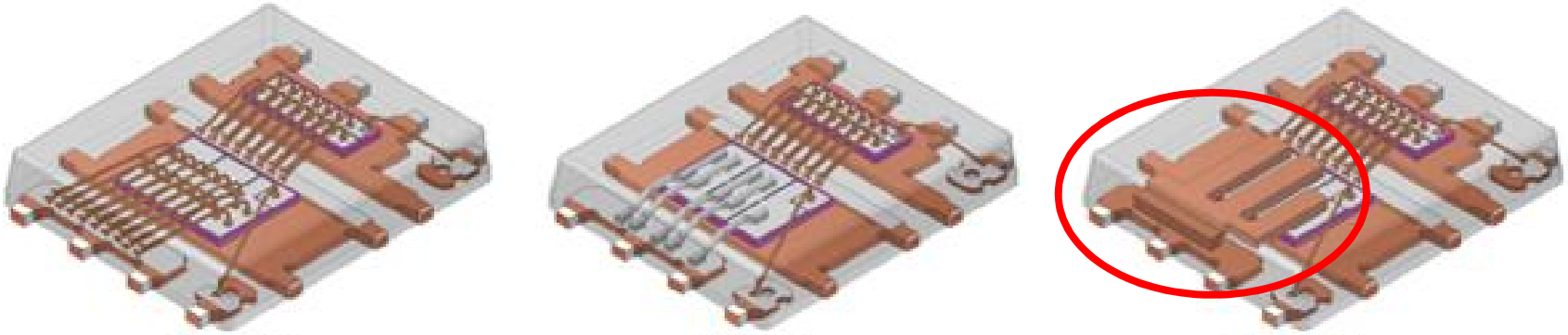


Source: GaN Systems / AT&S IMAPS 2014

Power QFN with Cu Clip

Replaces traditional wire bond interconnection, used for high performance MOSFETs (reference DrMOS)

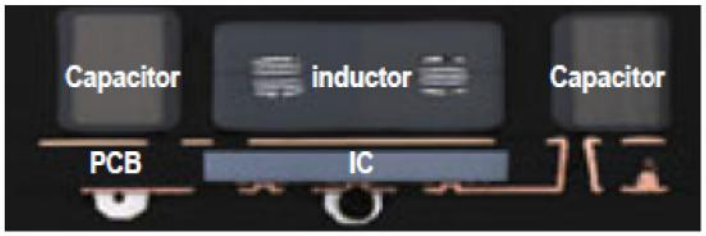
- Cu clip replaces multiple Cu or Al wire bonds
- Cu clip provides lower resistance and inductance than multiple wire bonds
- Cu clip improves thermal performance

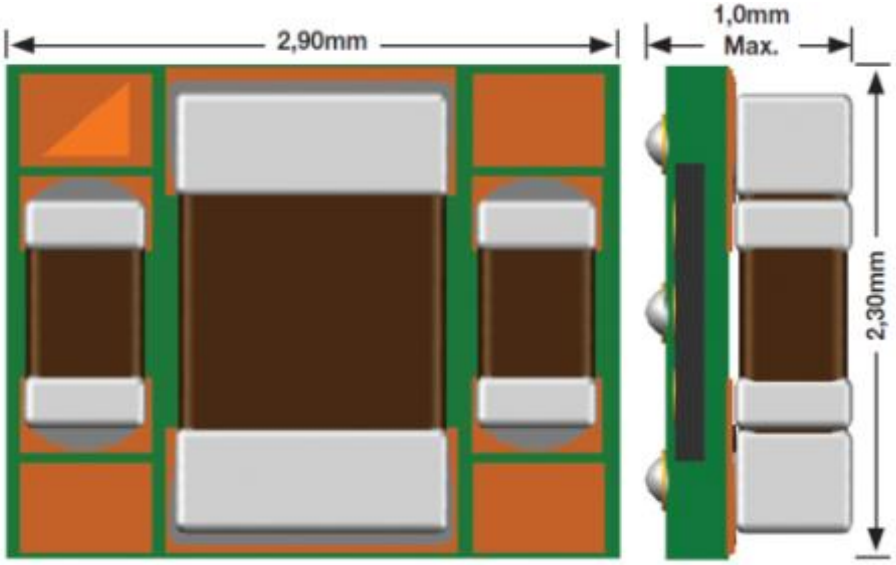


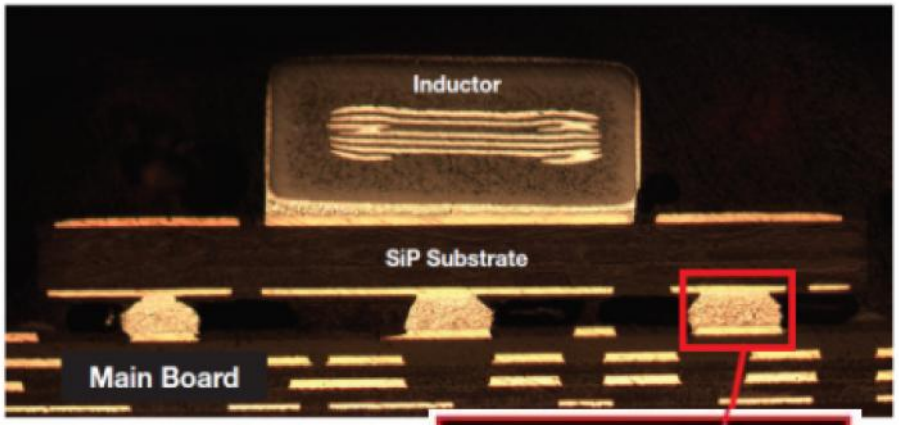
Cu Wire | Al Wire | Cu Clip

*Image Source: Electronic Design

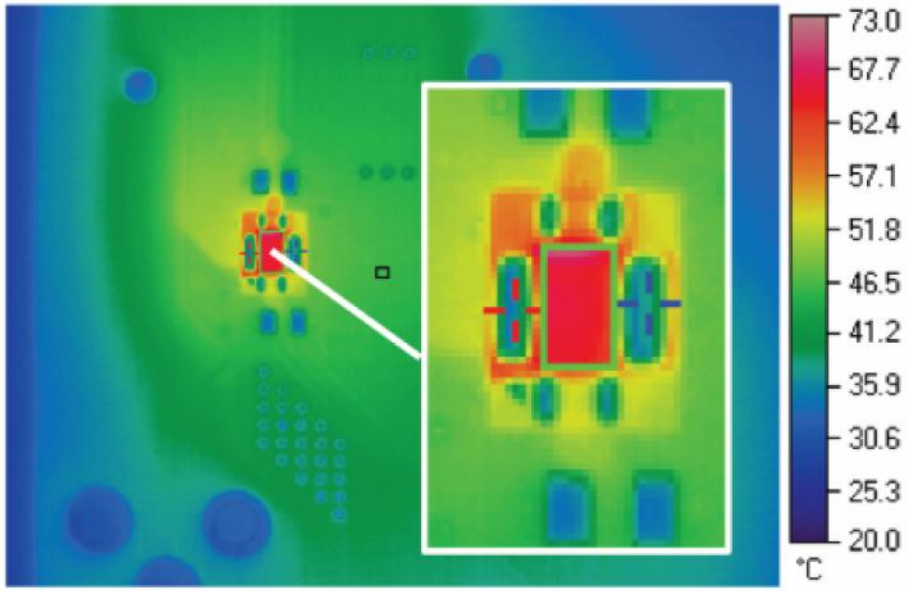
TI MicroSiP™ (Introduced 2011) > 20 products Step-down & Boost Converters







Thermal Evaluation



Thermal Image of MicroSiP™ when IC is dissipating 0.45W. Ambient temperature is 22°C, max junction temperature is 72°C. For thermal modeling, a value of Θ_{JA}=125°C/W provides an excellent initial estimate of thermal performance.

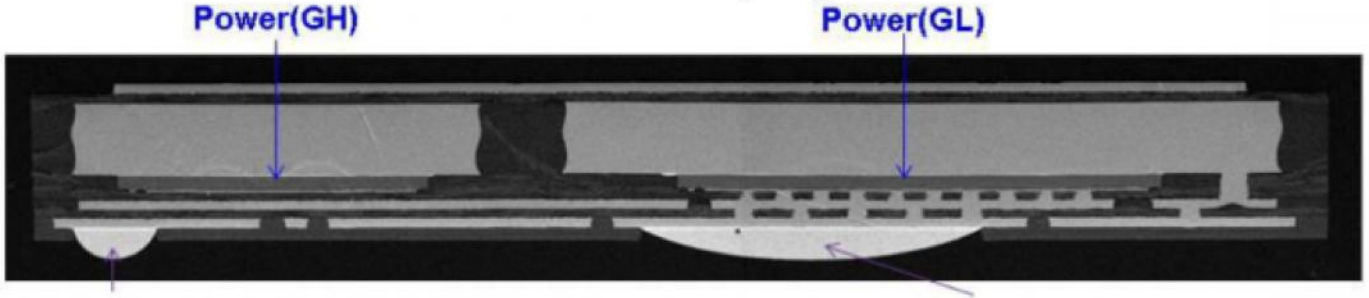
Board-Level Reliability Data

8-pin MicroSiP™

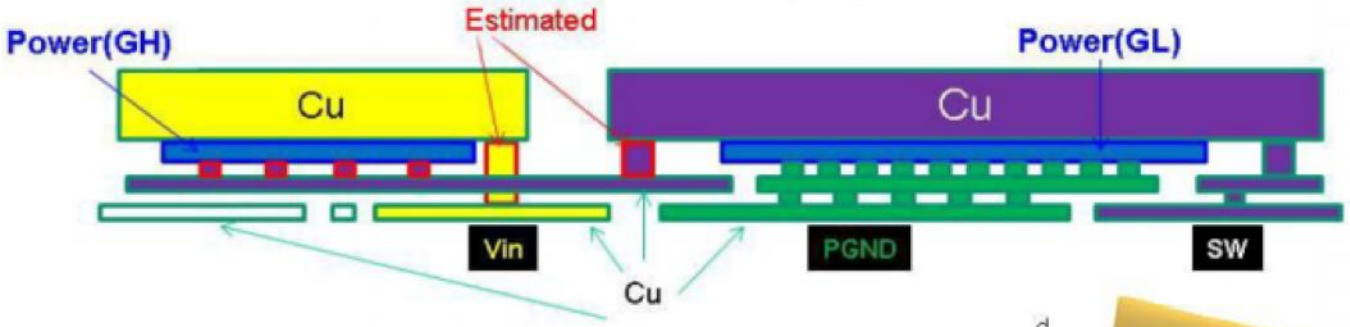
	Test Parameters	Results ($t_{first\ fail}$)
Drop	1500G/1.0ms pulse	> 100 drops
Temp Cycle	-40/125°C, 2 cycles/hr	> 1000 cycles

Embedded Chip Technology – adoption accelerating in Power Applications

Cross section (X-ray)



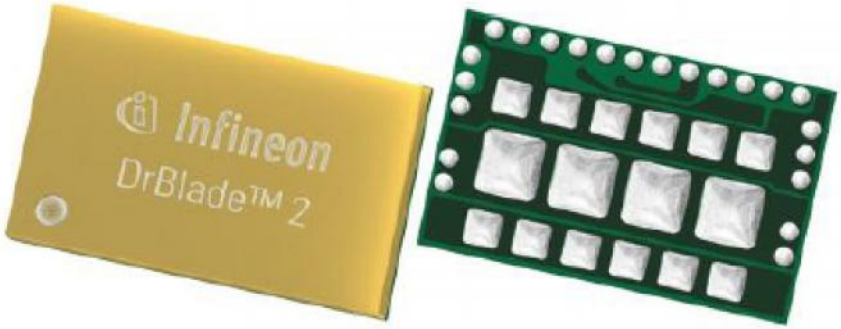
Cross section (SEM)



Embedded Chip Power Solutions also from:

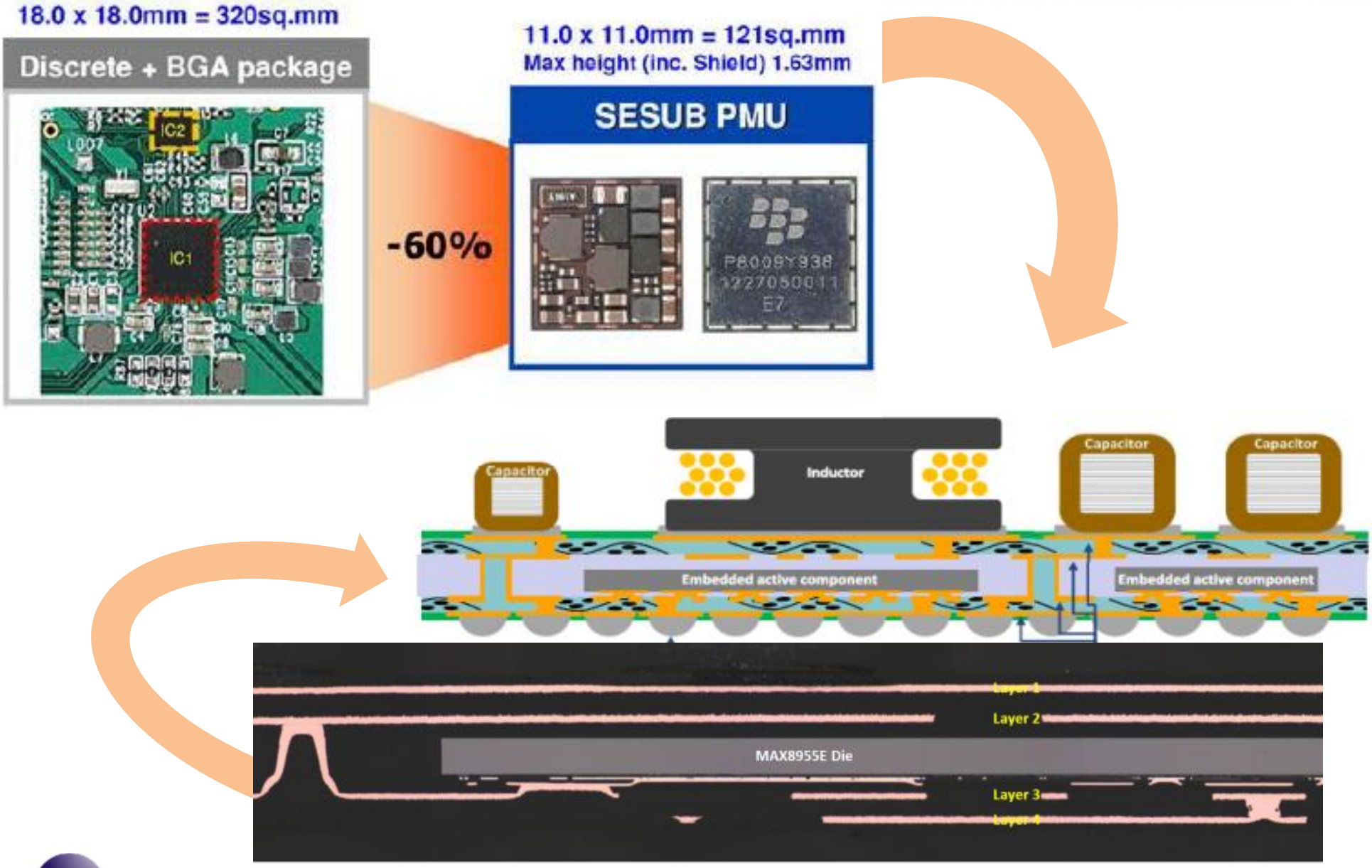
General Electric
Schweizer
TDK

Infineon's embedded chip DrBlade™



Buck converter with driver and high-side and low-side switches

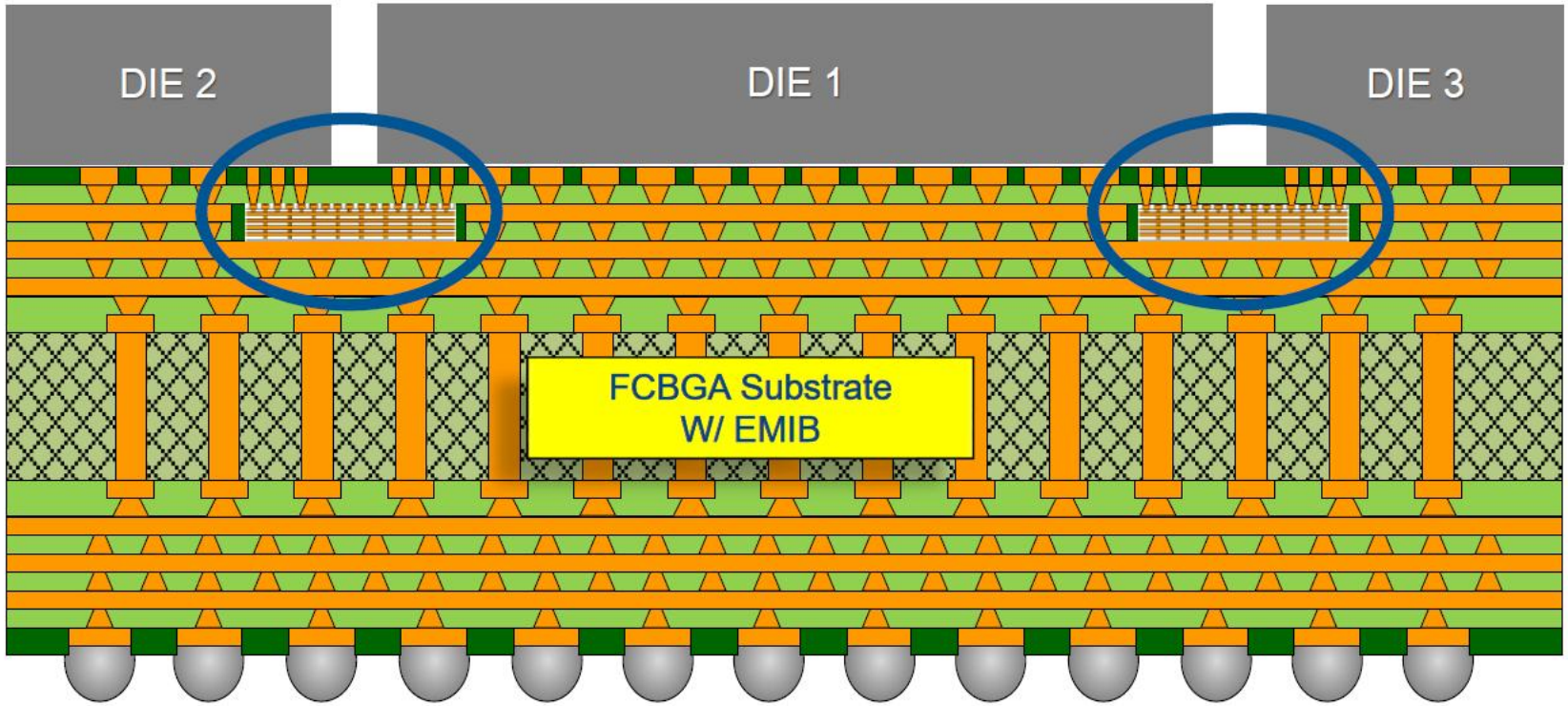
TDK's SESUB Technology shrinks Power Management section 60% in BlackBerry™ Z10 Phone



Cross-section details on MAX8955E

Embedded Chip Technology – for high density / bandwidth 3D Pkg (2.5D architecture w/out TSVs)

EMIB Construction (Embedded Multi-die Interconnect Bridge)



An Alternative Architecture for High Density Multi-Chip Package Connections

Source: Intel Corp. (IMAPS March 2016)

Intel EMIB vs. 2.5D Silicon Interposer: Evaluation Matrix

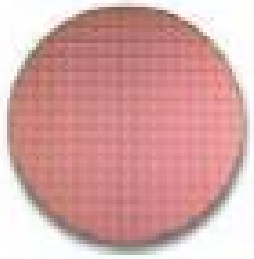
	Silicon Interposer	EMIB
Wiring Density		
Chip-to-Chip Signal Integrity		
Through Package Signal Integrity		
Through Package Power Delivery		
Silicon Processing		
Substrate Processing		
Assembly Processing		
Total Chip/Si Area on Package		
Overall Cost		
Final Recommendation		☑

Source: Intel Corp. R. Mahajan keynote IMAPS DPC 2016

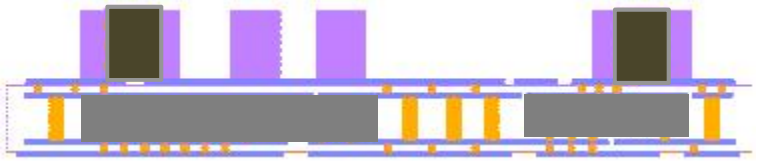
3D SiP Supply Chain UTAC / AT&S Collaboration

Alignment on Design Rules & Roadmaps
- Substrate design
- Assembly design
- Design integration

KGD test
RDL
Thin / Dice
Inspect / TnR



Substrate manufacturing
Embedded chip
Strip Test



SMT
Top FC / under fill
Cap or Mold
Solder Ball Attach
Package saw

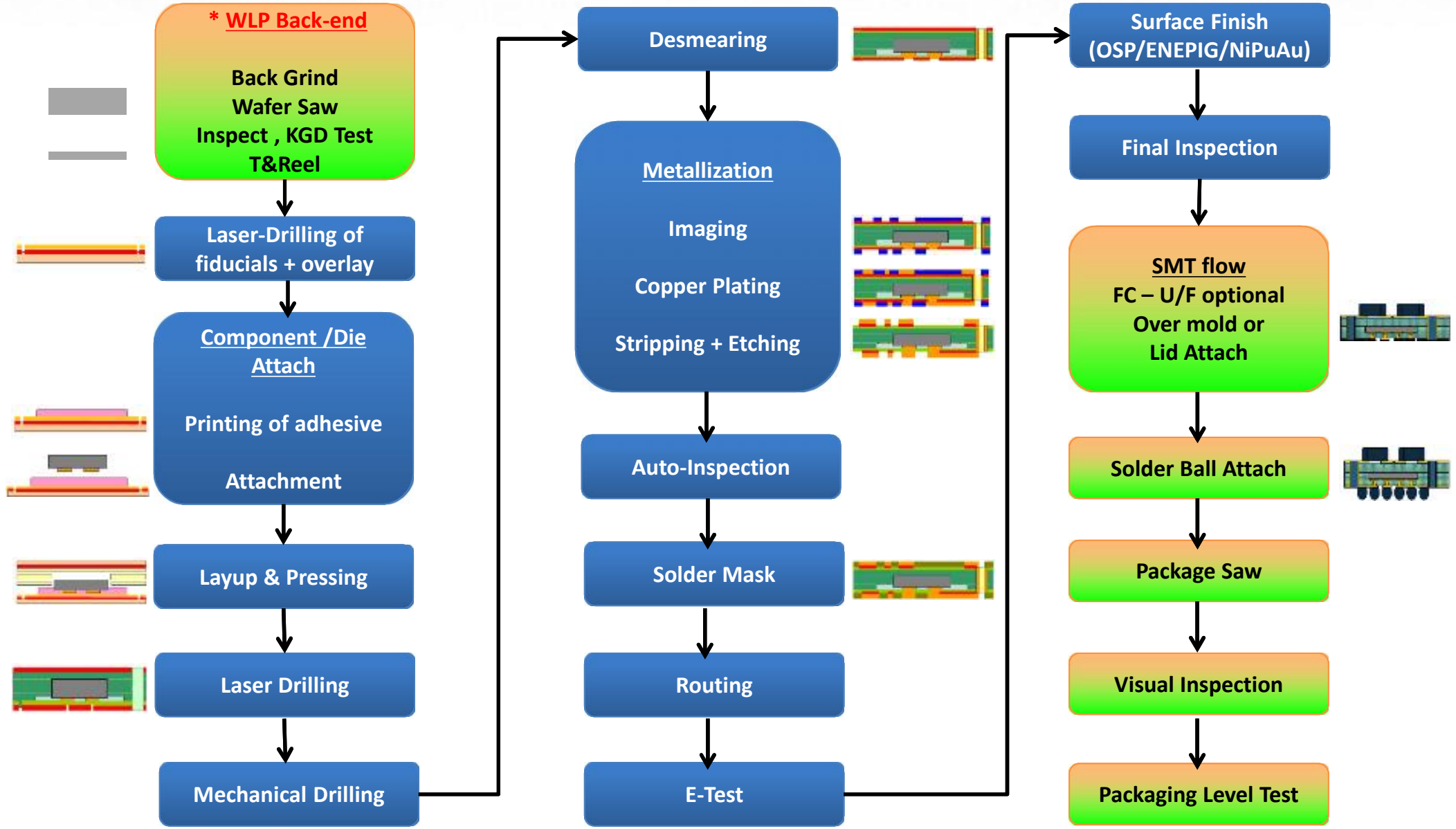
Package level test
Reliability test

Co-Design	Wafer to Die	Substrate embedded chip	Package assembly	Test
UTAC	*Customer Consigned Option*	AT&S	UTAC	UTAC
AT&S	UTAC			
Customer Specs				

April 2015 - Joint marketing / supply chain agreement Between AT&S and UTAC for 3D SiP with embedded chip technology. Collaboration press release April 2016. AT&S over 5 years production embedding experience.

UTAC

UTAC / AT&S 3D SiP Process Flow



AT&S

UDG

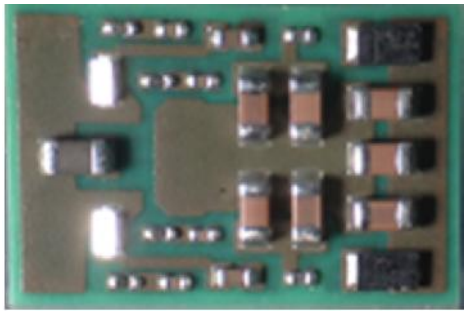
* Die require 5-10um thick Cu pads for embedding at > 200um pad pitch

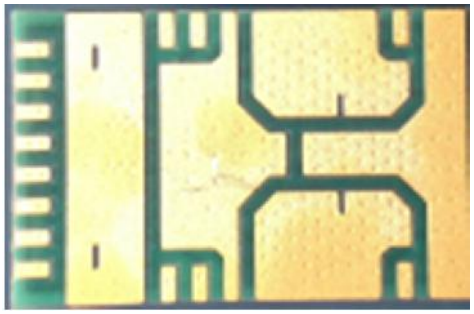
Sarda Technologies Rev. 1 HIPS

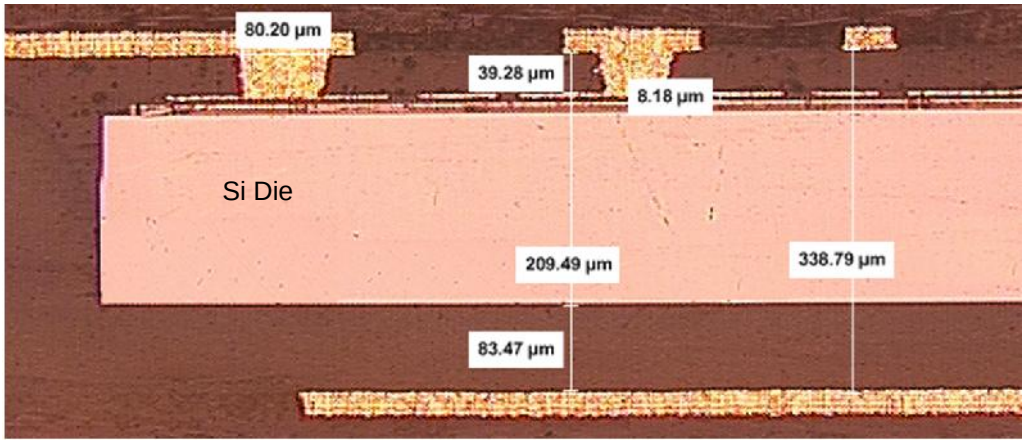
Package Type: 4.5 x 7.2mm LGA-SIP
Highlights: 2 embedded die + 24 passive components on substrate top side

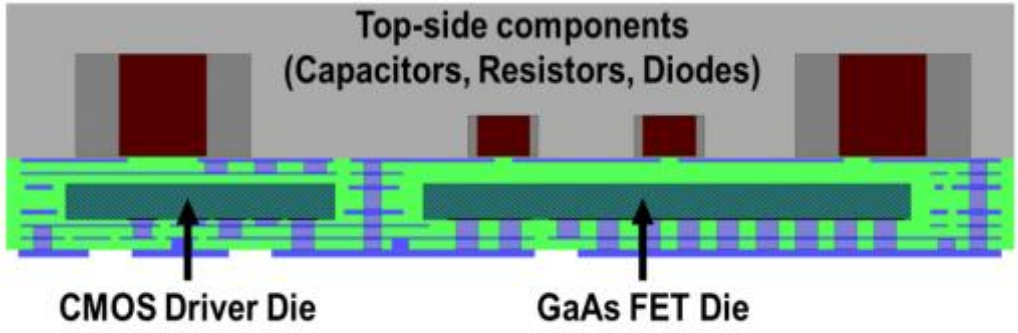
Package size / Type	4.5 x 7.2 mm LGA-SIP
Substrate Thickness	560 um ± 10% 320um core
Die thickness	200 um Max.
Surface finish (Die DAP)	Electrolytic NI/AU
Surface finish (Land Pad)	Electrolytic NI/AU
# of Passive Component (Top of substrate surface)	24ea Passive
Component Sizes	Passive 10ea 01005, 10ea 0402, 4ea 0201.
# of embedded chip	2
Strip Size	188x64mm
Substrate Metal layer	4 Layer

Assy Layout









Courtesy of Sarda Technologies, Inc.

3D SiP with Embedded Chip Reliability Summary

AT&S Reliability Data and UDG Laminate Reliability Requirements

AT&S			UDG Laminate Requirements
Method	**Specification**	**Result**	**Specification**
Moisture Sensitivity Level	Peak @ 260 C	Minimum MSL3	MSL3
Thermal Cycling	-55 C / +150 C	1000cycles passed (TC Grade 1)	-55 C / +125 C ; 1000 cycles
HAST	110 C @ 85%RH @ 5VDC	264 hours passed	uHAST - 130 C/85%RH; 96 hours
High Temperature Storage	@125 C	1000hours passed (TH Grade 2)	150 C ; 1000 hours
Temperature/ Humidity	85 C / 85%RH	1000hours passed (TH Group A)	Per customer
Board bending	5mm/s	80K bends passed	Per customer
Random vibration	3 g (rms) (5-500) Hz	30 min per axis passed	Per customer
Shock	10kg @ 0.2ms	3 per direction passed	Per customer
Reflow sensitivity	Pb-free profile (255 C)	30 cycles passed	Per customer
Drop Test	1500g @ 0.5ms	10 drops passed (MS Group F)	Per customer

PCB:

No of layers: 4
Base material: Panasonic R 1570
PCB size: 120mm x 120mm

Components:

Material: Silicon
Component type: Daisy Chain
Component size: 0.9mm x 0.9mm to 5.9mm x 5.9mm

UDG can perform Reliability Testing as required per Customer Specs.

Summary

- System in a package (SiP) is a strategic focus area for UTAC
- 3D SiP with Embedded Chip provides integration, size and performance benefits over 2D planar SiP solutions
- 3D Embedded Chip technology adoption is accelerating in Power and High Density Interconnect Applications
- Supply chain collaboration with AT&S for emerging 3D SiP solutions with embedded chip technology will advanced the technology and provide FTK supply solution for customers