Parasitic Capacitance in Magnetic Components

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BREAKING NEW GROUND
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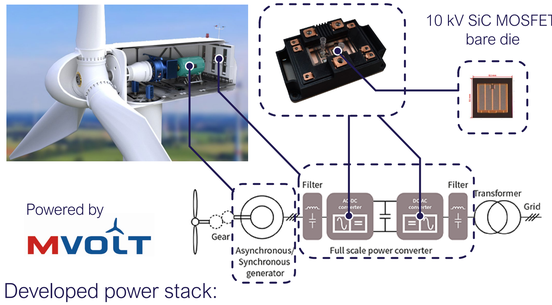
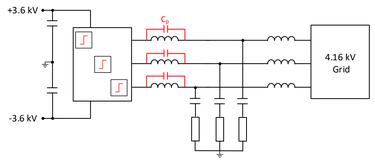
Background



Developed power stack:

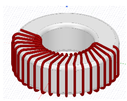
- Efficiency >99 % (measured in 50 kW)
  - Increase 3% efficiency at the full converter stage
  - Save 126 million Danish kroner @ 2022
  - Greener transition with less copper
- Switching frequency: 5-10 kHz
- dv/dt > 100 kV/μs (world record at 250 kV/us)



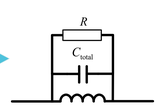
- EMI issues
  - Significant capacitive current circulating in the circuit
- Accelerate the aging of transistors
  - Slow down the switching speed and cause extra losses on transistors

Parasitic capacitance is more important in medium-voltage inductors !

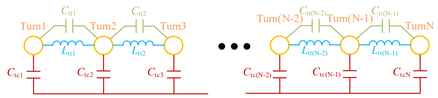
Problem Formulation



Toroidal inductor



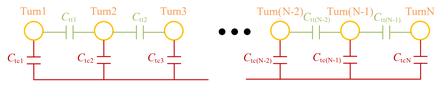
Equivalent circuit (before first resonant frequency)



Discrete-element circuit (without mutual inductance)

Two physic-based analytical method for modelling parasitic capacitance in inductor with applying different assumptions

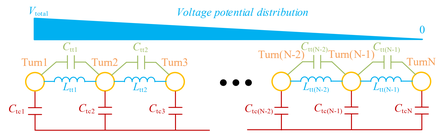
- Lumped-circuit-network method



$$C_{total}(2) = C_{tt} + \frac{C_{tc}}{2},\ C_{total}(3) = \frac{C_{tt}}{2} + \frac{C_{tc}}{2},\ C_{total}(N) = \frac{C_{total}(N-2) \times \frac{C_{tt}}{2}}{C_{total}(N-2) + \frac{C_{tt}}{2}} + \frac{C_{tc}}{2},\ \text{if } N > 3$$

$$C_{total}(\infty) = \frac{C_{tt}}{4}(\alpha + \sqrt{\alpha^2 + 4\alpha}),\ \alpha = \frac{C_{tc}}{C_{tt}}$$

- Energy-conservation method



$$C_{total}(N) = \sum_{n=1}^{N}\left(\frac{(N-n)V_{total}}{N-1} - \frac{V_{total}}{2}\right)^2 \frac{C_{tc}}{V_{total}^2} + \sum_{n=1}^{N-1}\left(\frac{V_{total}}{N-1}\right)^2 \frac{C_{tt}}{V_{total}^2} = \frac{NC_{tc}}{12} + \frac{C_{tt}}{N-1}$$

$$C_{total}(\infty) = \infty$$

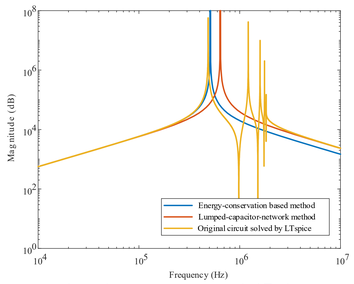
$C_{total}(\infty) = \frac{C_{tt}}{4}(\alpha + \sqrt{\alpha^2 + 4\alpha})$ **VS** $C_{total}(\infty) = \infty$

The total equivalent capacitance of inductor will converge with increasing number of turns

The total equivalent capacitance of inductor will increase with increasing number of turns

At least one of the methods is incorrect to calculate the parasitic capacitance before first resonantfrequency.

Evaluation of Different Assumptions



Impedance measurement in LTspice

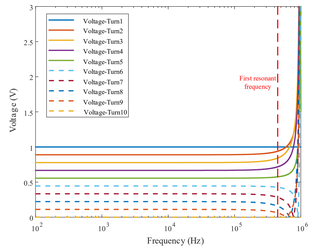
Lumped-circuit-network method:

- more errors around the first resonant frequency
- fit perfectly after the last resonant frequency

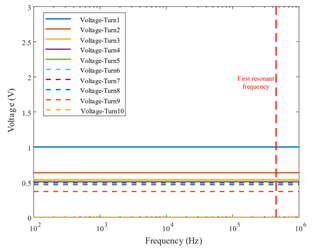
Energy-conservation method:

- less errors around the first resonant frequency

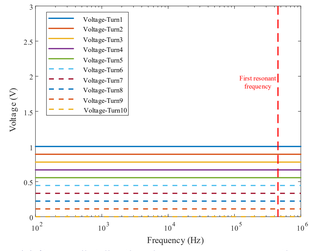
Who is correct? Where do the errors come from?



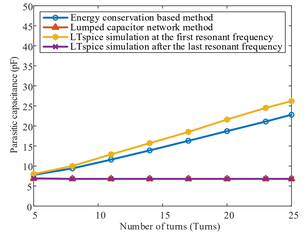
Voltage distribution in original circuit (simulated by LTspice)



Voltage distribution in lumped-capacitor-network (simulated by LTspice)



Voltage distribution in energy-conservation-based method (by assumptions)



Calculation and simulation results of parasitic capacitance

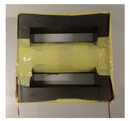
- LTspice simulation:
- Voltage distribution
  - Linear before the first resonant frequency
  - Nonlinear after the first resonant frequency
  - Almost linear around the first resonant frequency
- Parasitic capacitance
  - Be constant with the increasing number of turns after the last resonant frequency
  - Increase with the increasing number of turns at the first resonant frequency
- Lumped-capacitor-network method:

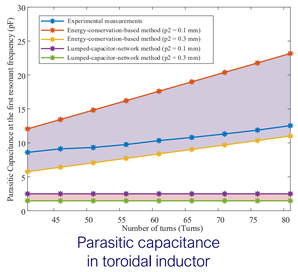
Voltage distribution is nonlinear and parasitic capacitance is constant with the increasing number of turns, which is accurate to predict the parasitic capacitance after the last resonant frequency.

- Energy-conservation based method:

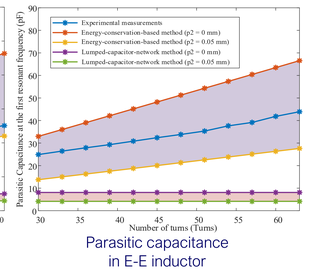
Voltage distribution is linear and parasitic capacitance increases with the increasing number of turns, which is more accurate to predict the parasitic capacitance at the first resonant frequency.

Experimental Verifications





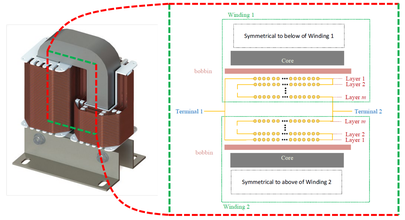
Parasitic capacitance in toroidal inductor



Parasitic capacitance in E-E inductor

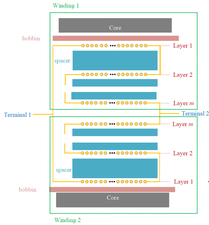
Energy-conservation based method is more accurate to predict the parasitic capacitance at the first resonant frequency.

Reduce Parasitic Capacitance



1020 pF
30 mH

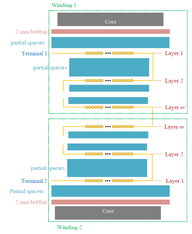
- Insertion of spacers



79.1pF
30 mH

Pros:
Parasitic capacitance contributed by two adjacent layers can be significantly reduced
Insulation strength can be icreased
Cons:
Power density will be slightly increased

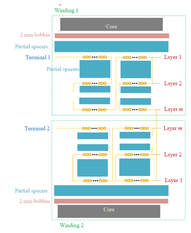
- Using series connections in multiple windings



17.2pF
30 mH

Pros:
Parasitic capacitance contributed by two adjacent layers can be reduced by 50%-75%
Cons:
Parasitic capacitance contributed by winding and core will be slightly increased
Only applicable for multiple-winding strcture

- Using 'multi-section' windings



7.1 pF
30 mH

Pros:
Parasitic capacitance contributed by two adjacent layers can be reduced by 50% with two sub-sections
Cons:
Parasitic capacitance contributed by winding and core will be slightly increased
Manufacture complexity is significantly increased

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Innovation Fund Denmark

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