MicroWatts AC-DC Conversion IC Design for Vibration and RF Energy Harvesting

Presented by
Mike Hayes for Wensi Wang, Jiaqi Yu
Beijing University of Technology

Wednesday, March 20, 2019
1. Research Background

2. Purpose And Significance

3. Circuits Implementation

4. Simulation Results

5. Conclusion
Solar energy, thermal energy and vibration energy are the main sources of today's energy harvesting technology. For vibrational energy, there are many forms of ambient source, such as:

- Human Walking (Sport)
- Vehicle Movement (Engine)
- Train Vibration (Track)
Typical vibration energy harvesters are mainly divided into three types: electromagnetic, capacitive and piezoelectric. The piezoelectric energy harvester (PEH) is usually formed in a cantilever-beam structure.

MIDE V22B (The PEH)  
Cantilever-beam Structure  
Equivalent Mechanical Model
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In this paper, the PEH is used as the input excitation source. So we design a Power Management IC based on Parallel-SSHI (synchronized switch harvesting on inductor) technique in a 0.18-µm CMOS process.

Diagram of efficiency changing with frequency for different input voltage

Equivalent Electrical Model

VEH Model

R_M L_M C_M C_P V_P

interface circuit
Comparing with the FBR*, Parallel-SSHI technique:

- shortens the flipping time
- prolongs the charging time at high potential
- reduces the loss of charge
- enables a high voltage change rate to the inductor.

*Schematics of FBR (left) and P-SSHI (right) connected to a PEH and its operation waveform

* FBR = full bridge rectifier
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Circuits Implementation

A. System Architecture

High-precision current reference

Charge Transfer Logic Circuit

External resistors to adjust max power point

Optimal efficiency point following (OPP) module

Current Reference

PEH

P-SSHII

AR

Cbuf

OPP

LDO
(External Load)

Cbuf

C_buck

External

Vsd

CTL

SW_{ad}

CG

Optimal efficiency point following (OPP) module

External resistors to adjust max power point
**Circuits Implementation**

**B. Charge Transfer Logic Circuit (CTL)**

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**Step 1.** The charge switch control circuit is running. It charges the inductor in the flipping time by controlling the transmission gate.

**Step 2.** The transmission gate is open. The discharge switch control circuit is running. It transfers the charge stored in $L_P$ to the output capacitor $C_{buf}$.

* The red line and green line are the current paths.
Circuits Implementation

C. Optimal Power Point Following

**Step 1.** Its role is to maintain the $V_{buf}$ at the voltage of optimal power point ($V_{buf,op}$). $V_{buf,op}$ is calculated using the harmonic balance method.

**Step 2.** It is used to control the switch $SW_{B2}$, so that the reverse current is released to form a new current path to prevent the output voltage from falling.

**harmonic balance method:** This theory describes the mathematical relationship between the vibration input source and the optimal power point.

$$V_{buf,op} = \frac{\pi V_M}{8 \left(1 - \frac{\pi^2}{4} (1 - \eta_F) f_C \eta_P\right)}$$
D. High-precision Current Reference

The differential current of the first stage bias current and the desired high-precision current is diverted to the BIAS3 and BIAS4 branches.

Simulation waveform of first stage bias current (green, above) and desired high-precision current (red, below).

Needed to generate high precision V into CTL circuit to optimise operating point and minimise flip losses.
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Simulation waveform of system. The PEH model parameters were set up: $R_M = 64.1k\Omega$, $C_M = 58.6pF$, $L_M = 8.2kH$, $C_P = 20nF$. $V_{buf}$ reached 4.1V at stable time.

Efficiency waveforms for different $V_{buf}$ peak efficiency can reach 83.2% in 3.3V (this paper).

Typically operated a few volts up to 5V max.
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Conclusion

- A system using a parallel-SSHI interface with power management has been designed and fabricated in a 0.18-μm CMOS process.
- Through the OPP, this system can be operated in the most efficient state.
- The CTL module uses a **small scale logic circuit** to achieve charge transfer.
- High-precision current reference enables the external load to provide a **more stable reference voltage and improve system flexibility**.
- Compared with the low efficiency of FBR structure, the **peak efficiency can reach 83.2%** in this paper.
Contact Info:

wensi.wang@bjut.edu.cn