Packaging Considerations in a High Power Density Inverter

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University of Arkansas

Applied Power Electronics Conference

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Outline

- **UA Power Capabilities and Focus**
- **Integration Basics & Heterogeneous Integration**
- **Design Automation for Heterogeneous Integration**
- **UA Packaging Highlights**

UA Power & Energy Team

1. **Simon Ang**, *power packaging, IC design, power converter design*
2. **Juan Balda**, *power systems and power electronics*
3. **Zhong Chen,** *devices and fabrication*
4. **Jia Di**, *asynchronous digital IC design, cybersecurity, hardware security*
5. **Jeff Dix,** *analog & mixed-signal IC design, neural networks*
6. **David Huitink**, *thermal management, packaging, and reliability*
7. **Qinghua Li**, *cybersecurity*
8. **Fang Luo**, *power conversion, motor drives, and packaging*
9. **Alan Mantooth**, *semiconductor device modeling, CAD, packaging, and power & analog IC design, cybersecurity*
10. **Roy McCann**, *motor drives, storage, cybersecurity, and controls*
11. **Yarui Peng**, *design automation tools*
12. **Greg Salamo**, *materials and devices, nitrides*
13. **Morgan Ware**, *wide bandgap devices, capacitors*
14. **Yue Zhao**, *motors, machines and drives*

UA Power Capabilities

High Density Electronics Center (HiDEC)

Assembly

- Dicing Saw
- Wire Bonders
- Flip Chip Bonders
- Soldering Stations

Reliability

- Delta Environmental Chambers
- Thermal Shock Chamber
- Hirayam Pressure Cooker

LTCC Fabrication

- LTCC fabrication
- Vacuum reflow oven
- nScypt 3D Printer

Thin Film

- Cleanroom facility
- E-beam Evaporator
- Suss Microtec Aligners
- Plasma Therm RIE
- Chemcut Spray Etcher

Analytical

- Multipurpose Bondtester
- Buehler Polisher
- CNC Milling Machine
- Makerbot 3D Printer

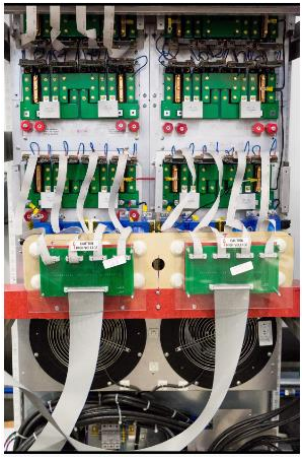
UofA Power Capabilities

National Center for Reliable Electric Power Transmission (NCREPT)

- 12,500 sq. ft state-of-the-art test facility
- (3) 2 MVA Regenerative Electronic Loads
- 10-ton Chiller Unit and Heat Exchanger
- Voltage Range: 15 kVac; 1.5kVdc
- Research Focus:
  - Power Electronics Design, CAD and Modeling
  - Power Electronics Packaging
  - Power Electronics Test
  - Mixed-signal Integrated Circuit Design
  - Sensors
  - Controls

Vertical Integration IS the UA's Strength and Uniqueness

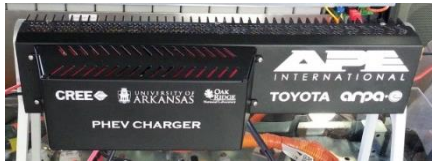
Packaging for High Power Density Inverters

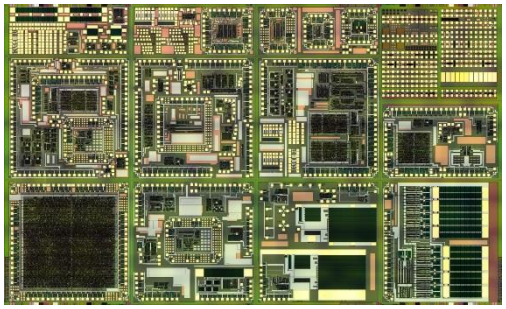


System Prototyping & Demonstrations

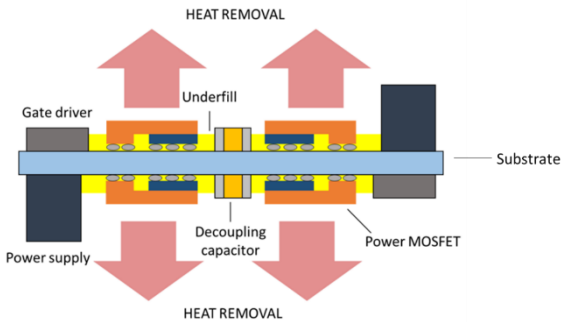
Control Systems

Power Electronic Circuits & Systems



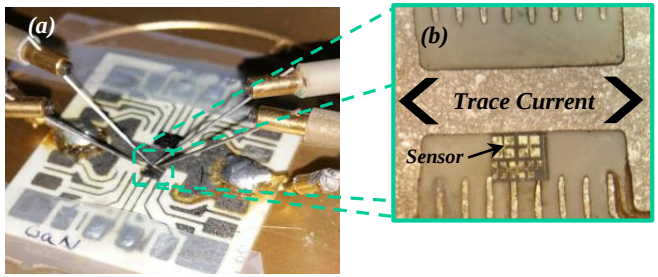


Advanced Integration



Integrated Circuits

Electronic Packaging



Devices

Materials

"Materials to Systems"

Integration Basics

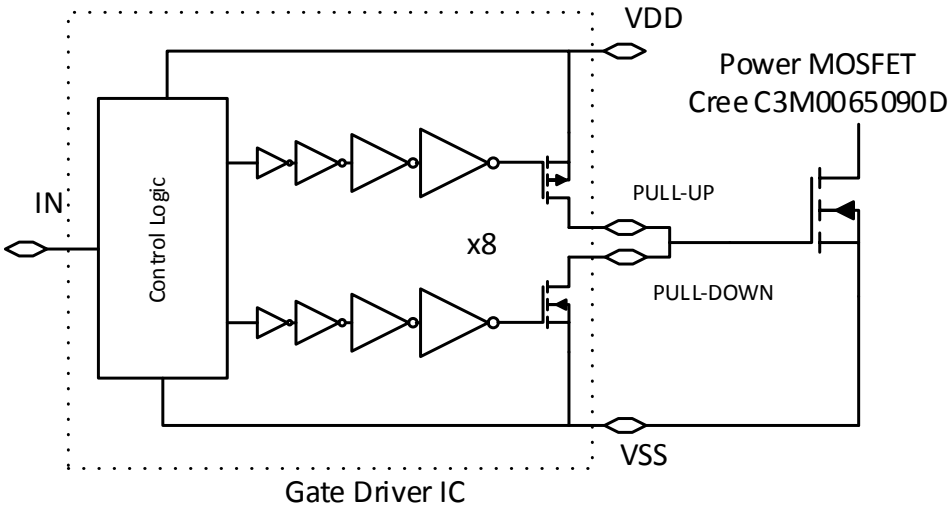
- **Size and weight reduction is desirable in most applications**
- **Higher switching frequencies can deliver reduced size and weight -> smaller passives to deliver power**
- **Can come with penalties such as EMI**
- **Must contend with higher frequency effects (parasitics)**
- **Demands a more integral approach to design and realization**

Heterogeneous Integration

Integration involves combining all of the following in a simultaneous electrical, thermal, and mechanical design:

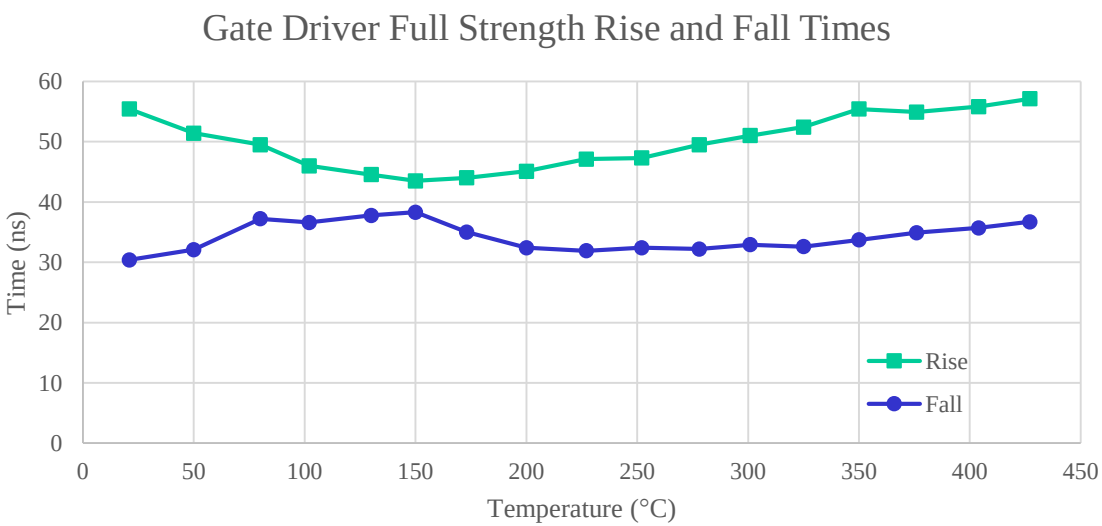
- **Devices**
- **Device models & modeling of the module**
- **Thermal management methods, new materials and devices**
- **Electrical performance (efficiency, integrity, isolation), new materials**
- **Mechanical performance, new materials**
- **Layout optimization (current sharing, EMI)**
- **IC design (supply, driver, control, protection, communication)**
- **Integration of passives**

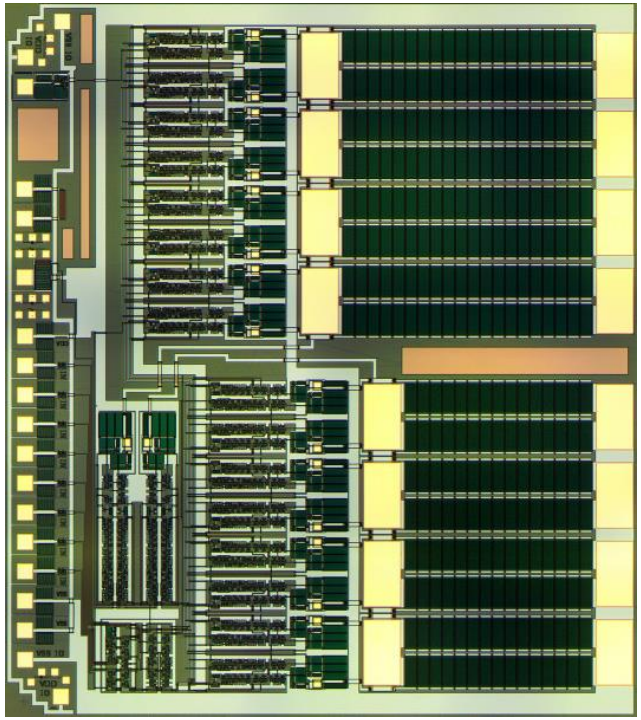
Gate Driver Circuit



Features

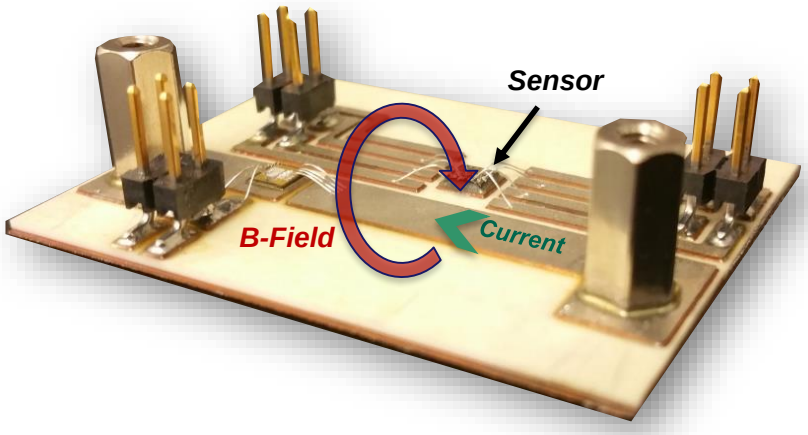
- ***Variable drive strength***
- ***Built-in test***
- ***Operational to over 400 °C***

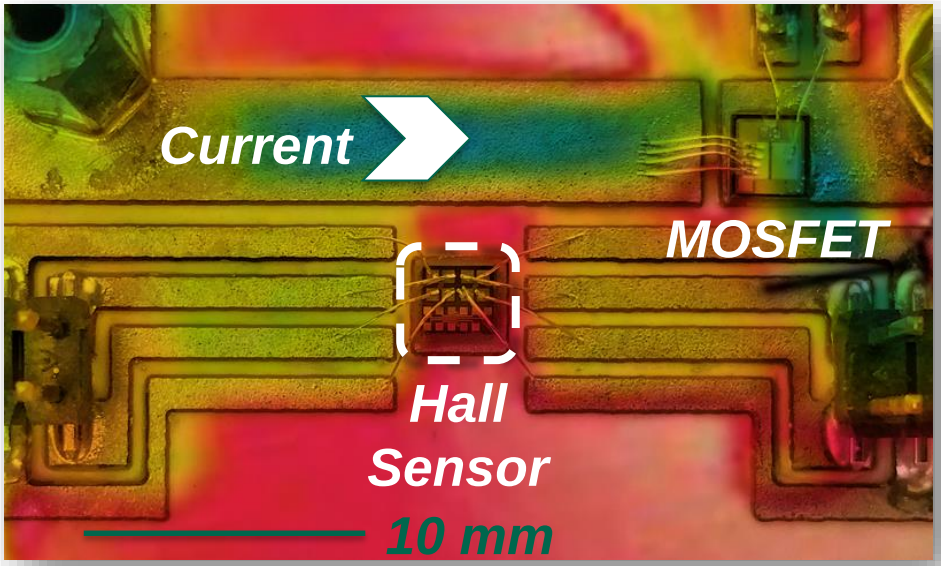


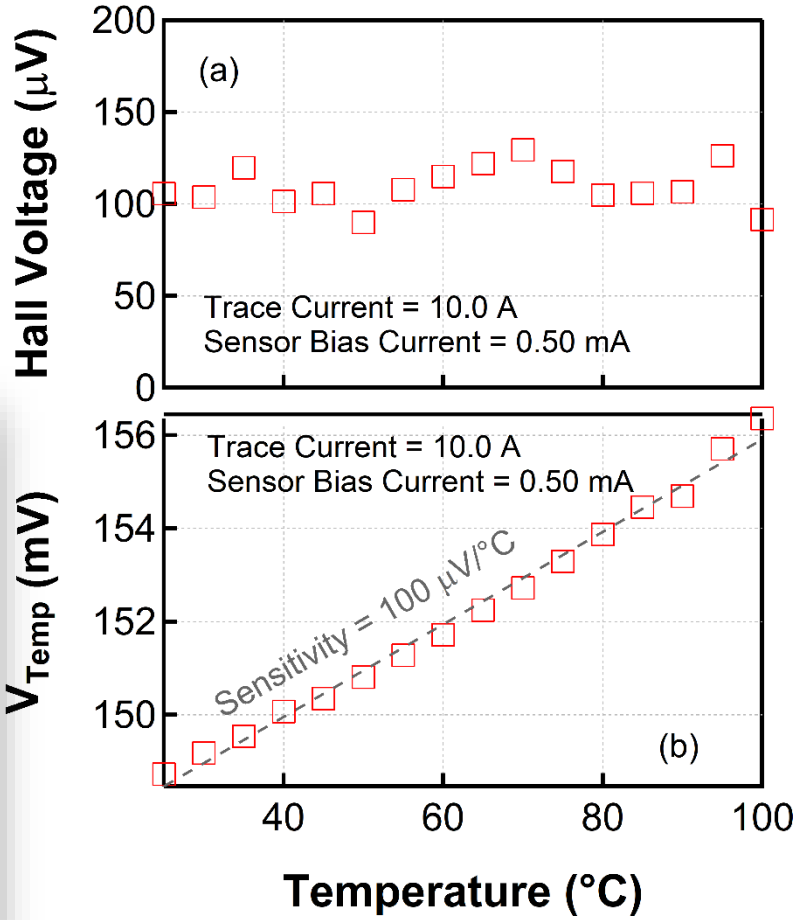


Simultaneous Current and Temperature Measurements

Packaging for High Power Density Inverters





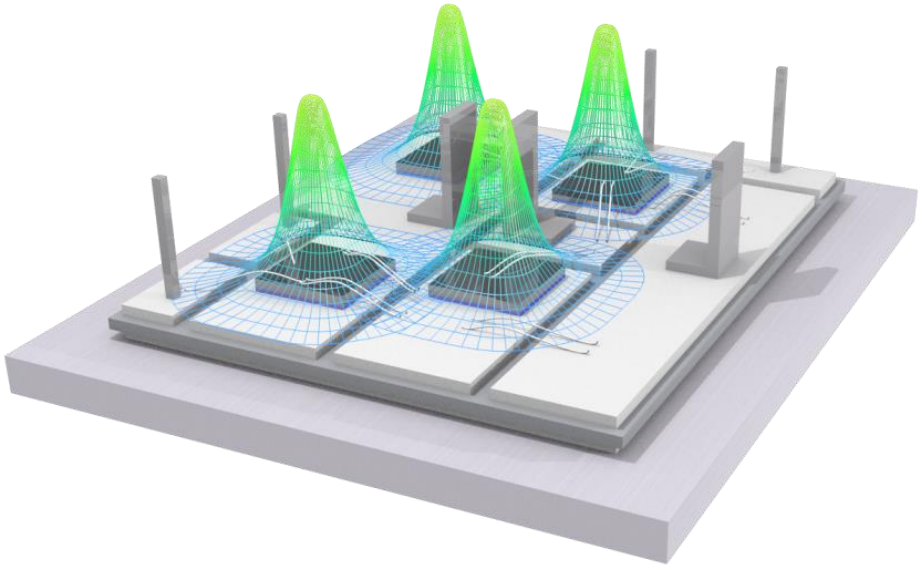


Alan Mantooth, University of Arkansas

Heterogeneous Integration

1. **To achieve the best performance out of WBG device advances, attention must be paid to electronic packaging.**
2. **Reduction of parasitics, higher frequency operation, thermal management, and long-term reliability mandate integration of a variety of technologies beyond the WBG die.**
3. **This requires advances in materials, packaging processes, and design tools.**

Multi-Chip Power Module Layout Synthesis Tool - PowerSynth

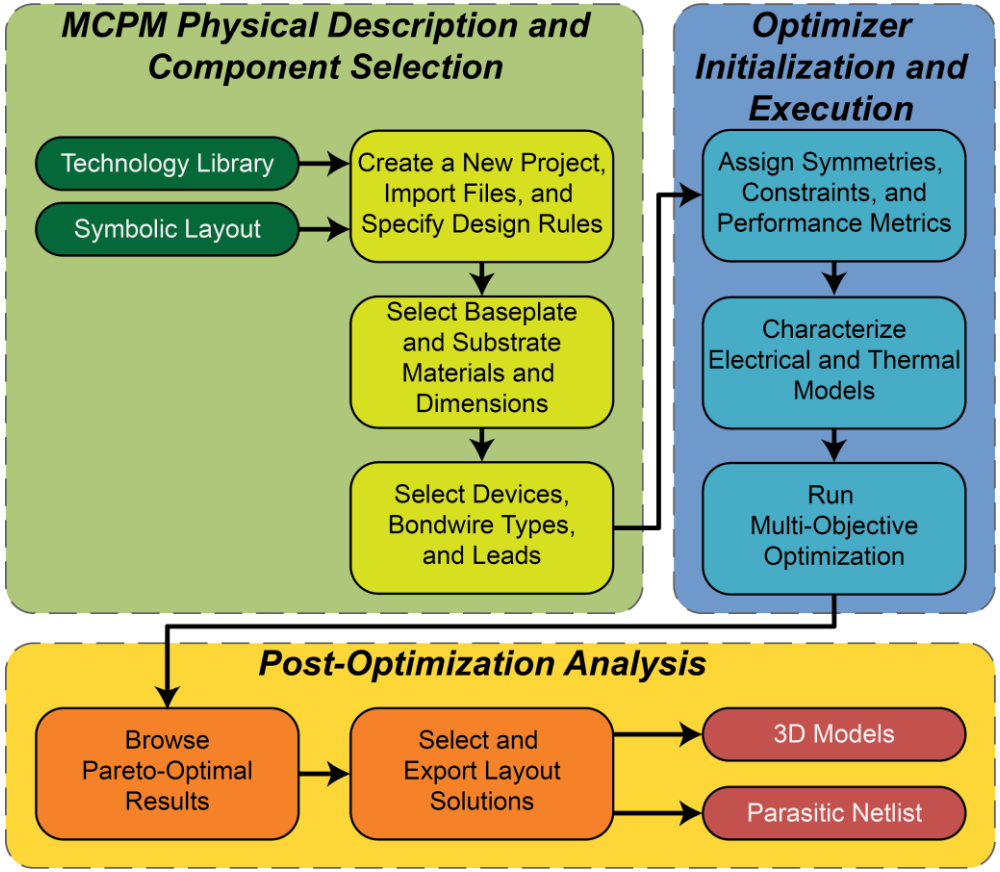


A software tool for the design and layout of multi-chip integrated power modules

PowerSynth Overview

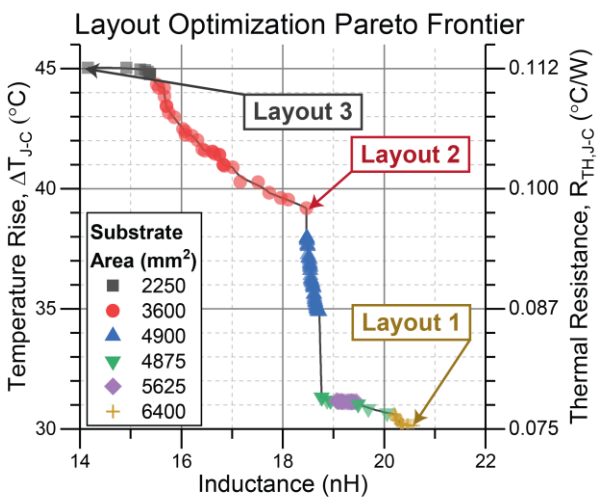
- **Explore the design spaces of integrated power modules**
- **Uses fast thermal and electrical models to gauge power module performance quickly**
- **Multi-objective optimization allows for many trade-off design solutions to be considered**
- **Easily export design solutions to FEA tools**
- **Current work:**
  - **New layout engine toward 3D layout optimization**
  - **New PEEC-based electrical model**
  - **Conducted EMI prediction**
  - **Post-layout optimization for partial discharge reduction**

PowerSynth Workflow

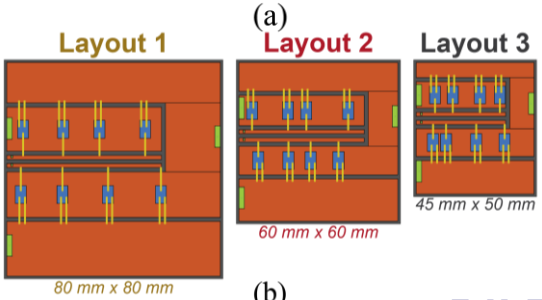


PowerSynth Features

- **Users can choose designs from a Pareto frontier of tradeoffs and export for further analysis:**
  - **Parasitics and thermal netlists**
  - **3D EM solvers (Q3D, HFSS, and EMpro)**
  - **SolidWorks**
- **Reduced order models have been hardware validated**
  - **Thermal model shows excellent agreement while capturing multi-chip interaction**
  - **Electrical model accurately approximates inductance and capacitance over wide frequency range**
- **Fast model evaluation: 3-4 orders of magnitude faster than FEA**



(a)



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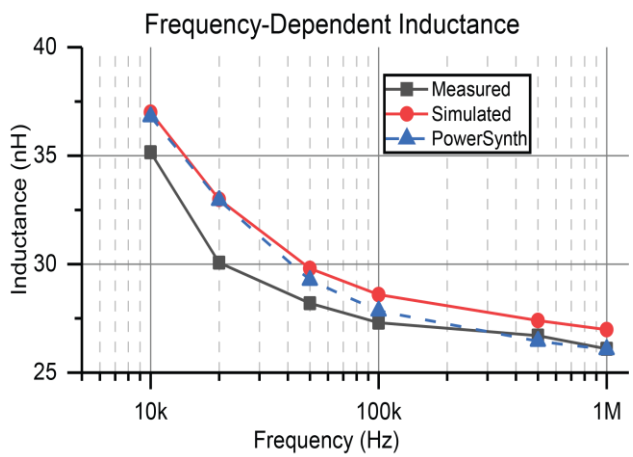
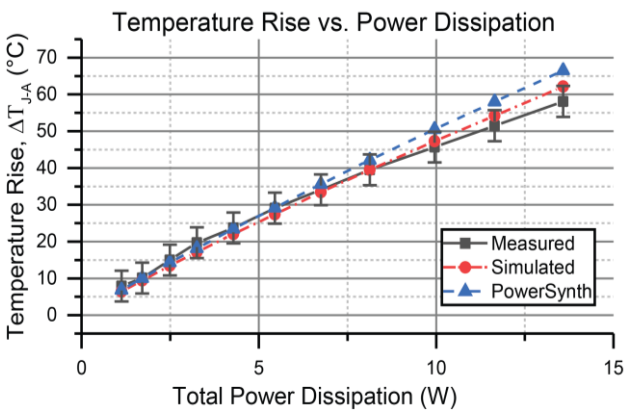
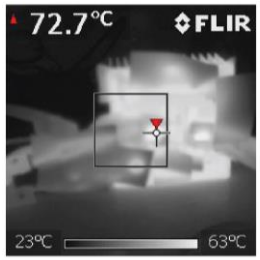
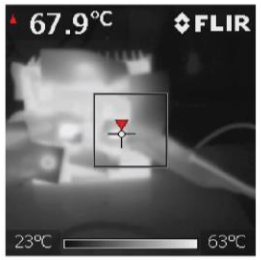








T. M. Evans, et. al, "PowerSynth: A Power Module Layout Generation Tool," IEEE Trans. on Power Electronics, DOI: 10.1109/TPEL.2018.2870346.

Electrical Modeling for 3D

Objective

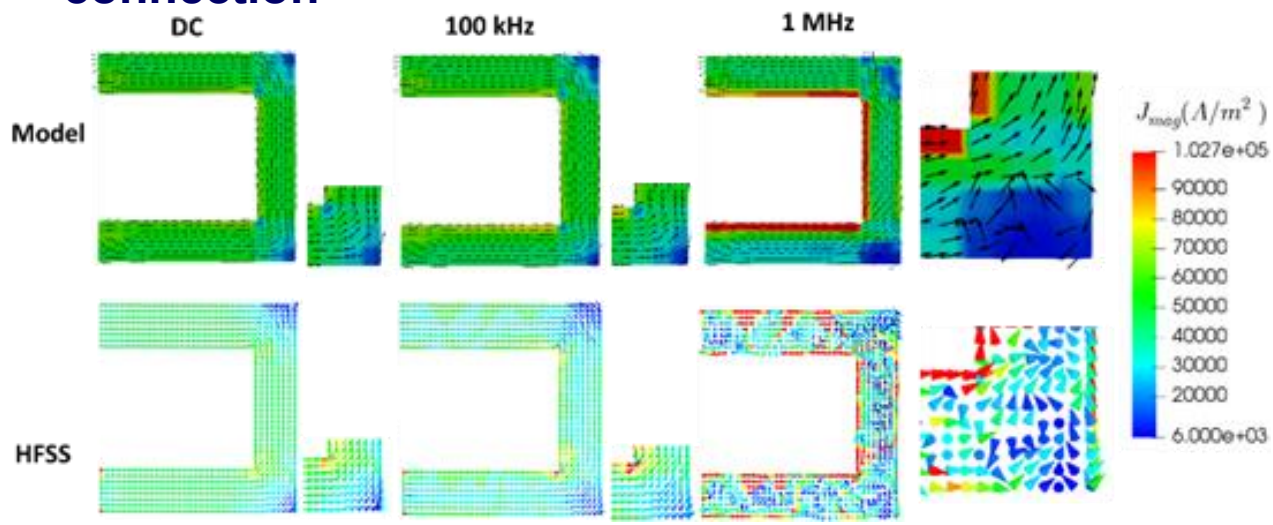
Moving towards 3D structures:

Mutual coupling, electric field, current density need to be considered for more reliable design.

Method	Evaluation Time	# Mesh
Model	30 ms	120
HFSS	180 s	1371

Main approaches

- **Fast electrical parasitics evaluation based on PEEC with coarse mesh**
- **Analytical equations for mutual inductance calculation**
- **Hierarchical representation for devices, bond wires connection**



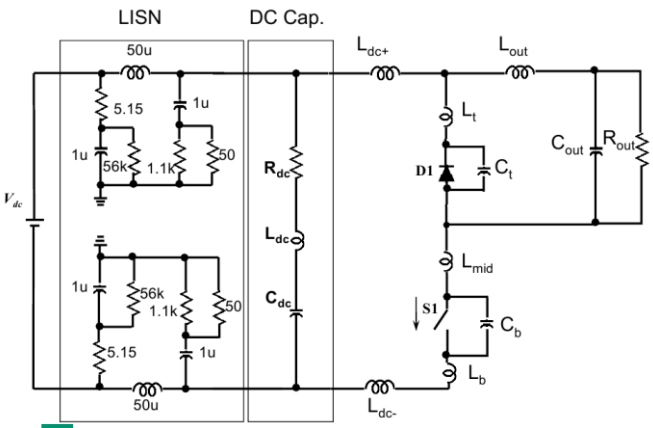
Current density in comparison to Ansys HFSS for a simple U-Shape

PowerSynth EMI Methodology

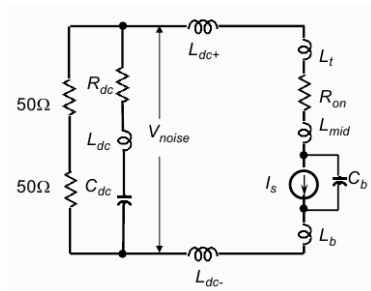
Packaging for High Power Density Inverters

- **Conducted EMI Modeling**
  - Differential and Common Mode noise paths split up
  - Represented as high frequency equivalent circuits
- **Noise Source Modeling**
  - Uses frequency domain representation of trapezoidal waveform
  - Provides approximation of switching current

Example Chopper Circuit



High Frequency Equivalent DM Circuit



Current Source Representation

$$C_n = 2AD\left|\frac{\sin(n\pi D)}{n\pi D}\right| \cdot \left|\frac{\sin(n\pi t_r / T_s)}{n\pi t_r / T_s}\right|$$

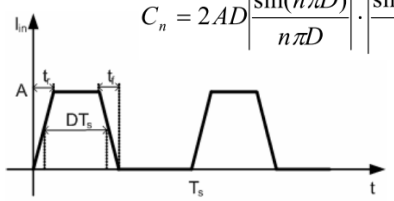


Figure 2-7 Time-domain Trapezoidal Waveform

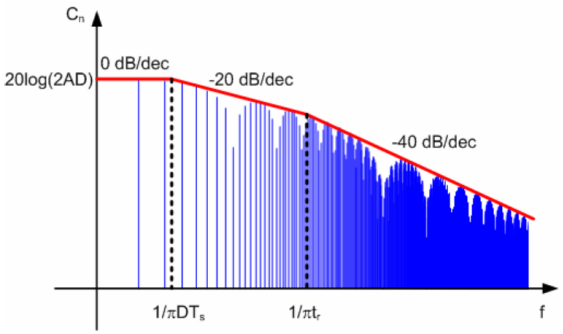


Figure 2-8 Frequency-domain Spectrum of Trapezoidal Waveform

HF Equivalent Circuit
- Built from PowerSynth Netlist
- Incorporates DC Bus parasitics and device C_{oss}

→ **Noise Source Model** →

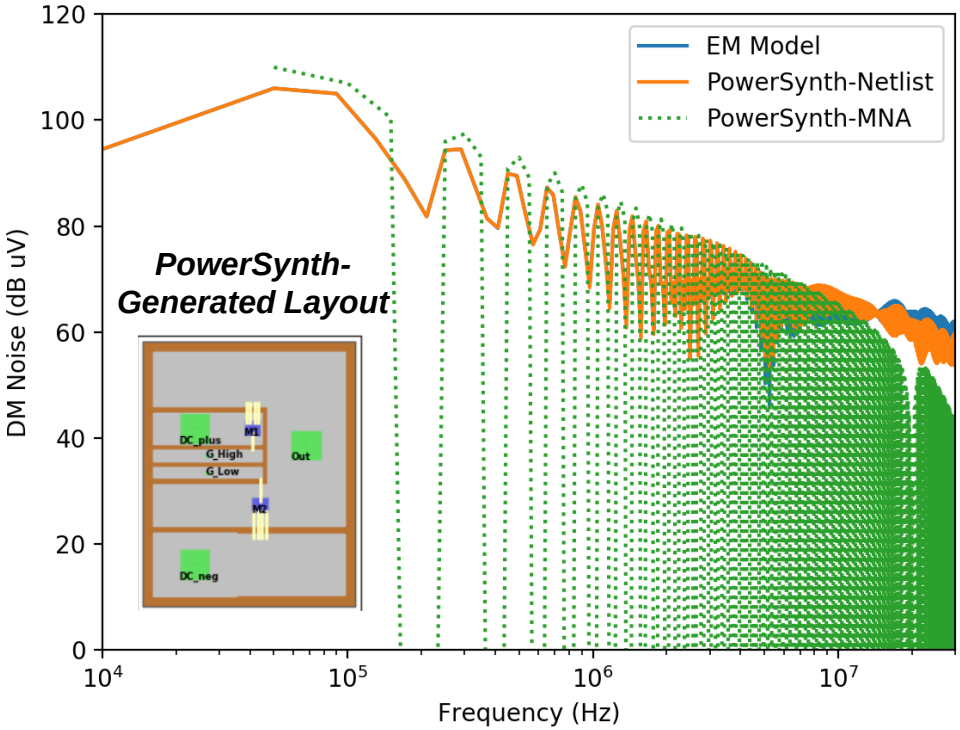
Modified Nodal Analysis
- Frequency domain calculation of HF circuit using Noise Source
- Implemented in Python

References:
- *Q. Liu, Modular Approach for Characterizing and Modeling Conducted EMI Emissions in Power Converters, Doctoral Dissertation, Virginia Tech, 2005.*
- *X. Huang, Frequency Domain Conductive Electromagnetic Interference Modeling and Prediction with Parasisitcs Extraction for Inverters, Doctoral Dissertation, Virginia Tech, 2004.*

PowerSynth EMI Results

- ***Test Setup***
  - ***PowerSynth-generated half-bridge layout***
  - ***Double Pulse Test***
  - ***50 kHz, 25% Duty***
  - ***20 A, tr=tf=50 ns***
- ***Comparison***
  - ***Transient simulation of EM model***
  - ***Transient simulation of PowerSynth-generated netlist***
  - ***MNA frequency response from PowerSynth***

DM Noise Comparison



Currently accurate up to 5MHz, working on implementing broadband parasitics model and C_{oss} nonlinearity

Run Time Comparison

Calculation	Time (s)
Full-Wave Parasitics Extraction	1060
Transient Simulation	200
PowerSynth MNA	**21**

Constraint-Aware Layout Engine

Objective

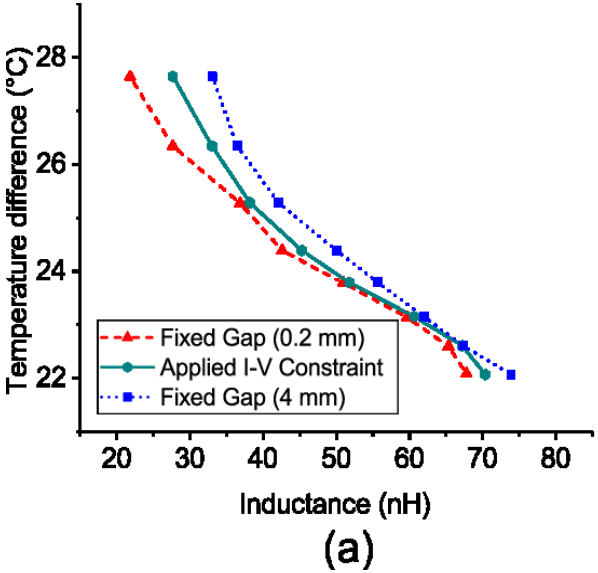
A generic, scalable, and constraint-aware layout engine to create DRC-clean reliable layout solutions with a high efficiency.

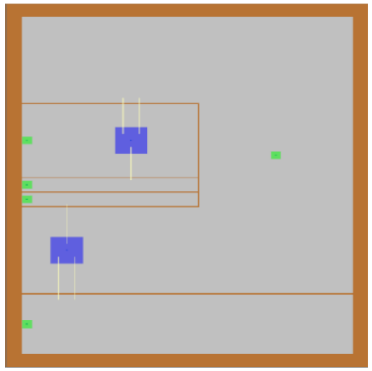
Approaches

- **Corner stitch data structure with hierarchical constraint graph methodology**
- **Scalable, generic, and efficient optimization algorithms**

Progress

- **Implemented both DRC and reliability constraint-aware layout generation in flat-level floorplan[1]**
- **Hierarchical 3D optimization is on-going; Hierarchy consideration reduces coordinate correlation, complexity in both modular and system level optimization**





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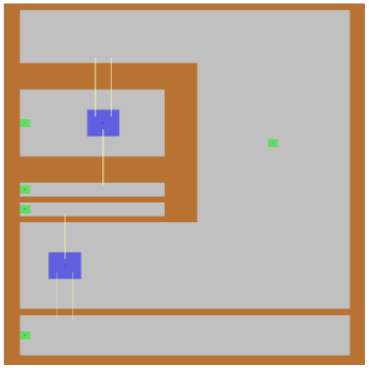

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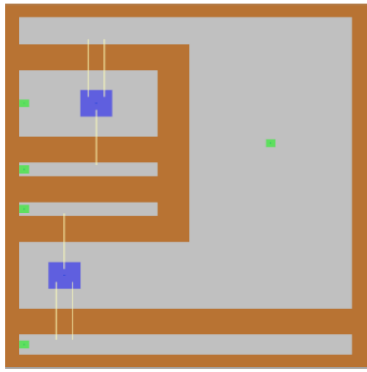


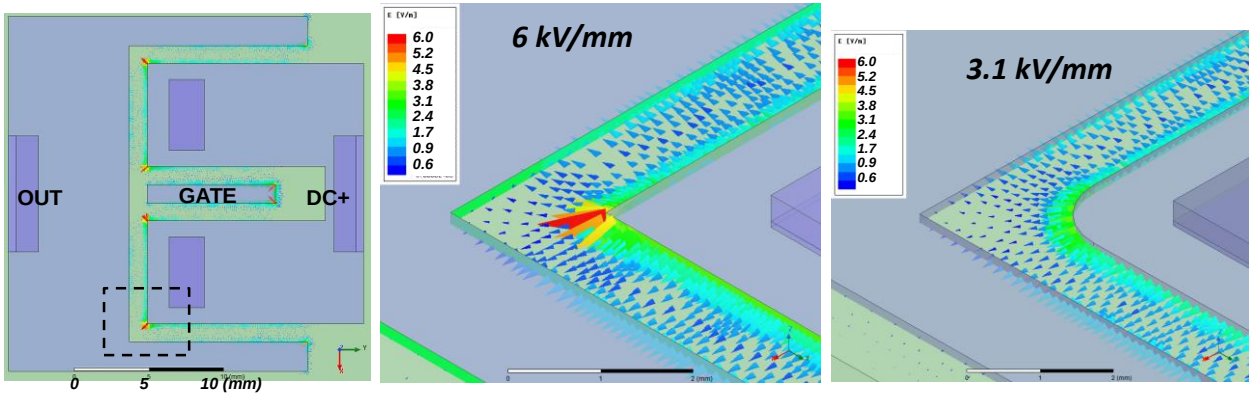
(d)

(a) Three Pareto-fronts of layout solutions. Sample layout (b) with fixed gap 0.2 mm, (c) I-V constraints, (d) fixed gap 0.4 mm

Partial Discharge

Packaging for High Power Density Inverters

Simulations show increased E-field concentration at sharp corners.



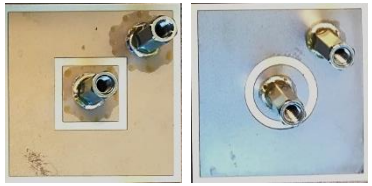
Partial Discharge Tests show increased PD inception voltage for layouts with filleted power traces.

<u>PD Test Setup</u>:
MPS 60, a 60 kV PD Tester available at Wolfspeed.

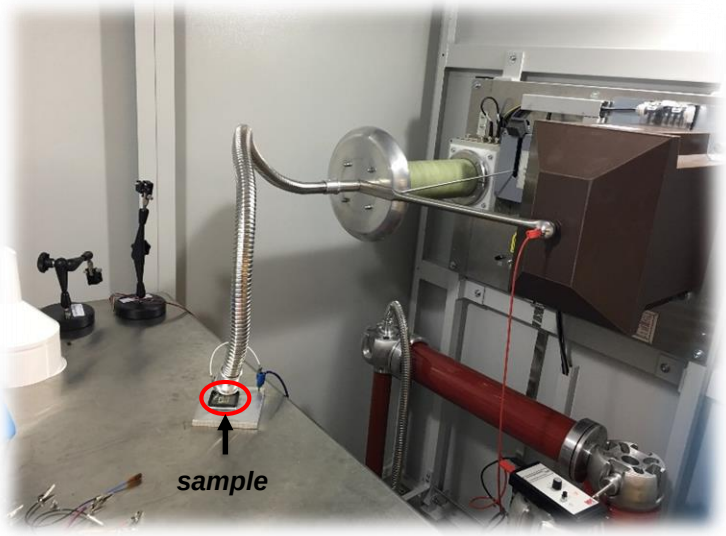
HV tests show increased breakdown voltage for samples with circular traces.

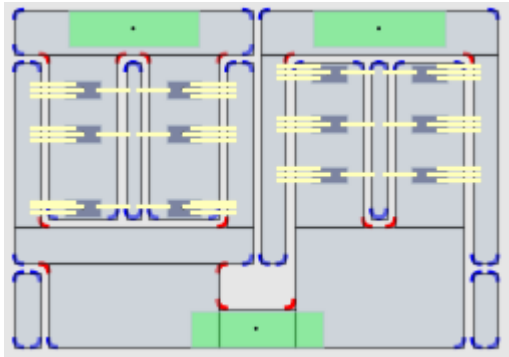
COMPEL 2018

Samples in Silicone Gel



Samples in Fluorinert (liquid dielectric)

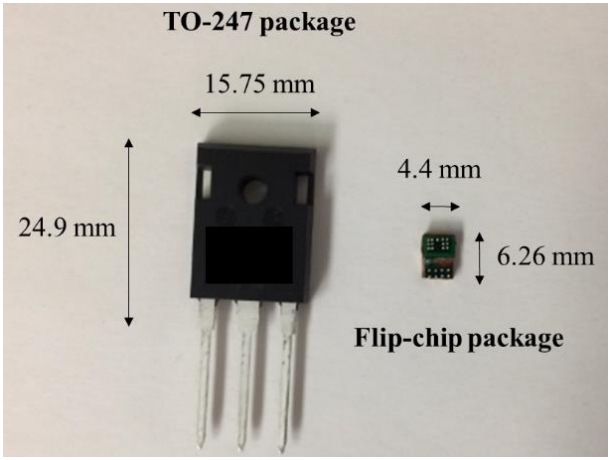


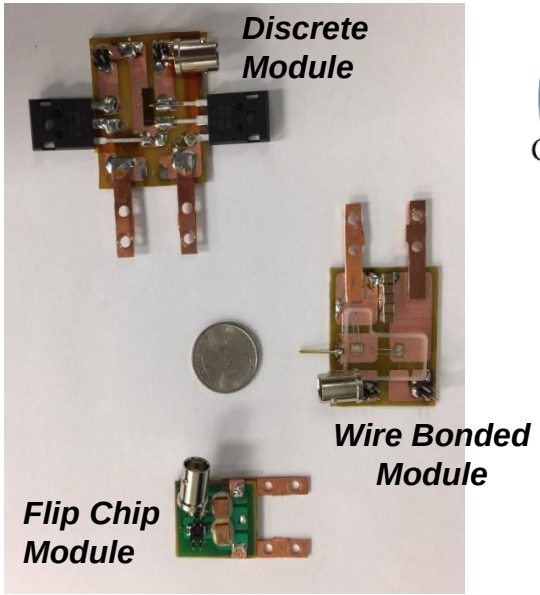


Implementation in PowerSynth

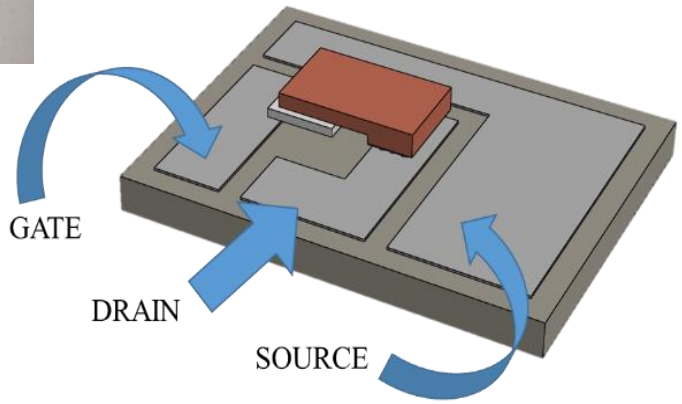
Novel Wire Bondless SiC Power MOSFET Packaging Technique Developed at UA

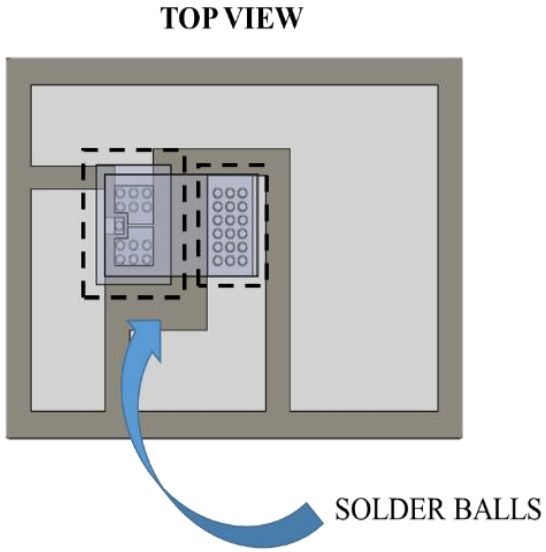
1200 V SiC MOSFET from ROHM Semiconductor (S2301TCSF)

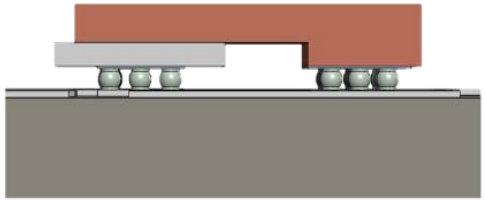




- ***14x reduction in footprint compared to TO-247 package***
- ***Demonstrated reduction in parasitic loop inductance by a factor of 3***

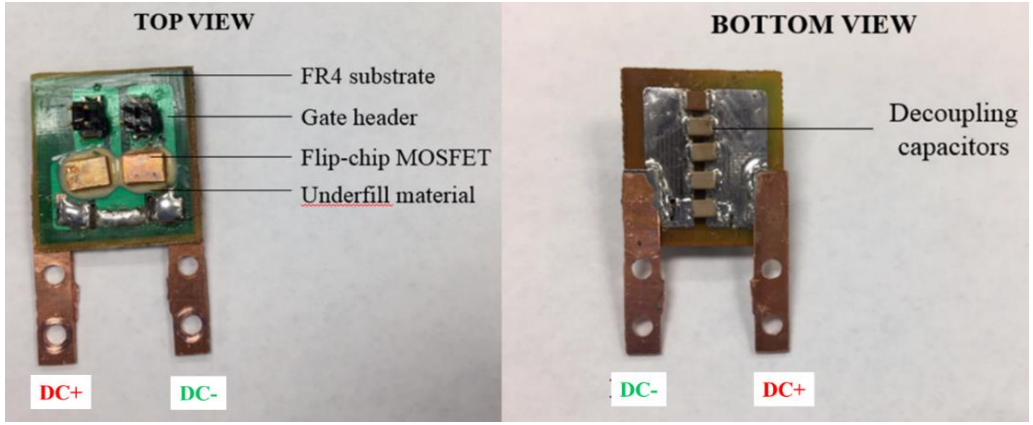




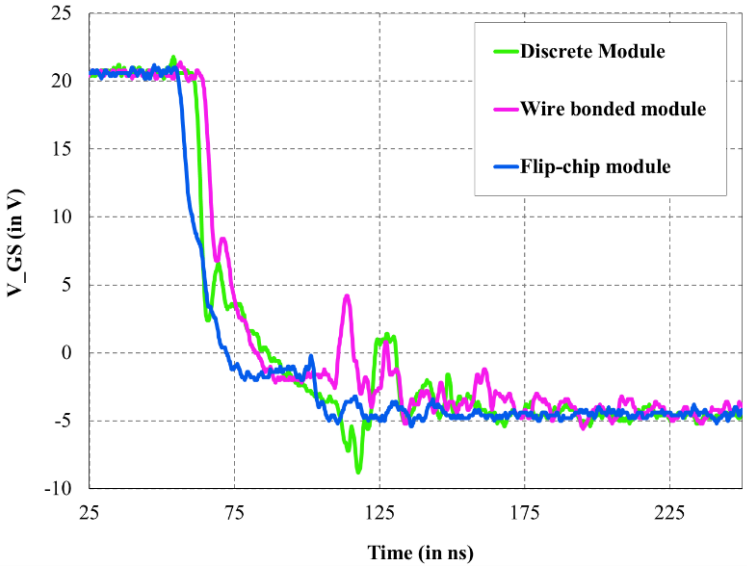


SiC Switching Cell + Vertical Power Loop

Packaging for High Power Density Inverters

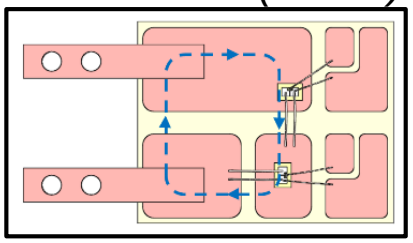


< 5 nH loop inductance @ 16 ns rise time

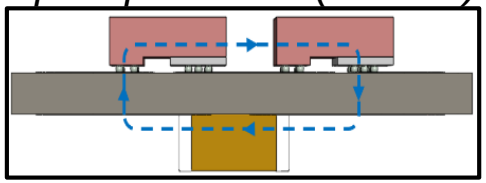


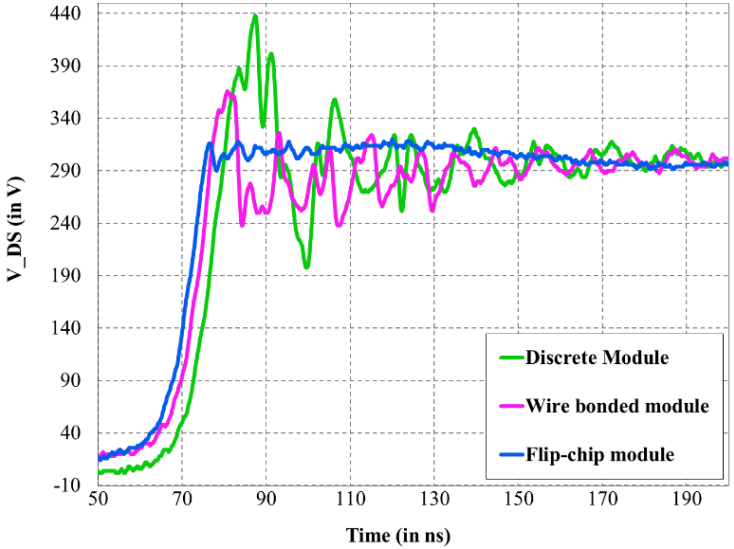
Inductance Paths

Wire bonded (lateral)



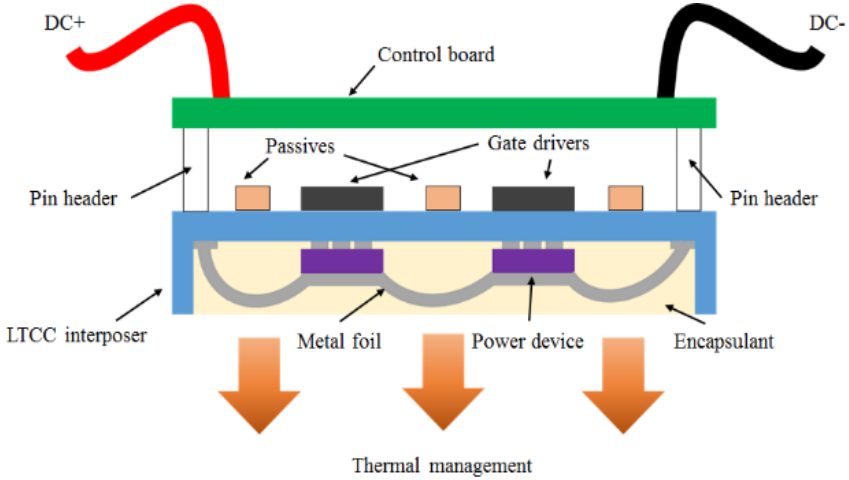
Flip chip bonded (vertical)



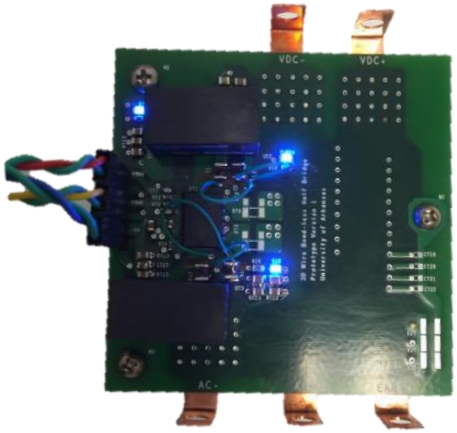


An 3D Wire Bondless Half Bridge with Integrated Gate Driver

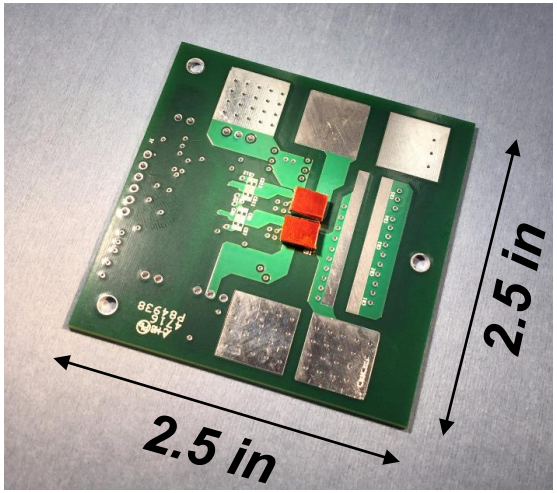
Packaging for High Power Density Inverters



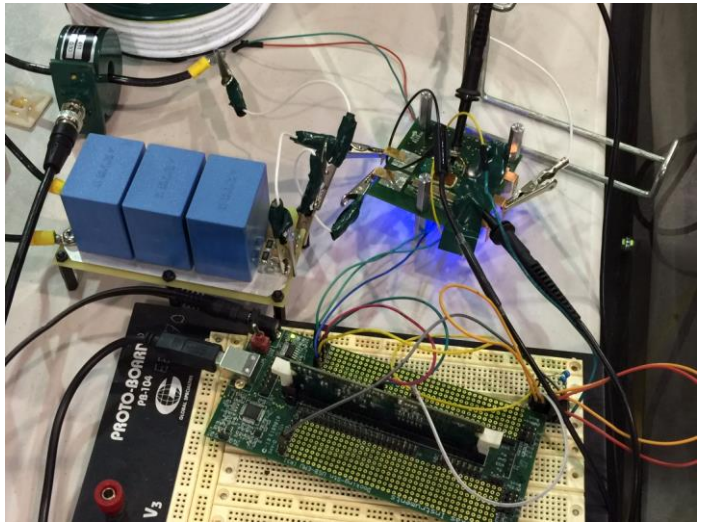
Top side of interposer with Gate Driver and Passives



Bottom side of interposer with Wire bondless MOSFETs



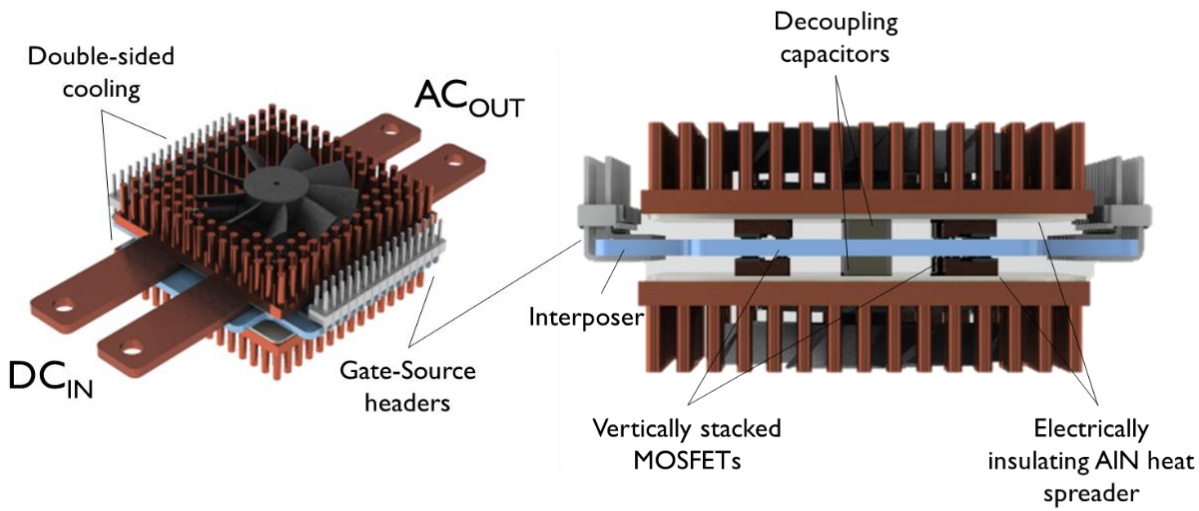
Functioning module on double-pulse test stand at NCREPT



The Flip-Chip Power MOSFETs

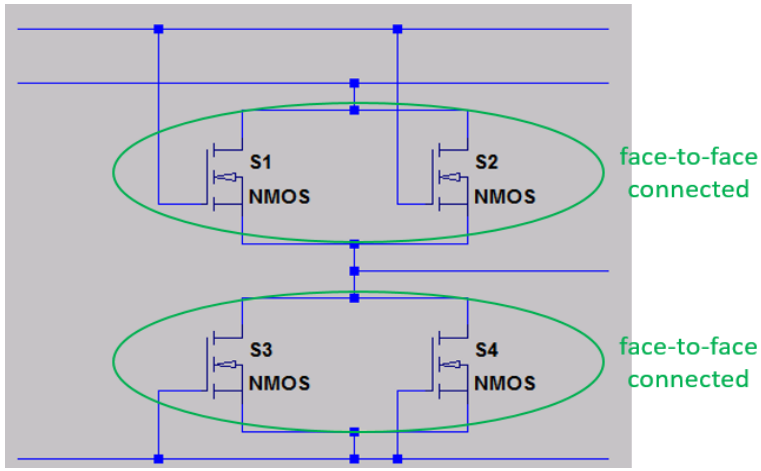
- ***Mechanical Performance***
- ***Electrical Performance***
- ***Thermal Performance***
- ***Manufacturability***

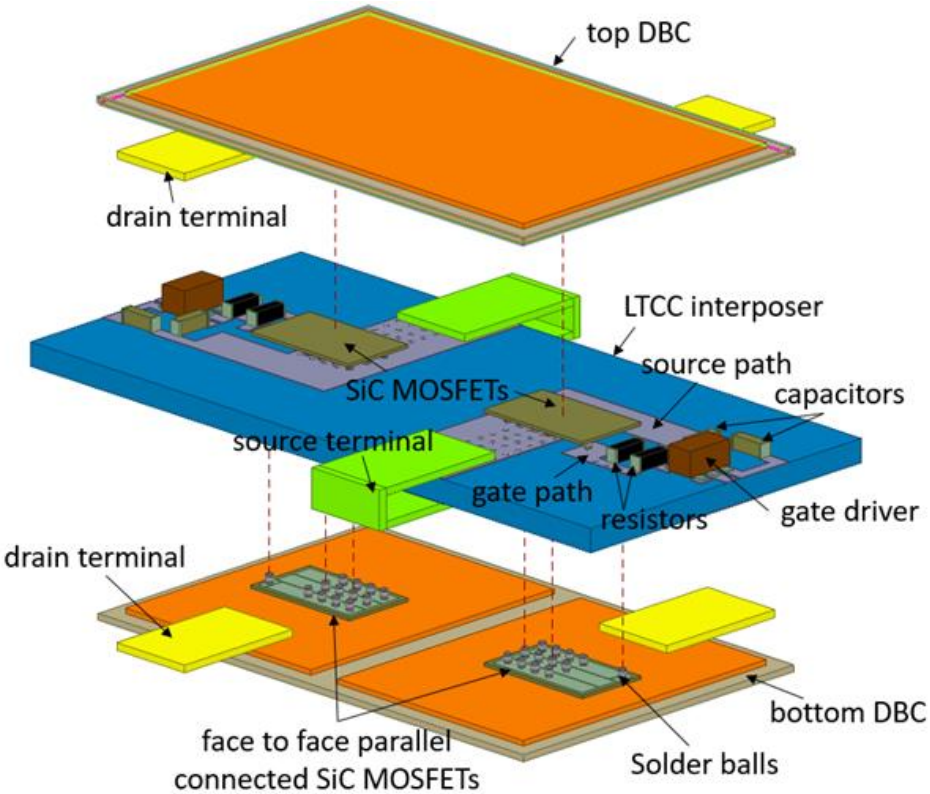
- ***Verifiability***
- ***Reliability***
- ***System Performance***
- ***System Cost***



A concept for a 3D wire bondless SiC power module based on flip-chip MOSFET packages

Vertically Stacked SiC Module

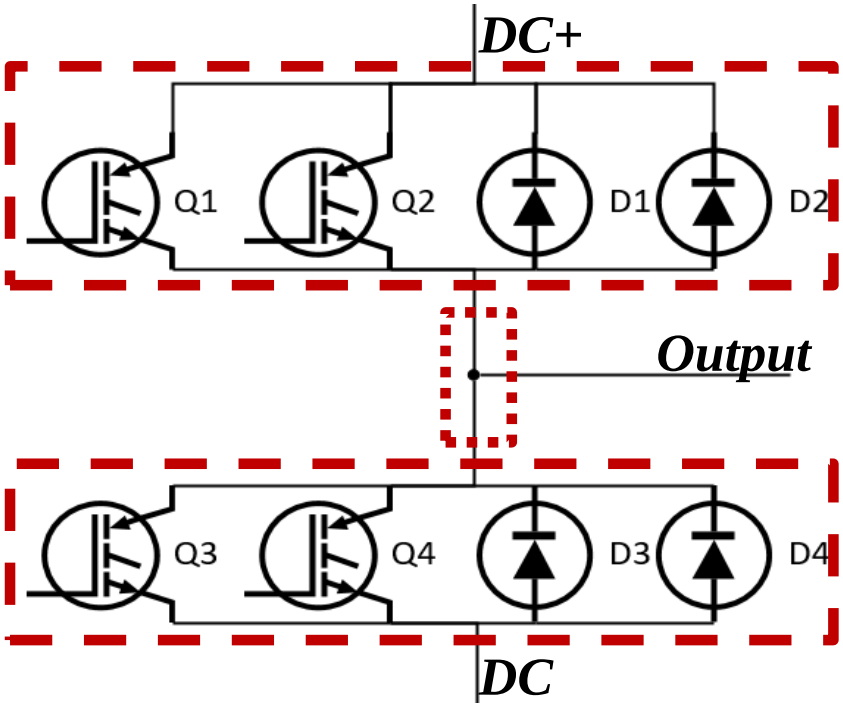




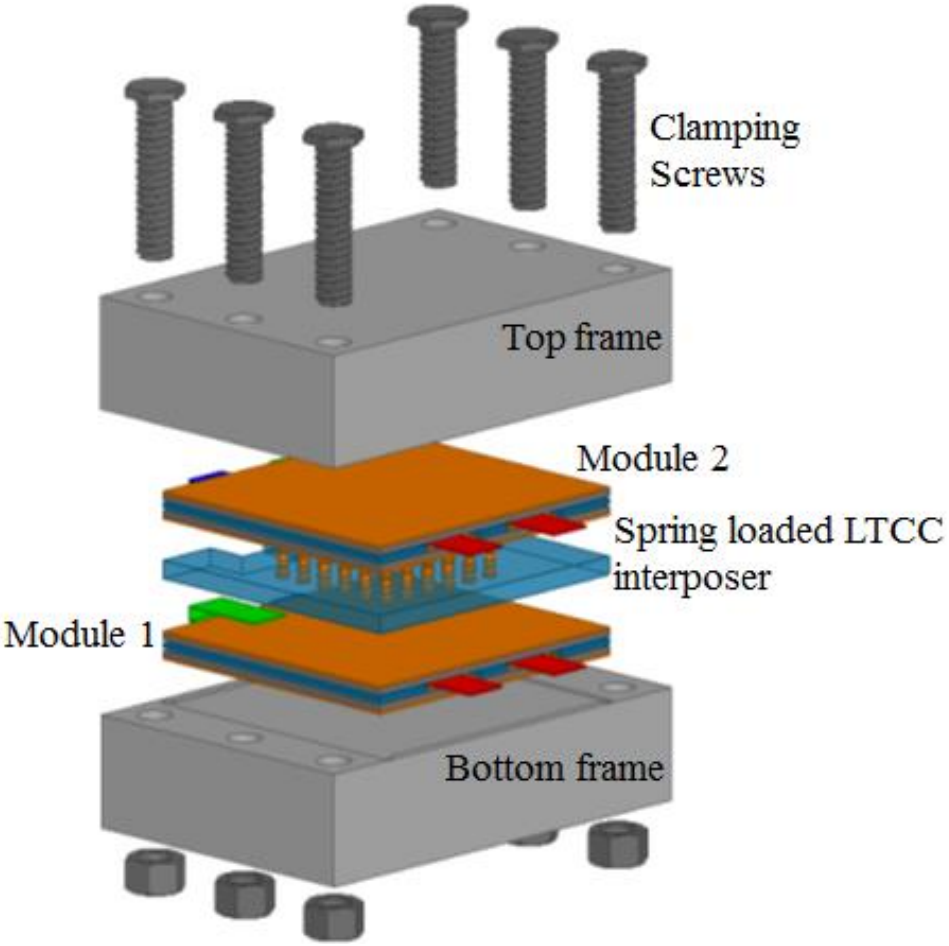
Module-Level 3-D Stack

Key components of 3-D stack:

- ***Two stand-alone wire bondless power modules***
- ***A spring-loaded low temperature co-fired ceramic (LTCC) interposer***
- ***Top and bottom holding frames***
- ***Clamping screws***

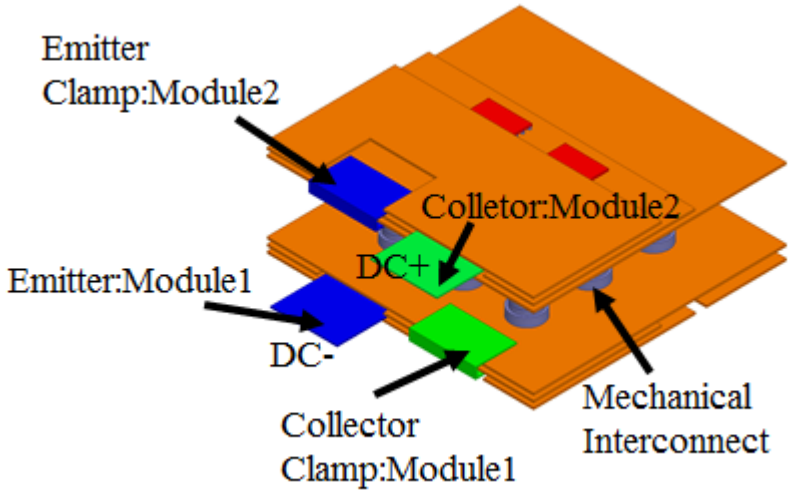


Half-bridge circuit schematic

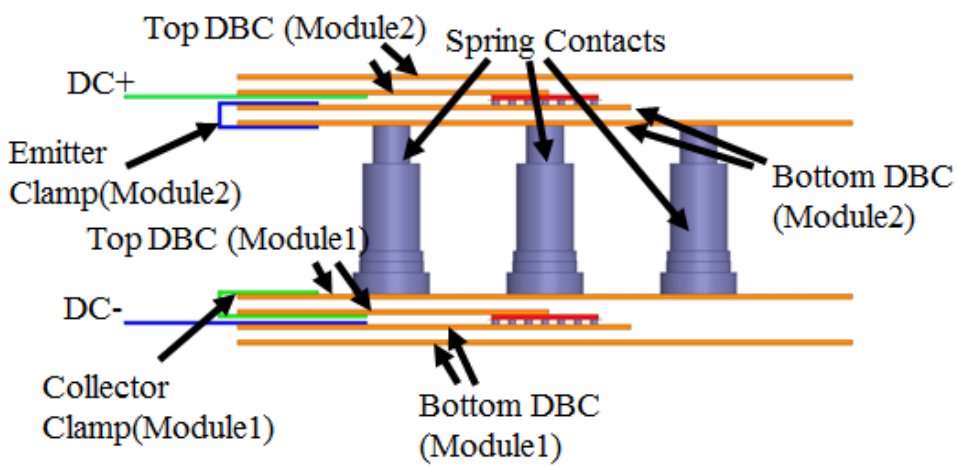


Exploded view of the proposed module-level 3-D wire bondless half-bridge power module

Interconnection Scheme



Interconnection scheme

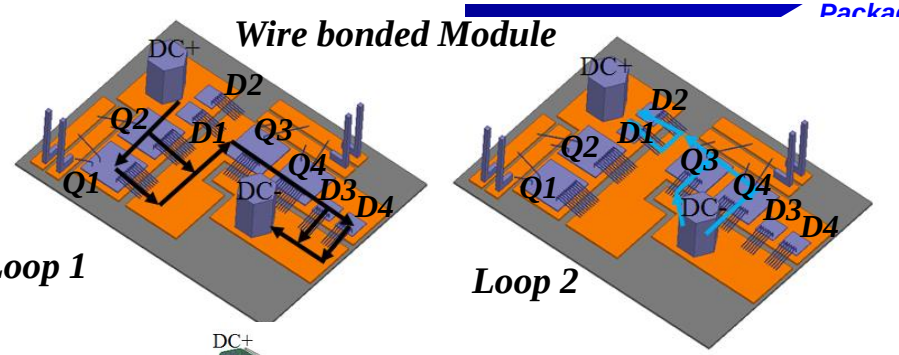


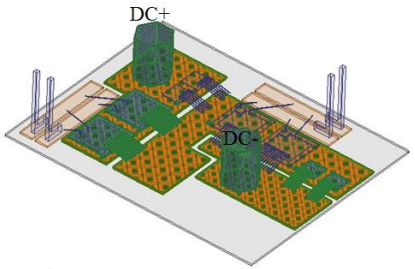
Side view of interconnection scheme

- ***Collector clamp***
  - ***To route the collector of module 1 to outer copper of DBC***
- ***Emitter Clamp:***
  - ***To route the emitter of module 2 to outer copper of DBC***
- ***LTCC Interposer:***
  - ***Spring loaded interposer to establish electrical connection between the collector (module 1) and emitter (module 2) to realize module-level 3-D wire bondless half-bridge stacked power module***

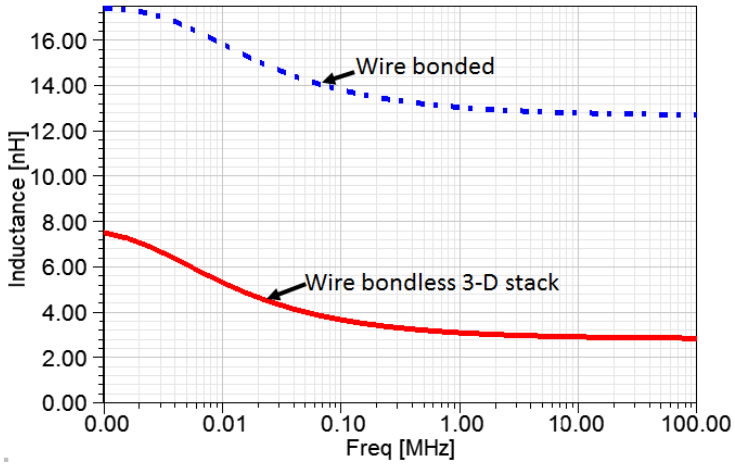
Inductance Minimization

Wire bonded Module





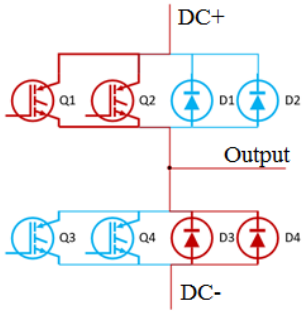
Wire bonded module loop net in ANSYS Q3D

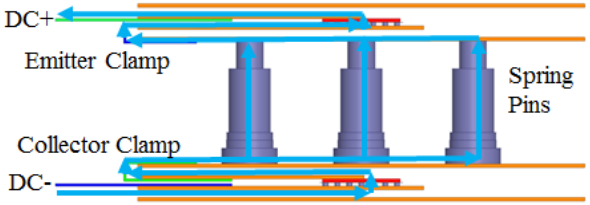


Frequency dependent loop inductance

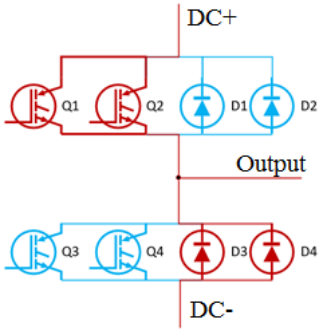
- ***71% reduction in loop inductance @ 100 kHz***

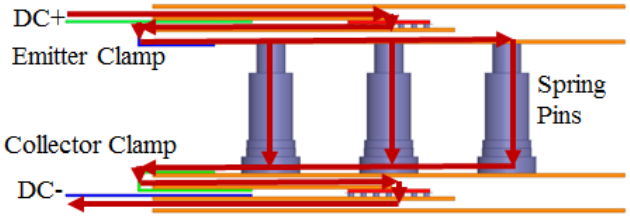
Anti-parallel current path



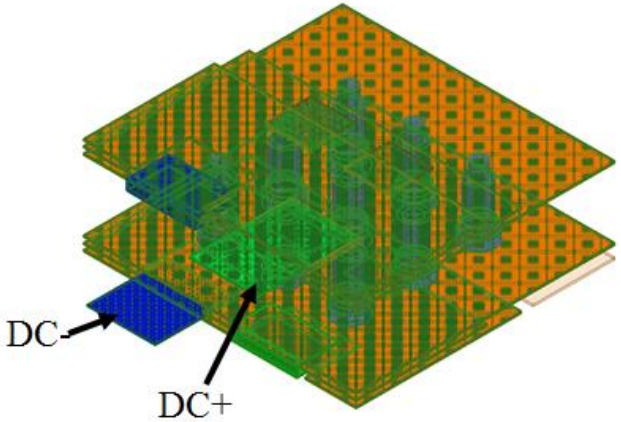


Loop 1



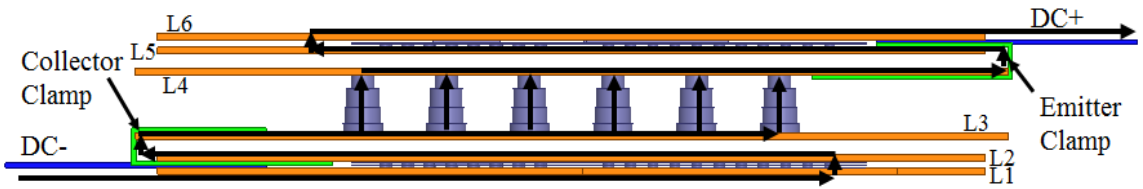


Loop 2

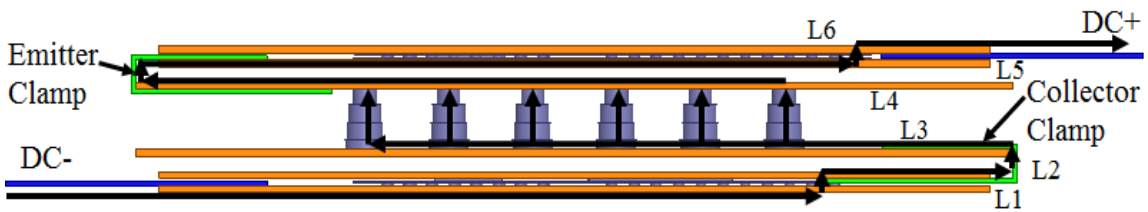


3-D wire bondless module loop net in ANSYS Q3D

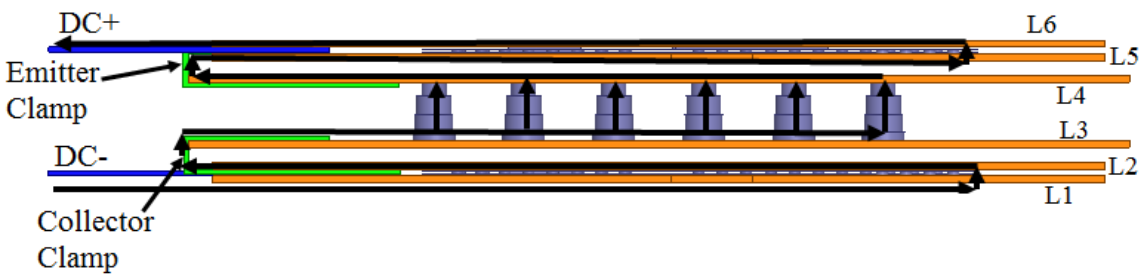
Optimized Connector Placement



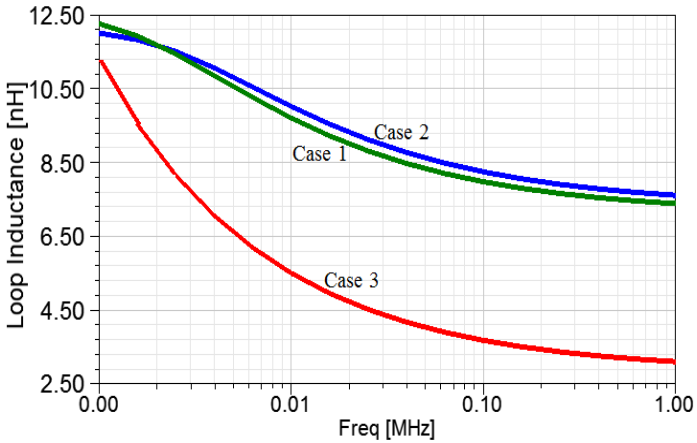
Case 1, Partially violated anti-parallel current path configuration



Case 2, Partially violated anti-parallel current path configuration

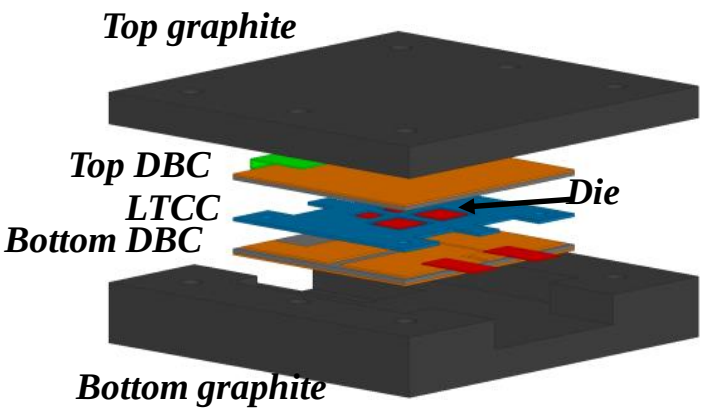


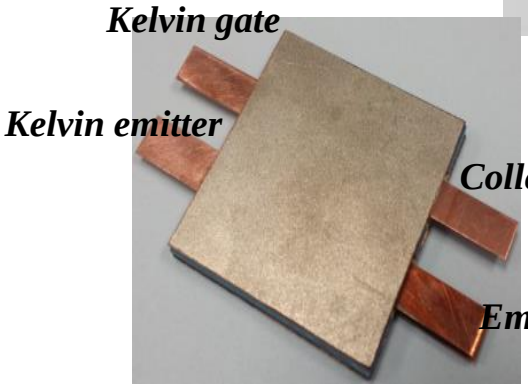
Case 3, Maintained anti-parallel current path configuration

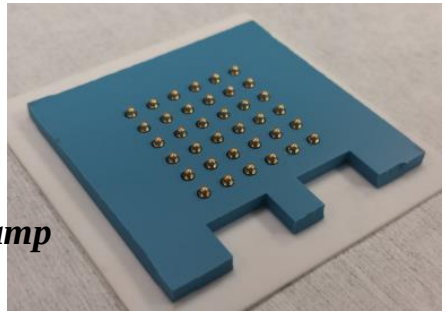


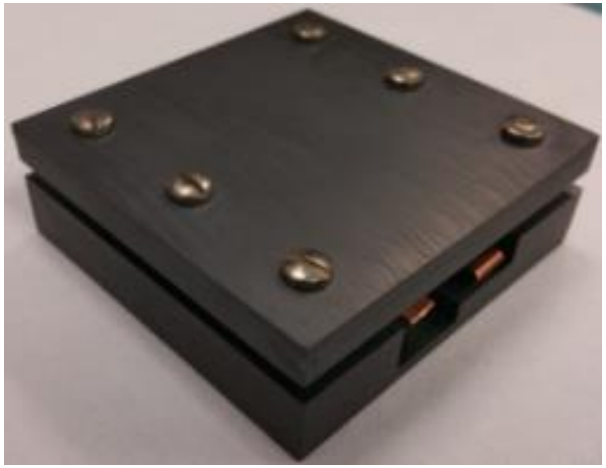
- ***Case 3 yields 57% reduction in loop inductance that is achieved by optimum connector placement following anti-parallel path configuration***

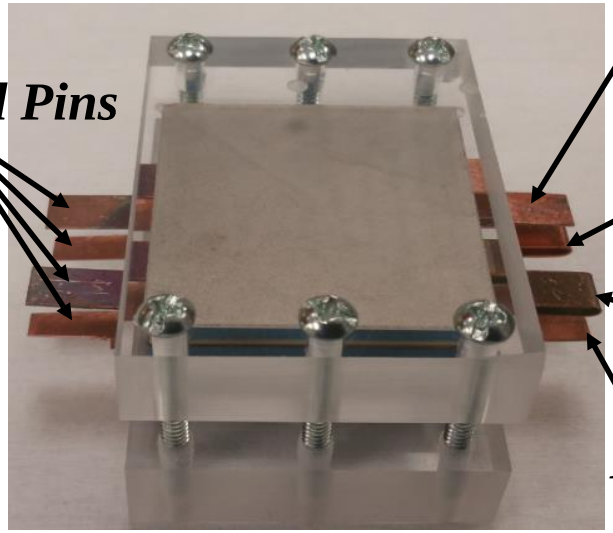
Fabricated Power Module



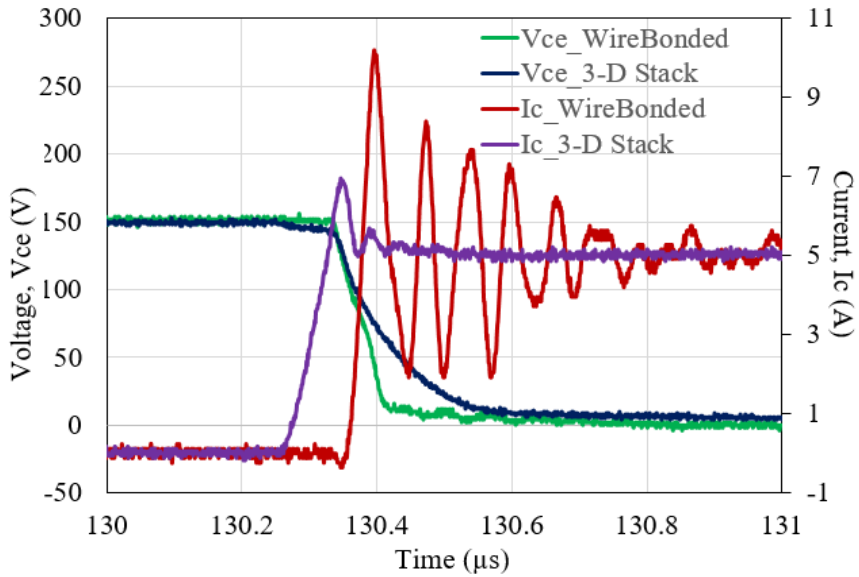


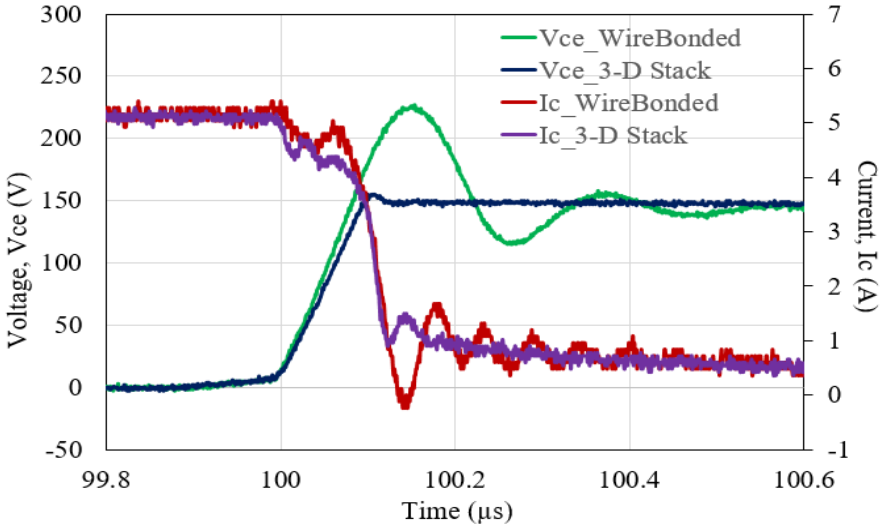


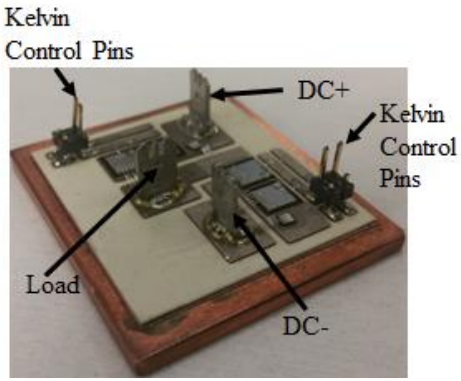




Double-Pulse Test Comparison



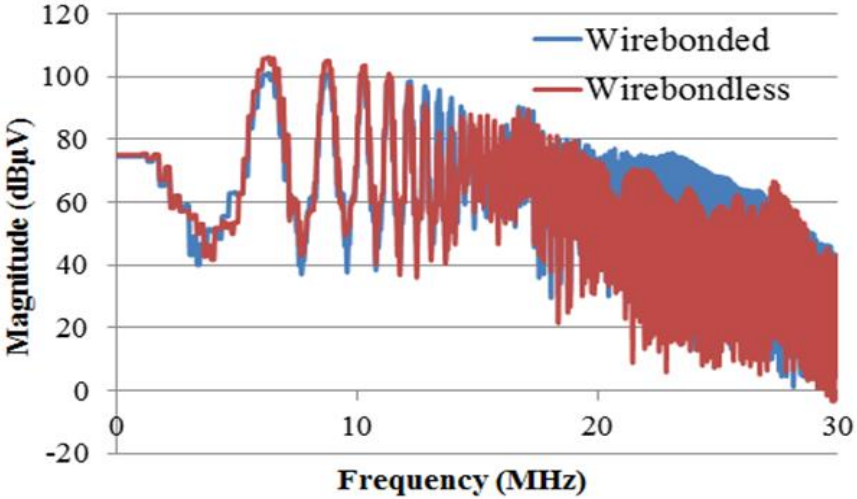




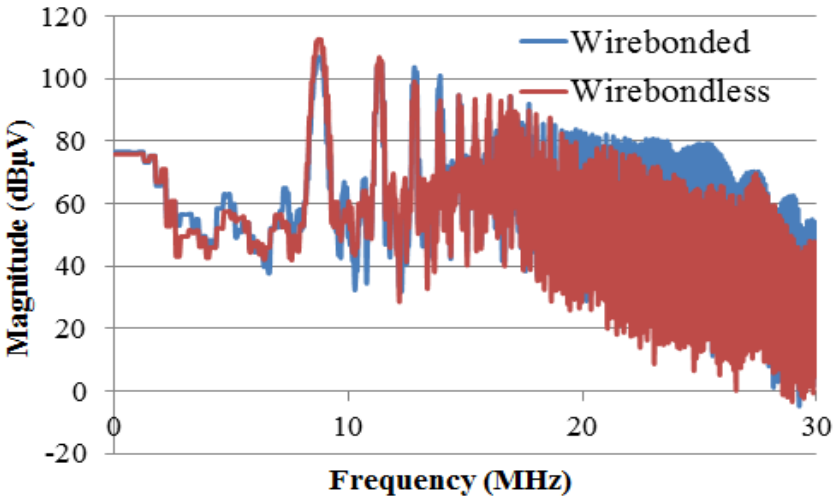
Fabricated wire bonded module for comparison

- ***Turn-on performance improvements***
  - ***30% reduction in peak current overshoot***
  - ***~100 ns reduction in turn on delay***
  - ***Reduction of settling time of turn-on current ringing***
- ***Turn-off performance improvements***
  - ***43% reduction in peak voltage overshoot***
  - ***Reduction of settling time of turn-off current ringing***

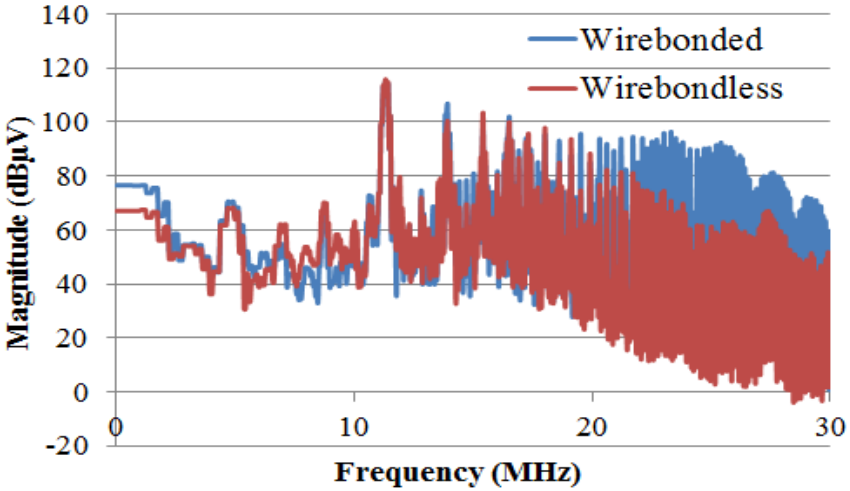
Conducted EMI Characterization



Measured conducted EMI @ 50 kHz



Measured conducted EMI @ 100 kHz



Measured conducted EMI @ 200 kHz

Summary

- **Need for higher efficiency is being driven by all sorts of energy demands**
- **Heterogeneous integration is being driven by the "need for speed", which translates into volumetric reduction and higher efficiency**
- **Wide bandgap IC design provides solutions silicon cannot touch**
- **New design automation approaches are needed for WBG power electronics**
- **Heterogeneous power electronics integration is key to unleashing WBG performance**