Performance, Reliability and Yield considerations in state-of-the-art SiC Diode and MosFET technologies during ramp-up

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SiC History @ ON Semiconductor

2004
TranSiC founded
- works on SiC BJT switch
- prototypes of SBD

2011
Fairchild bought TranSiC
- SBD released on 6” SiC wafer
- MosFET Gen1 start 2013
- setup Epitaxy line
- setup 6” manufacturing line

2015
Gen1 1200V SBD
Gen1 650V SBD generic
Gen 2 650V SBD automotive
Gen1 1200V MosFET
900V MosFET
1700V SBD

2016 2017 2018 2019
ON-Semi bought Fairchild
- annually new technology platforms released
- ramp rates: doubling volume
ON's status chart for SiC

**Diodes:**

- 4A – 50A for 650V, available as discretes
- 6A – 50A for 1200V, and in modules
- 25A – 100A for 1700V, releasing shortly

**MosFET:**

- 80mW 1200V in TO247 released – safe launch from Q2/2019:
- 20mΩ, 40mΩ, 160mΩ in TO247-3L
- Q2 same products in D2PAK-7L, T0247-4L
Large Fab capacity available: >10,000 WSPW
Global development - 24hrs: Asia/EU/US
From 2021: supply chain vertical integrated

SiC 6” Volume ramp-up
Challenges - SiC MosFET in its infancy

SiC IDMs offer passive and active devices in comparable packages and modules
- ease of use
- drastic switching loss reduction
- as of today SiC technology enables *system cost*, *weight* and *size* reduction
Performance SiC MosFET vs IGBT

ON Semi 1200V IGBT 20A vs. SiC MOSFET under identical drive conditions

Paralleling of 20mΩ ON Semi SiC MosFETs vs IGBTs

600V 500A turn on
$V_{GE} = -5 / +20V$
$R_G = 5\Omega$

Eon at 25°C

Eoff at 25°C
1200V Transient comparison FS2 IGBT with FWD Si vs SiC

Double pulse switching
- Active switch 200A FS2
- 100A Si FZ Diode vs 50A SiC
- Temp: 25C
- IC~150A
- VCE~600V
- Rg~120hm (di/dt~5A/ns)

- \( \Delta E_{SW} \approx 25C \sim 15\% \) improved
- \( \Delta E_{SW} \approx 125C \sim 30\% \) improved
Performance SiC MosFET vs Si SuperJunction FETs

Example 900V SiC FET vs 600V SuperJunction FET for CCM PFC

due to low $Q_G$, $Q_{OSS}$ and $Q_{RR}$ – SiC FET excellent in LLC as well
Challenges - SiC chip in discrete package

Large SiC chips in discrete packages

<table>
<thead>
<tr>
<th>Material</th>
<th>Si</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Elastic Modulus (Gpa)</td>
<td>130</td>
<td>410</td>
</tr>
<tr>
<td>Tensile strength (Mpa)</td>
<td>7000</td>
<td>3440</td>
</tr>
<tr>
<td>Hardness (mohs)</td>
<td>6.5</td>
<td>9</td>
</tr>
<tr>
<td>CTE (1E-6/C)</td>
<td>2.6</td>
<td>4.5</td>
</tr>
</tbody>
</table>

Temperature cycling (-55C – 150C)

FEA modeling discovers:

Dependent on chip design, certain locations experience >20 times stress and strain during cycling than Silicon chip

Overcame problem with patented design and optimized assembly BOM
Stress in overmolded power modules

Stress index S.I. \( (= E_{MC} \times CTE_{MC}) \)

eg by Nguyen (1993)

Young modulus MC1 vs MC2

CTE MC1 vs MC2

Z-Axis deformation ~290um

Z-Axis deformation ~160um

Package reliability (power cycling), cooling performance etc strongly dependent on material system. Fracture mechanics simulation possible
Challenge - Edge termination in moisture

Anodic corrosion in moist environments under stress

- H3TRB stress 85%/85C/80%BV

- Corrosion fails within 1\textsuperscript{st} 168hrs

Proper SiC edge design survives >5000hrs under worst case H3TRB acceleration without any visible changes or electrical drifts
Challenge - SiC dicing

SiC dicing typically done using
- diamond sawing (like Silicon but slower, more blade consumption)
- laser assisted methods
- plasma assisted methods

500um chip/side view

<table>
<thead>
<tr>
<th></th>
<th>Si-face</th>
<th>C-face</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>good</td>
<td>poor</td>
</tr>
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</table>

Trade off between dicing speed, scribe lane width, chip size and tape selection (glue thickness)
much development on equipment and consumable side to optimize COO of SiC dicing
strong correlation to product robustness
Gate oxide integrity for SiC MosFETs and TDDB

In mass production SiC MosFETs need:

- optimized cleaning and gate oxide
- Very low electric field (<3 MV/cm)
- tight Fab contamination control
- highest substrate and Epi quality

- continuous monitoring of extrinsic failure rate required
Challenges – Gate oxide integrity

Typical failure cases for GOX (HTGB – burn-in):

...caused by typical Fab contaminations and process imperfections and material defects/roughness
D0 and Fab Yields for large die size

Size comparison: 200A Si IGBT and (equivalent) SiC MosFET

feature size IGBT: 0.3um
SiC FET: >1.0um

Substrate and Epi defects and differences in SiC Fab process lead to pronounced Yield detractors for “large” die sizes
Challenges - SiC Epitaxy and defectivity control

Tracing back burn-in failures to substrate defects

Made visible by post Epi scans
Epitaxy trend

Epitaxy quality keeps improving
- high resolution Metrology
- selection of incoming substrate
- improved parts cleaning

Auto defect classification before
Fab start to exclude killer defects

Time [several month]
Epi defect Yield over several month grouped by time after PM/HW change
Screening for new SiC “high dvdt” failure modes

Discrete **silicon** devices are speed-limited due to their intrinsic BJT latch-up effect (fast IGBT turn-off)

SiC MosFET dvdt simulation

pass at 26V/ns  
fail at 28V/ns

Si IGBT in latch-up condition  
SiC FET unit cell in latch-up condition

308V/ns
ON-Semi requires its SiC MOSFETs to undergo repetitive continuous operation tests (168 h). Where both Body-Diode and MOSFET are stressed at different \( \frac{dv}{dt} \), \( ID \) and frequencies

- H-Bridge in Continuous Conduction mode
- \( V_{DC} = 800 \) V
- \( f_{SW} = 25 \) kHz
- \( T_J = 100 \) °C, \( I_{LOAD} \) controlled
- Test duration = 168 hrs
- \( R_{gon} = 1 – 22 \) Ohm
- \( R_{goff} = 1 – 5 \) Ohm
- \( V_{GS} = +20/-5 \) V
- 3 Lots 12 devices per Lot
SiC - Surge current testing

- Pulse shape and length can be freely controlled
- Useable for Diodes and MosFETs (1\textsuperscript{st} and 3\textsuperscript{rd} quadrant)
- Single and repetitive surge testing
SiC devices in very strong in avalanche
- Avalanche energy scales well with die area

In hybrid setup SiC SBD can project Si IGBTs from voltage overshots.
For SiC FETs less overvoltage margin required
Diode avalanche robustness

Each series is 10k pulses

single-shot rating

UIS failure repetitive

single-shot failure

forward drop at rated current (V)

average $I_{AVAL}$ in the series (A)

$10k$ pulses

$I_1$

$10k$ pulses

measure $I$-$V$

$I_1 + 10$ Amp

$I_1 + 20$ A

$100$ $120$ $140$ $160$ $180$

forward drop at rated current (V)

average $I_{AVAL}$ in the series (A)
ON SiC Vertical Integration

Internal and external boule supply
several sources: EU, US

SiC Wafering
EU

SiC Epi, Metrology
US, Asia

SiC FE Process
Asia

Applications
dicing, assembly, test
Asia

WAT/Sort test
Asia

Thinning, backmetal
Asia

Public Information
ON Semiconductor®
Summary

- Silicon carbide product ramp-up accelerated due high MosFET demand
- Multiple package and module setups are available/under rollout
- SiC devices can replace Si Diodes, SuperJunction MosFETS and IGBTs
- Challenges:
  - SiC stress in discrete and module packages can be solved
  - GOX integrity – failure modes can be screened well
  - Large SiC chips vs Yield – still inhibitive
  - Epitaxy, dicing improvements in conjunction with equipment supplier
- Robustness
  - SiC allows extreme transient dvdt and didt – failure modes can be screened well
  - SiC surge, short circuit and avalanche
- SiC needs vertical integration for cost, quality and supply
Thank You

any questions:

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