APEC 2019 PSMA Industry Session IS11: "Current reliability and product qualification topics for SiC and GaN wide band gap devices", March 20th, 2019

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World’s First GaNFast™ Power ICs

Fastest, most efficient GaN Power FETs

- >20x faster than silicon
- >5x faster than cascoded GaN
- Proprietary design
- Gate is fragile and sensitive to noise

First & Fastest Integrated GaN Gate Drivers

- >3x faster than any other gate driver
- Proprietary design
- 30+ patents granted
- Fast, protected gate, no need for negative drive

Up to 40MHz switching, 5x higher density & 20% lower system cost

- Simple, fast and reliable
- Easy to use and package
Enabling Advanced Technologies

Reliability corners defined using reliability physics based lifetime models

Robust PDK = successful integration

Increasing Integration

Design corners

Process corners

Reliability corners
### Device element | Reliability model requirement
--- | ---
Capacitor | Guaranteed by proprietary design, verified by characterization – reliability models not required
Resistor | Mature process and Foundry qualified
Electro-migration | Reliability models required
LV GaNFET | Reliability models need to replicate stresses seen in real application
HV GaNFET | Reliability models need to replicate stresses seen in real application
Typical Application: Mobile Chargers

MacBook <100 kHz
<6.5 W/in³, 92%

Navitas ~300 kHz
Power density = 39 W/in³

- ACF (ZVS) Topology
- 300kHz – 1 MHz
- 120 V – 240 V AC

65W USB-PD
Application Profile for ACF Charger

- **Full Power** ($T_{DUT} = 100^\circ C$)
  - Voltage
  - Current
  - 1 us/div

- **Light Load** ($T_{DUT} = 50^\circ C$)
  - Voltage
  - Current
  - 5 us/div

- **Burst Mode** ($T_{DUT} = 25^\circ C$) (No Load)
  - Voltage
  - Current
  - 500 us/div

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Full Power Stress Breakdown

Full Power \((T_{DUT} = 100^\circ C)\)

- Voltage
- Current
- 1 us/div

Stress seen by HV GaNFET:
- High Temperature
- High Frequency
- High Voltage (Switching)
- High Current

Stress seen on LV GaNFET:
- High Temperature
- High Frequency
Burst Mode Stress Breakdown

**Burst Mode ($T_{DUT} = 25^\circ C$) (No Load)**

- **Stress seen on HV GaN FET:**
  - Low Temperature
  - Low Frequency (~static)
  - High Voltage (Blocking)
  - Low/No Current

- **Stress seen on LV GaN FET:**
  - Low Temperature
  - Low Frequency (~static)
# Reliability Stresses to Model

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<thead>
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<th>Test method used to characterize</th>
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HTRB Acceleration & Lifetime Models

Voltage/Temperature

<table>
<thead>
<tr>
<th>Voltage</th>
<th>100°C</th>
<th>125°C</th>
<th>150°C</th>
</tr>
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<tbody>
<tr>
<td>650V</td>
<td>✓</td>
<td></td>
<td>✓</td>
</tr>
<tr>
<td>700V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>750V</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>

Lifetime = $A \times (V^{-n}) \times \left( e^{\frac{E_A}{kT}} \right)$

$V = 700 \text{ V}, \text{Temperature Acceleration}$

$T = 150 \degree C, \text{Voltage Acceleration}$

$Time \ to \ Fail \propto \left(\frac{1}{\text{Voltage}}\right)^{n=1.86}$

$Time \ to \ Fail \propto e^{\left(\frac{E_A=0.91eV}{kT}\right)}$

Projected Application Condition Using Model

Lifetime in no load condition is $>1E8$ years, significant built-in margin
## Reliability Stresses to Model

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Gate Reliability Acceleration Models

<table>
<thead>
<tr>
<th>Voltage/Temperature</th>
<th>25°C</th>
<th>50°C</th>
<th>75°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.5V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>10.0V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>10.5V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

Static and switching stresses have same acceleration factors

\[ 
\text{Time to Fail (hrs)} \propto e^{(E_a = -0.63eV)/kT} 
\]

T=75 °C, Voltage Acceleration

\[ 
\text{Time to Fail (hrs)} \propto \frac{1}{(\text{Voltage})^{n=60.5}} 
\]

V= 10V, Temperature Acceleration

\[ 
\text{Time to Fail (hrs)} \propto e^{(E_a = -0.65eV)/kT} 
\]

T=75 °C, Voltage Acceleration

\[ 
\text{Time to Fail (hrs)} \propto \frac{1}{(\text{Voltage})^{n=59.7}} 
\]

T=75 °C, Temperature Acceleration

\[ 
\text{Time to Fail (hrs)} \propto e^{(E_a = -0.63eV)/kT} 
\]

V= 10V, Temperature Acceleration

\[ 
\text{Time to Fail (hrs)} \propto e^{(E_a = -0.65eV)/kT} 
\]
Frequency Acceleration

Lifetime improves at higher frequencies

V=11V, T=25°C, 50% duty cycle

V=11V, T=25°C, 100KHz

Frequency ↓ / Duty cycle ↑ / Pulse width ↑ ⇔ Closer to static stress

Typical applications for GaN devices operate at >100KHz

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Gate Reliability Lifetime Estimation

Integrated regulator guarantees operation with 10+ years of estimate life
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Mission Profile Driven HTOL (ZVS)

Full Power ($T_{DUT} = 100^\circ C$)

- Current
- Voltage

1 us/div

ZVS test bench replicates stresses seen in ACF application
Failure Mode Matters

650V, 150°C HTOL

System degradation

Device degradation

Group 1: In-situ system power loss monitoring

Normalized Power loss per cell

Stress Time

Group 2: Measure parameters at interim intervals

Parametric failure probability

Stress Time

1%

10%

100%

1000V, 150°C HTOL
Failure Mode Matters

650V, 150°C HTOL

Parametric failure = minor efficiency degradation

Lifetime estimation using parametric failure → conservative approach

Group 1: In-situ system power loss monitoring

Group 2: Measure parameters at interim intervals

System degradation

Device degradation

System failure

Parametric failure

Lifetime estimation using parametric failure → conservative approach
HTOL-based Lifetime Model

<table>
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<tr>
<th>Voltage/Temperature</th>
<th>100°C</th>
<th>125°C</th>
<th>150°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>550V</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>575V</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>600V</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>625V</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>650V</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

\[
\text{Time to Fail (hrs)} \propto \left( \frac{1}{\text{Voltage}} \right)^{17.2}
\]

\[
\text{Time to Fail (hrs)} \propto e^{\frac{E_a}{kT}}
\]

- $T = 150 ^\circ C$, Voltage Acceleration
- $V = 650 \text{ V}$, Temperature Acceleration
<table>
<thead>
<tr>
<th>Mode</th>
<th>Voltage</th>
<th>DUT $T_{\text{case}}$</th>
<th>Typical time spent (1 charge/day)</th>
<th>Relevant reliability stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Power</td>
<td>460V</td>
<td>100°C</td>
<td>8 hours (33%)</td>
<td>HTOL</td>
</tr>
<tr>
<td>Light Load</td>
<td>460V</td>
<td>50°C</td>
<td>4 hours (17%)</td>
<td>HTOL</td>
</tr>
<tr>
<td>No Load (burst)</td>
<td>340V</td>
<td>25°C</td>
<td>12 hours (50%)</td>
<td>HTRB HTOL</td>
</tr>
</tbody>
</table>

Assuming worst case scenario at 240VAC

HTOL is more aggressive than HTRB
### Lifetime Estimation Methodology

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<td>HTOL</td>
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**Temperature Acceleration Factor**

$$AF_{\text{temp}} = e^{rac{E_a}{k}(T_{\text{application}} - T_{\text{reliability}})}$$

$E_a = 0.71\text{eV}$

**Voltage Acceleration Factor**

$$AF_{\text{voltage}} = \left(\frac{V_{\text{reliability}}}{V_{\text{application}}}ight)^n$$

$n = 17.2$

---

**Total Acceleration Factor**

- **Full power:** $AF_{\text{total}}$ = $AF_{\text{temp}} \times AF_{\text{voltage}}$
- **Light load:** $AF_{\text{total}}$ = $AF_{\text{temp}} \times AF_{\text{voltage}}$
- **No Load:** $AF_{\text{total}}$ = $AF_{\text{temp}} \times AF_{\text{voltage}}$

**Lifetime estimate in application**

$$AF_{\text{Total}} \times \text{Time to failure in reliability (TTF_{reliability})}$$

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Lifetime Estimation in Charger Application

Significant built-in reliability margin \( \rightarrow \) even at worst case conditions (exceeds 10+ year lifetime requirement)
## Reliability → Qualification → Release

### Reliability models on IC building blocks = Robust design

### Mission profile driven reliability = Protected Customer

### Comprehensive reliability monitoring

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<table>
<thead>
<tr>
<th>Reference</th>
<th>Test Conditions</th>
<th>Duration</th>
<th>Lots</th>
<th>S.S.</th>
</tr>
</thead>
<tbody>
<tr>
<td>JESD22-A113</td>
<td>Preconditioning (MSL1): Moisture Preconditioning + 3x reflow: HAST, UHAST, TC &amp; PC</td>
<td>N/A</td>
<td>3</td>
<td>308 PASSED (0/308)</td>
</tr>
<tr>
<td>JESD22-A104</td>
<td>Temperature Cycle: -55°C / 150°C</td>
<td>1,000cy</td>
<td>3</td>
<td>77 PASSED (0/231)</td>
</tr>
<tr>
<td>JESD22-A122</td>
<td>Power Cycle: Delta TJ = 100°C</td>
<td>10,000cy</td>
<td>3</td>
<td>77 PASSED (0/231)</td>
</tr>
<tr>
<td>JESD22-A110</td>
<td>Highly Accelerated Stress Test: 130°C / 85%RH / 100V Vgs</td>
<td>96hrs</td>
<td>3</td>
<td>77 PASSED (0/231)</td>
</tr>
<tr>
<td>JESD22-A108</td>
<td>High Temperature Reverse Bias: 150°C / 500V Vgs</td>
<td>1,000hrs</td>
<td>3</td>
<td>77 PASSED (0/231)</td>
</tr>
<tr>
<td>JESD22-A108</td>
<td>High Temperature Gate Bias: 150°C / 500V Vgs</td>
<td>1,000hrs</td>
<td>3</td>
<td>77 PASSED (0/231)</td>
</tr>
<tr>
<td>JESD22-A108</td>
<td>High Temperature Operating Life</td>
<td>1,000hrs</td>
<td>3</td>
<td>77 PASSED (0/231)</td>
</tr>
<tr>
<td>JESD22-A108</td>
<td>Early Life Failure Rate</td>
<td>24 hrs</td>
<td>3</td>
<td>1,000 PASSED (0/1,000)</td>
</tr>
<tr>
<td>JS-001-2014</td>
<td>Human Body Model ESD</td>
<td>N/A</td>
<td>1</td>
<td>3 PASSED 0/3</td>
</tr>
<tr>
<td>JS-002-2014</td>
<td>Charged Device Model ESD</td>
<td>N/A</td>
<td>1</td>
<td>3 PASSED 0/3</td>
</tr>
</tbody>
</table>

### Metric | Results
--- | ---
Equivalent device hours tested* | 1.5 billion hours
FIT* | 0.6

*Statistics calculated from HTOL tests

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### GaNFast™ POWER ICs

Now in high volume production!

- Quality
- Speed
- Efficiency
GaNFast Chargers now in production

**Fast**
Up to 3x more power
Up to 3x faster charging

**Mobile**
Half the size & weight of traditional chargers

**Universal**
One charger for **ALL** your devices
*One and Done!!*

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**AUKEY**

- 27W
- 24W
- 30W

**RAVPower**

- 45W

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